

United States Patent

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 [73] Assignee **RCA Corporation**

Technical Report No. RADC-TR-65-74; Rome Air Development Center, A.F.S.C., Griffis A.F.B., N.Y.; May 1965; pp. 27-35 (340/173.1)

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[54] **LOW INDUCTANCE INTERCONNECTION OF CRYOELECTRIC MEMORY SYSTEM**
 9 Claims, 7 Drawing Figs.

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 H05k 7/06

[50] Field of Search. 340/173.1,
 174 (MA); 339/(Inquired), 17 (F), 19, 143;
 174/(Inquired), 36, 88, 117.11

[56] **References Cited**

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ABSTRACT: A length of flexible insulating material such as Mylar or Kapton having parallel conductors on one surface and including a magnetic field shield insulated from the conductors. The parallel conductors are connected at one end to lines at one edge of one cryoelectric memory plane and at the other end either to lines at the corresponding edge of the next adjacent plane, or to a terminal bar whose lines and shield are similar to that of the memory plane. The adjacent plane, in this case, is also connected to the terminal bar but via a second connector such as described. The shield comprises side-by-side discrete conductive sections insulated from one another, each section registering with, that is, lying under (or over) a pair of conductors. Each adjacent pair of conductors is driven in such manner that one carries current in one direction and the other "simultaneously" carries an equal amount of current in the opposite direction.

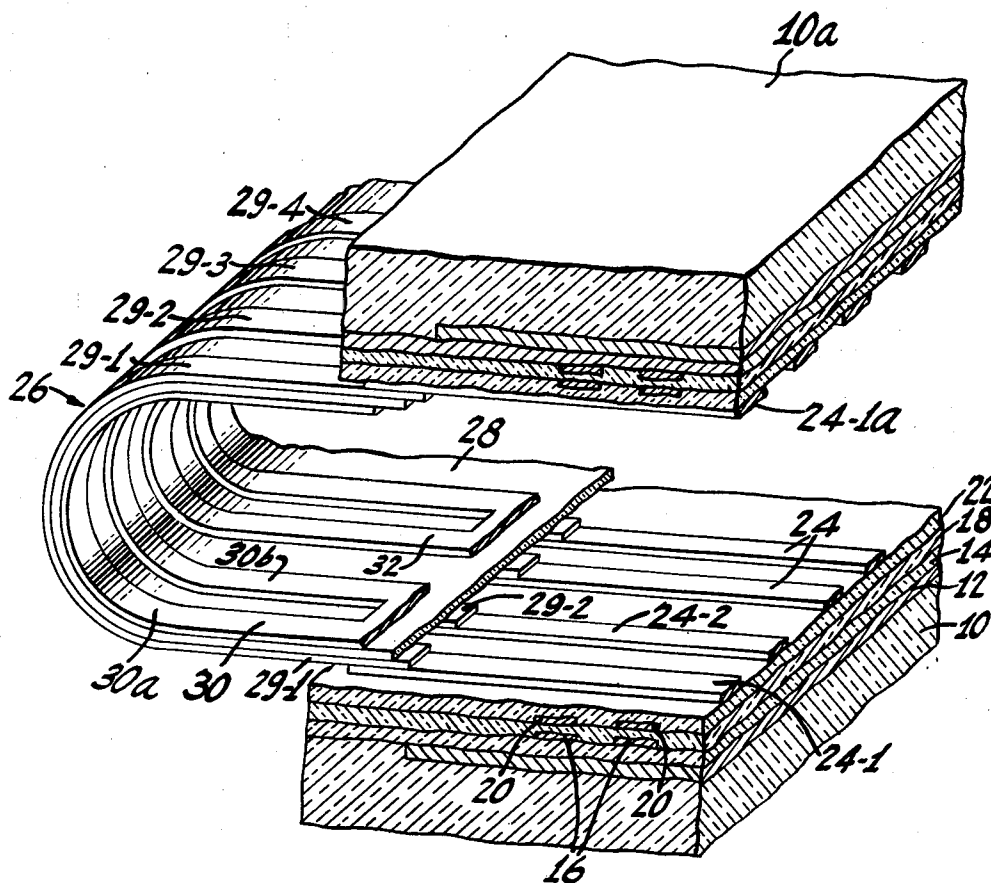


Fig. 1.

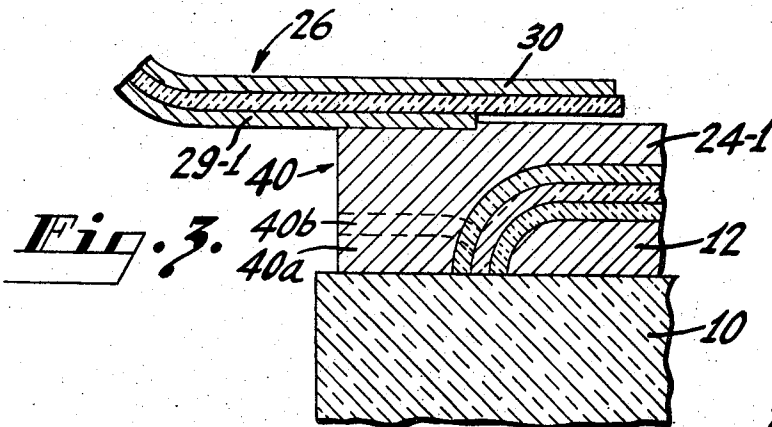
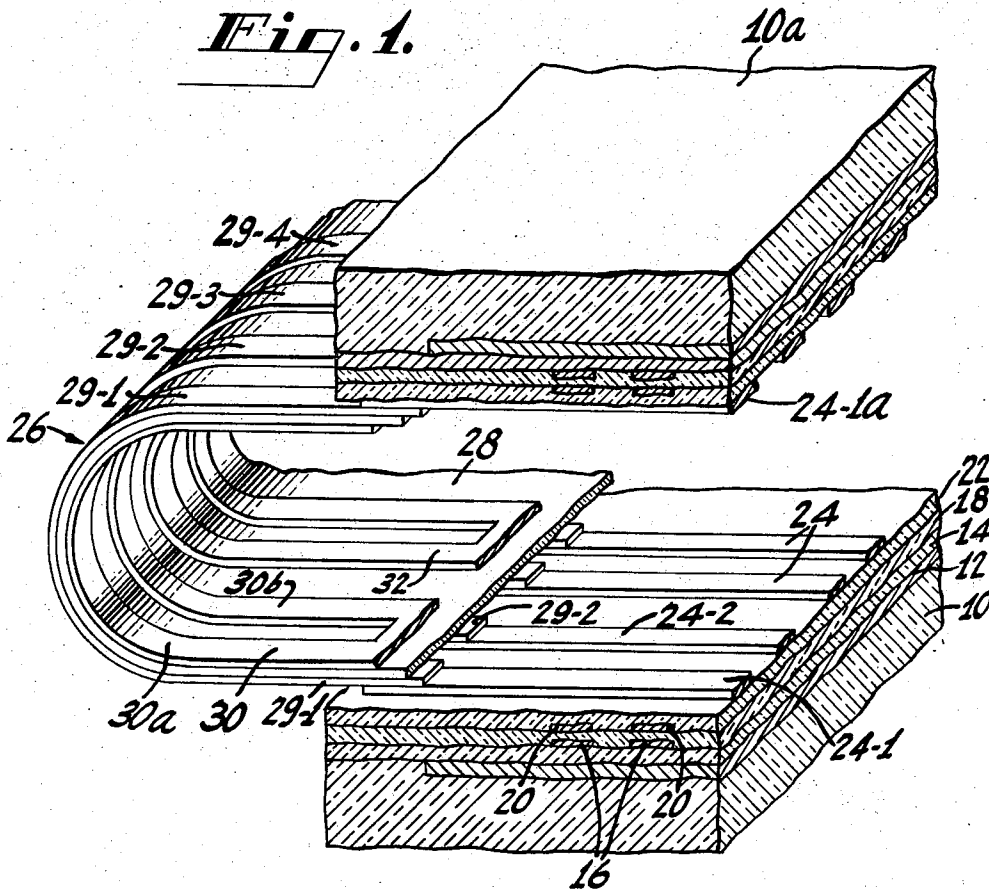


Fig. 3.

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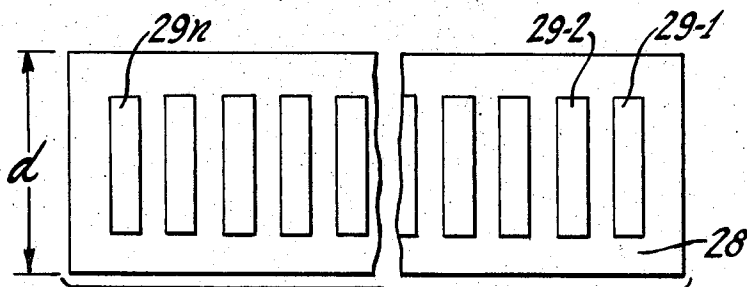


Fig. 2a.

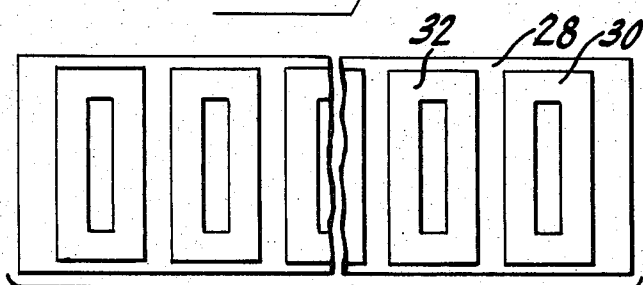


Fig. 2b.

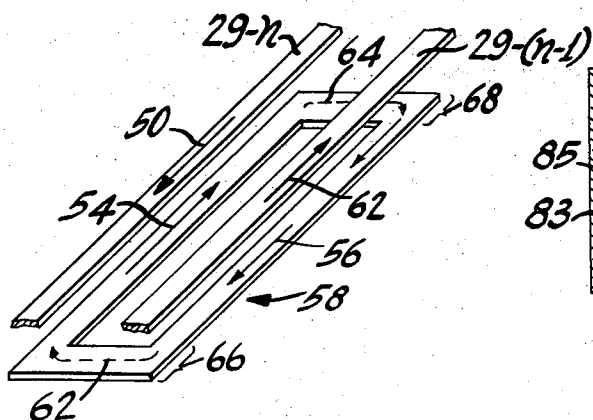


Fig. 5.

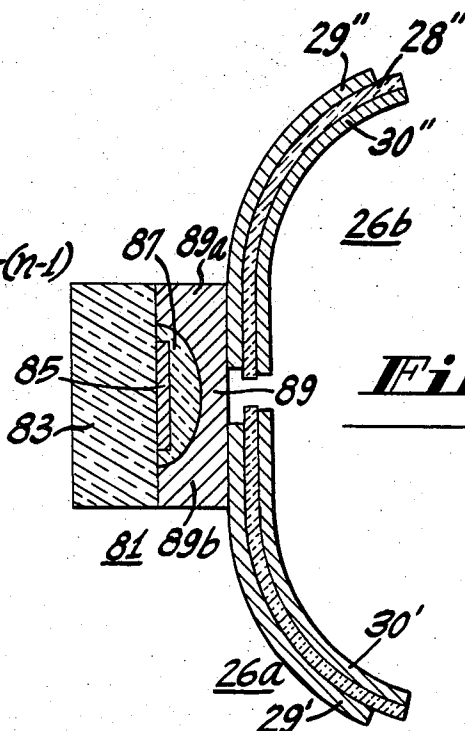


Fig. 6.

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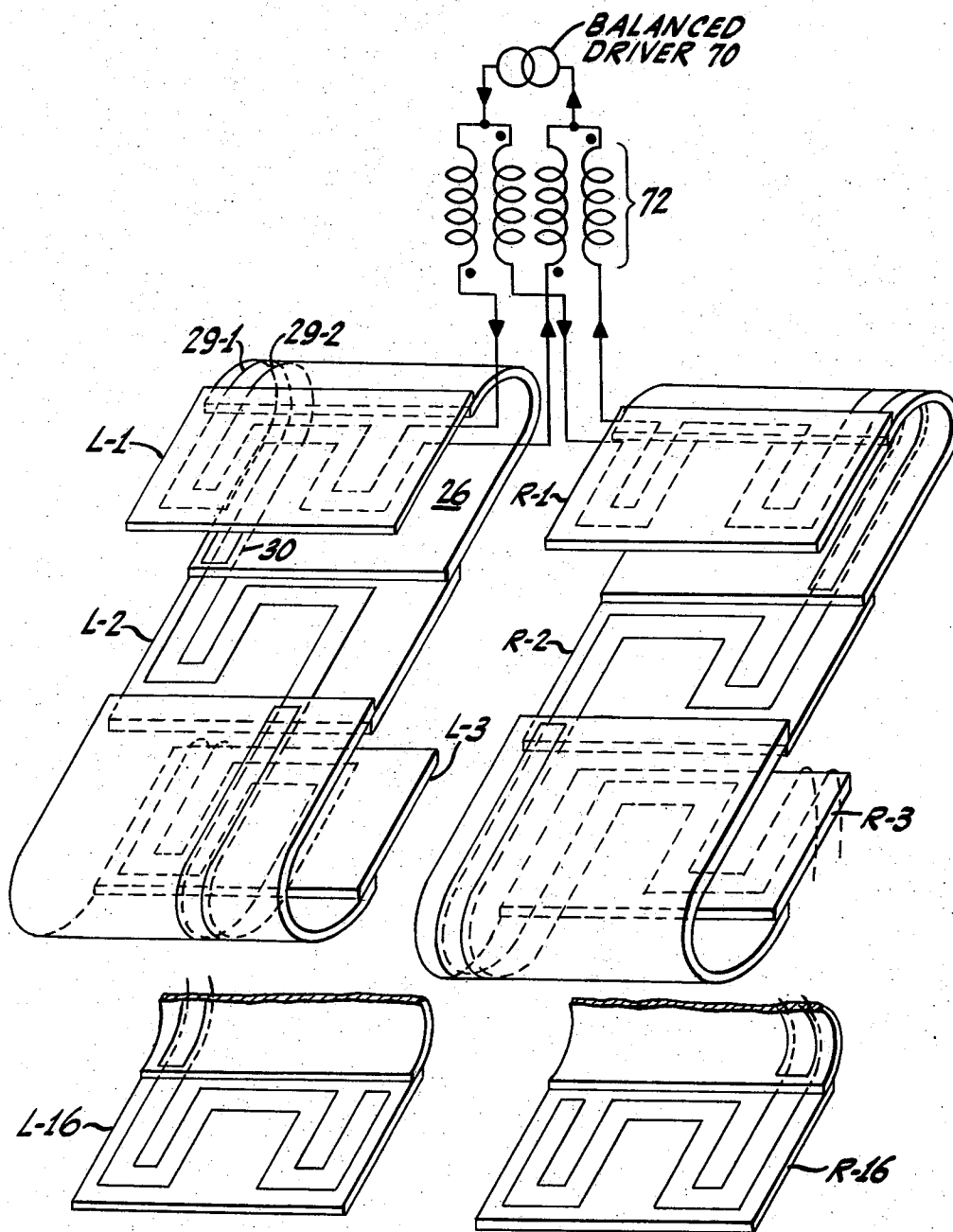


Fig. 4.

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LOW INDUCTANCE INTERCONNECTION OF CRYOELECTRIC MEMORY SYSTEM

BACKGROUND OF THE INVENTION

In the hybrid cryoelectric memory system described in articles by the present inventor, "Taking Cryoelectric Memories out of Cold Storage," *Electronics*, Apr. 17, 1967, p. 111, and "Cryoelectric Hybrid System for Very Large Random Access Memory," *Proceedings of the IEEE*, Oct. 1968, p. 1967, the a lines and also the d (sometimes also known as s) lines are serially connected from plane to plane of a stack of planes. These lines are relatively long and the time delay they introduce is significant compared to the width of the pulses employed to drive the lines. This delay is equal to the line length divided by the velocity with which a signal propagates down the line. It is therefore clear that one way of achieving relatively low memory access and cycle times for a fixed electronics cost is to increase as much as possible the signal propagation velocity.

In many electrical signal transmission systems, the per unit length inductance and capacitance of the transmission line along which the signal propagates is a constant. This is not the case with the cryoelectric memory system dealt with in the present application. Here, the interconnections among the planes of the stack introduce periodic inductance and capacitance discontinuities. One researcher, Dr. A. R. Sass, formerly of RCA Laboratories, has calculated that the propagation velocity v along a line such as an a line of a cryoelectric memory is

$$v = \left\{ \left(L + \frac{L'}{x} \right) \left(c + \frac{c'}{x} \right) \right\}^{-1/2} \quad (1)$$

where

v is the signal propagation velocity

L is the per unit length inductance of an a line over the memory plane

L' is the total inductance of the lines used to connect a lines from one plane to the next adjacent plane

c is the per unit length capacitance of an a line over the memory array

c' is the total capacitance of the lines used to connect the a lines from one plane to the next adjacent plane

x is the total length of the a line over any memory plane.

As a practical matter,

$$c \gg \frac{c'}{x} \quad (2)$$

so that

$$v = \left\{ \left(L + \frac{L'}{x} \right) c \right\}^{-1/2} \quad (3)$$

It is clear from equations (1) and (3) above that if the magnitude of the ratio of interconnecting inductance to memory plane length is comparable to the per unit length inductance of the a strip which lies over the memory plane, the signal propagation velocity will decrease and the cycle time will increase correspondingly. While this problem has been recognized for a considerable period, there has been no practical solution to it up to the present time and the object of this invention is to provide such a solution.

SUMMARY OF THE INVENTION

The connector of the invention comprises a length of flexible insulating material having $2n$ parallel conductors and including also a magnetic field shield insulated from the conductors. The magnetic field shield comprises n discrete sections, each registering with, that is, lying under (or over) a pair of adjacent conductors.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a broken-away perspective view of portions of two memory planes and a portion of a connector according to one form of the invention joining the two planes;

FIGS. 2a and 2b are top and bottom views, respectively, of the connector of FIG. 1;

FIG. 3 is a cross section taken at an edge of a memory plane showing how the connector is joined to the plane;

FIG. 4 is an exploded schematic showing of two stacks of memory planes with the planes of each stack interconnected in accordance with the present invention;

FIG. 5 is a perspective showing to help explain how the interconnection means of the invention achieves a reduction of interconnection inductance; and

FIG. 6 is a cross section through a modified form of connecting structure according to the invention.

DETAILED DESCRIPTION

The memory system to be described is operated at a low temperature such as that of the order of liquid helium temperature. As the means for achieving such an environment is now well understood in the art, it is not illustrated or discussed further.

Two memory planes of a stack of such planes are shown, in part, in FIG. 1. Details of the planes are given in the articles mentioned above and in a copending application by the present inventor and Peter Hsieh, application Ser. No. 736,341 for "Line Terminating Circuits," filed June 12, 1968. In brief, each memory plane comprises a glass substrate 10 on which a lead ground plane 12 is formed. A layer of insulation 14, such as one formed of silicon monoxide, is over the ground plane and the sense lines s , two of which are shown at 16, are located over this layer. The next layer 18 is also insulation and there are additional lines, b lines, two of which are shown at 20 on this insulation layer. The final insulation layer is 22 and the a lines 24 are present on this layer. The sequence of the a , b lines is somewhat arbitrary, and the order shown in FIG. 1 is chosen for reasons of clarity. In addition, the b lines 20 are at all times orthogonal to the s lines; they appear as shown, however, for reasons of clarity.

The interconnection structure of the present invention is shown generally at 26. It comprises a length of flexible insulating material 28 such as Mylar or Kapton. Mylar is a trade name for a polyethylene terephthalate insulating film and Kapton is a trade name for a polyimide insulating film. Both names are trademarks of Dupont and both products are commercially available. Parallel conductors, four of which, 29-1, 29-2, 29-3 and 29-4 are shown, are located on one surface of the insulating material 28. A magnetic field shield comprising discrete conductive sections, two of which are shown in part at 30 and 32, are shown located on the opposite surface of the insulation material 28. However, they may also be located on the same side of 28, provided, of course, that the shield sections are insulated from the conductors. Each shield section is insulated from the adjacent section and is of the shape of an elongated 0 that is, it is formed with a central opening. The longer legs, such as 30a and 30b, of each shield section, register with, that is, they lie directly beneath the corresponding conductors 29-1 and 29-2 on the opposite surface of the insulating member 28. The conductors and shield are formed of a superconductor such as lead.

The parallel conductors 29 are connected at one end to the a conductors on one plane and are shown connected at the opposite end to the a conductors on the immediately adjacent plane. For example, conductor 29-1 is connected at one end to the a conductor 24-1 and is connected at its opposite end to the corresponding end of the a conductor 24-1a, only the end of which is visible on the next adjacent plane 10a. Note that the adjacent plane may be replaced with a terminal bar which may serve as a convenient disconnect interface between two adjacent memory planes, the ends of which both connect to opposite sides of the terminal bar; the key requirement here is that the conductors and shield of the terminal bar appear as that of a memory plane to the flexible interconnecting structure.

The connecting structure is shown more clearly in FIGS. 2a and 2b. The parallel conductive strips 29-1, 29-2... 29- n on one surface are shown in FIG. 2a. The shielding means comprising sections 30, 32 and so on, on the opposite surface of the insulating material 28, are shown in FIG. 2b.

The more detailed showing of how the connection is made appears in FIG. 3. The a line 24-1 is located, for the major portion of its extent, over the ground plane 12. However, the end of each a line is terminated in a terminal 40 which is known as a "land." This land 40 is fabricated by depositing a metal layer each time a metal layer is deposited during fabrication of the memory array. For example, when the lead ground plane 12 is laid down, the lead region 40a of the land is deposited. When the next metal layer, namely the s lines 16 of FIG. 1 are laid down, the region 40b of the layer is deposited. This region is made of tin, just as are the s lines. During the chemical etching which takes place after each deposition, region 40 (40a40b and so on) is protected by a polymerized photoresist so that it is not removed by the etching chemicals. In this manner the land 40 is built up in successive layers to form a sturdy columnar structure solidly secured to the glass substrate 10 and capable of being soldered to.

The interconnecting structure 26 is shown only in part in FIG. 3. The conductor 29-1 is soldered to the land 40, as shown. The conductive shield section 30 preferably extends over the ground plane 12.

In the operation of the memory, care is taken to insure that current flows in one a line at the same time that current of an equal amount flows in the opposite direction in the next adjacent a line. One way this can be done is discussed in the copending application mentioned above. As a result, the same currents flow in opposite directions in two adjacent strips such as 29- n and 29-($n-1$) as shown in FIG. 5. For purposes of clarity of illustration, the insulating material 28 is not shown in FIG. 5 and the strips and shield are shown to be flat rather than curved.

In response to the two drive current waves which propagate in the conductive strips 29 in the directions indicated by arrows 50 and 52 in FIG. 5, corresponding image currents, indicated by arrows 54 and 56, flow in the shield section 58. These image currents flow substantially entirely on the side of the shield section 58 facing the conductors 29 thereby providing a magnetic field distribution which corresponds to a minimum in the free energy of the structure. The return paths for these image currents are relatively very short and are indicated by the dashed arrows 62 and 64. For example, the conductors 29 may be 2 mils in width and spaced 2 mils apart so that each return path is only 2 mils in length. Except for these return paths, the shield section 58 acts as a perfect magnetic field shield for the magnetic energy of the conductors 29 and since these conductors are much longer (of the order of 500 to 1,000 mils) than the spacing between the conductors, the inductance they exhibit is extremely low. It should be recalled here that a current-carrying conductor whose magnetic field is completely shielded exhibits an extremely low inductance.

While not essential, it is preferable that the end regions 66 and 68 of the shield sections be located over the ground planes of the respective memory planes as is illustrated in FIG. 3. The reason is to provide additional magnetic field shielding for even these very small image return paths.

The use of discrete shielding sections for the interconnection member 26 rather than a continuous shield has a number of important advantages. From an electrical viewpoint, each conductive strip 29 has substantially the same value of inductance, regardless of its location. This is true even if there is some shifting of the mask used to lay down the pattern of FIG. 2b relative to that of FIG. 2a so that the conductors 29 do not precisely register with the legs of O-shaped shields. In this case, the inductance may be slightly higher than in the ideal case in which there is full registration of conductors with the legs of the O's, but it does not change from location-to-location. In contrast, if a continuous magnetic field shield were employed for the interconnection member, there would be edge effects. The conductors close to the edges of the member would exhibit a somewhat different value of inductance than the conductors at the center of the member. This would be disadvantageous as it would mean that the propagation velocity of the memory drive currents would be "address de-

pendent," that is, the time required to access one memory location could be different than that required to access another memory location, especially since the effect would be cumulative over many planes.

It has also been found that the sectioned magnetic field shield, as shown, has an important mechanical advantage over the use of a continuous shield. The latter is unduly stressed when cycled between room temperature and liquid helium temperature and this stress can result in crazing, cracking and/or other damage to the interconnection member. The use of discrete, spaced shielding sections prevents this from occurring.

A memory system including the invention is illustrated schematically in FIG. 4. Only two of the hundreds or thousands of a drive lines are shown. Further, while for purposes of illustration, the planes are shown relatively widely spaced from one another, in practice they lie adjacent to one another. The space between the planes is determined by packaging constraints and may be of the order of 250 to 500 mils.

The planes may be arranged in two groups of 16 planes each. The balanced driver 70 supplies current to and draws current from the two sets of planes through the baluns 72 to insure that equal and opposite current waves propagate along the two lines on each plane. The operation of one form of balanced driver (shown in FIG. 4) is discussed in detail in the copending application mentioned above. Terminating resistors are not shown for reasons of clarity and it is to be understood that many other driving arrangements are possible for obtaining drive currents such as discussed herein. Each pair of adjacent planes is connected by an interconnection element such as described in detail above. Each pair of adjacent planes face in opposite directions. For example, the a lines on plane L-1 are shown facing downwardly as viewed in FIG. 4, whereas the a lines on plane L-2 are shown facing upwardly as viewed in FIG. 4. The a lines on the plane L-3 face downwardly, whereas the a lines on the plane L-2 face upwardly, and so on. FIG. 6 shows the arrangement mentioned briefly above employing a terminal bar 81. The bar may comprise a length of glass 83 on which is deposited a sectioned or even a continuous ground plane 85. Insulation 87 is located over the ground plane and a plurality of parallel conductors one of which is shown at 89, are located over the insulation. The ends of each conductor are terminated by a land, two such lands, these for the conductor 89 are shown at 89a and 89b. The ground plane 85 and the parallel conductors 89 are preferably formed of superconductive material such as lead.

The terminal bar 81 acts just like a memory plane from an electrical viewpoint, although its only function is to join the two connectors 26a and 26b. The conductors 29' connect at one end to the conductors 24 (not shown) of one memory plane and connect at their other end to the respective lands such as 89b of the parallel conductors of the terminal bar. The shield elements, one of which is shown at 30', are identical to the shield elements already discussed and preferably extend over the ground plane 85 of the terminal bar at one end and over the ground plane (not shown) of the memory plane (not shown) at their other end. The connector 26b is connected between the terminal bar 83 and a second memory plane similarly to the connector 26a.

We claim:

1. An interconnection element for the conductive strips on two memory planes comprising, in combination:
 - a strip of flexible insulating material;
 - $2n$ spaced, parallel conductors on said strip; and
 - n discrete, spaced magnetic field shielding elements also on said strip and insulated from said conductors, each shielding element registering with exactly one pair of adjacent conductors and insulated from the other shielding elements, where n is an integer greater than 1.
2. An interconnection element as set forth in claim 1, wherein each shielding element is of O-shape and is formed with a central opening lying beneath the space between the two conductors registered with said shielding element.

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3. An interconnection element as set forth in claim 1, wherein said shielding elements and conductors are formed of superconductive material.

4. An interconnection element as set forth in claim 2, wherein said shielding elements and conductors are formed of superconductive material.

5. An interconnection element as set forth in claim 1, wherein the spaced parallel conductors are on one surface of the strip of insulating material and the magnetic field shielding elements are on the opposite surface.

6. In combination:

two superconductor memory planes stacked one over the other and facing in opposite directions, each having at one surface thereof conductors terminated at an edge of the plane by lands; and

an interconnection element for electrically connecting the two planes, said element comprising:

a length of flexible insulating material;

a plurality, equal in number to the number of lands on a plane, of parallel superconductive strips, each joined at one end to a land on one plane and at the other end to a land on the other plane, said strips being located on one surface of said insulating material; and

a plurality of shielding elements, insulated from one another, equal to half the number of lands on a plane, said shielding elements lying on the opposite surface of said insulating material and each shielding element lying beneath a pair of adjacent superconductive strips.

7. In the combination set forth in claim 6, each shielding element being in the shape of an elongated O, one element of the O being of the same width as and lying immediately under one strip and another element of the O being of the same

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width as and lying under an adjacent strip.

8. In the combination set forth in claim 7, each memory plane having a ground plane and the lands on each plane extending beyond the ground plane, and each end of each elongated O-shaped shielding element lying over and insulated from a ground plane.

9. In combination:

two superconductor memory planes stacked one over the other and facing in opposite directions, each having at one surface thereof conductors terminated at an edge of the plane by lands;

two interconnection elements for electrically connecting the two planes, each said element comprising:

a length of flexible insulating material;

a plurality, equal in number to the number of lands on a plane, of parallel superconductive strips, said strips being located on one surface of said insulating material; and

a plurality of shielding elements, insulated from one another, equal to half the number of lands on a plane, each such element on the opposite surface of said insulating material and beneath a pair of adjacent superconductor strips; and

a terminal bar comprising an insulator, parallel conductors equal in number to the number of lands on a plane on one surface of the insulator, and a magnetic field shield on the other surface of the insulator, the conductors on the respective interconnection elements being connected at one end to the conductors of the terminal bar and at the other end to the lands of the respective memory planes.

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