Nov. 6, 1962 R. L. WALLACE, JR 3,062,971

NEGATIVE RESISTANCE DIODE BUILDING BLOCK FOR LOGIC CIRCUITRY

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FIG. 1

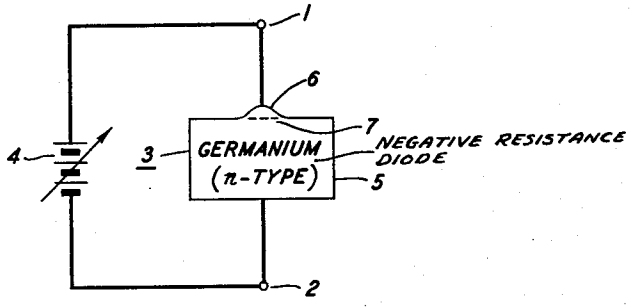

FIG. 2

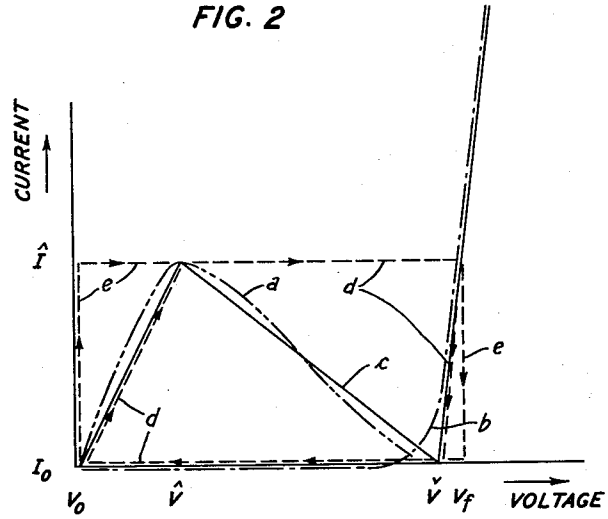

FIG. 3

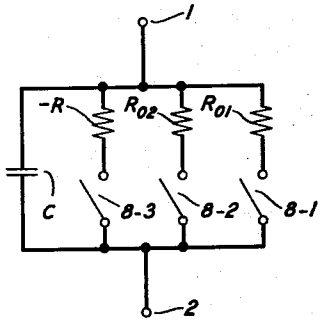

FIG. 4

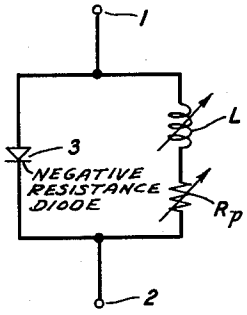

FIG. 5A

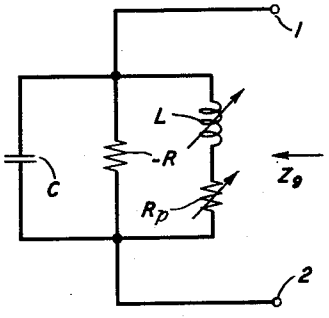

FIG. 5B

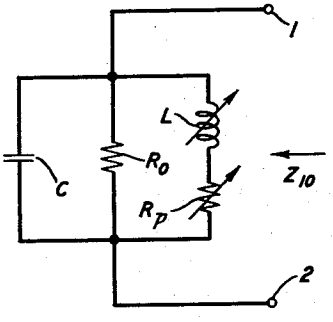

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FIG. 6

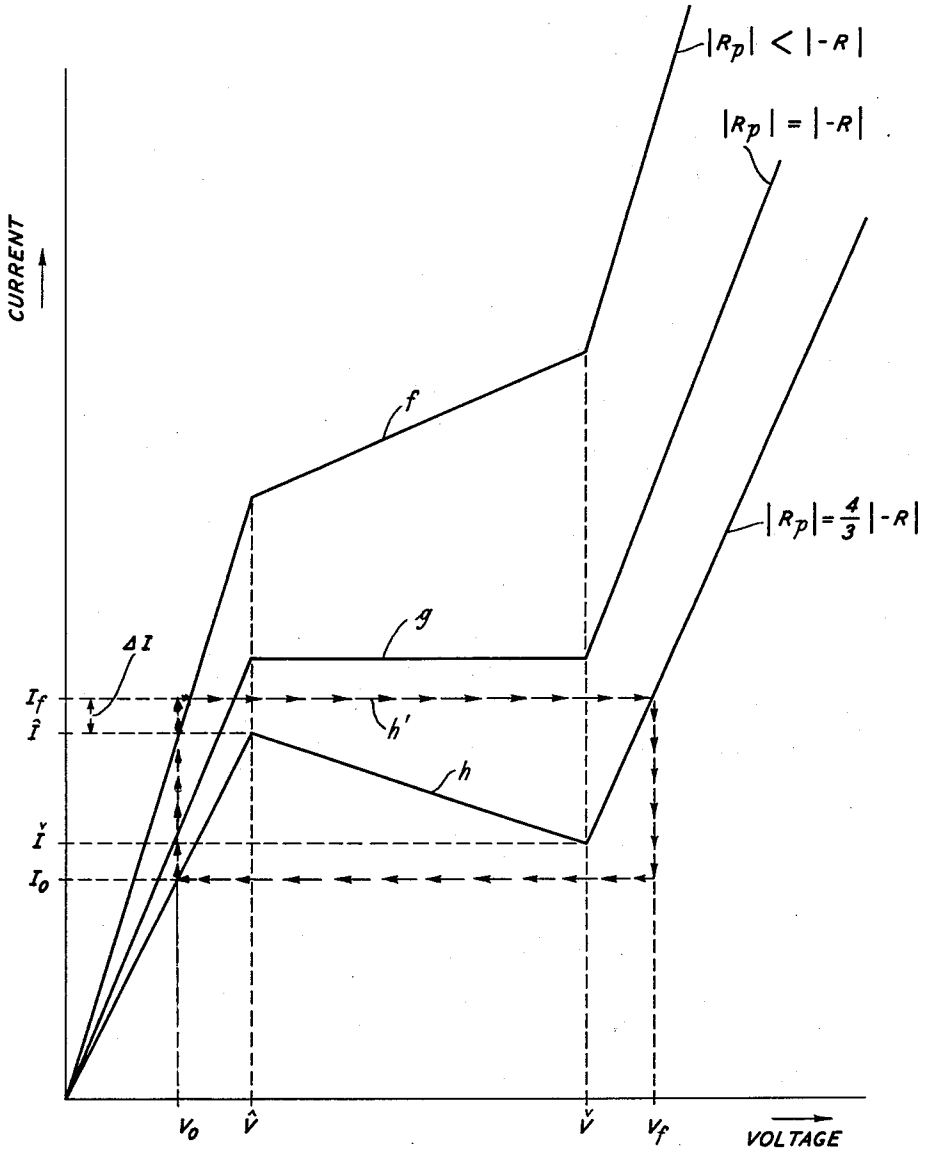

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FIG. 7A

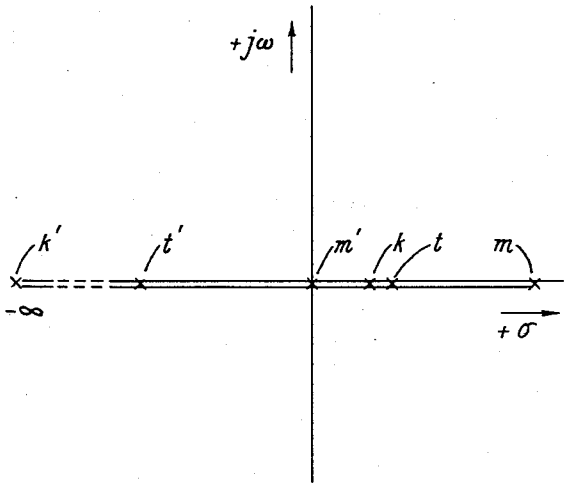

FIG. 7B

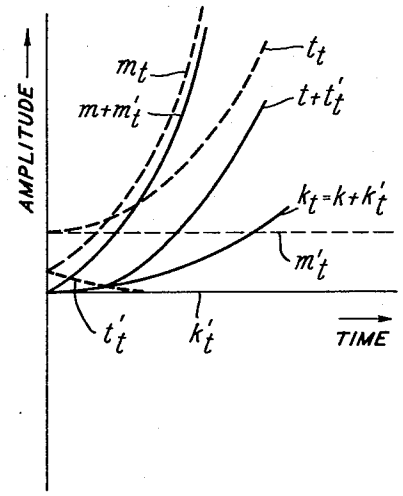

FIG. 7C

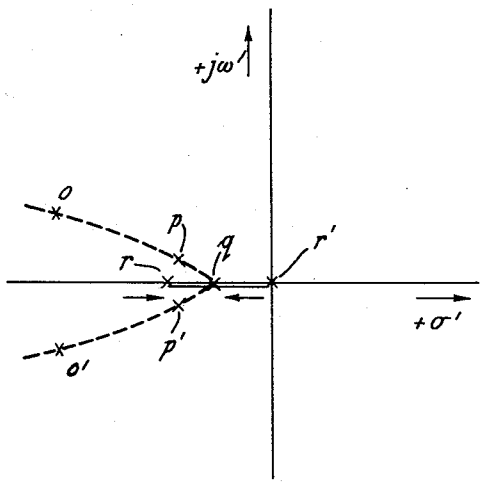

FIG. 7D

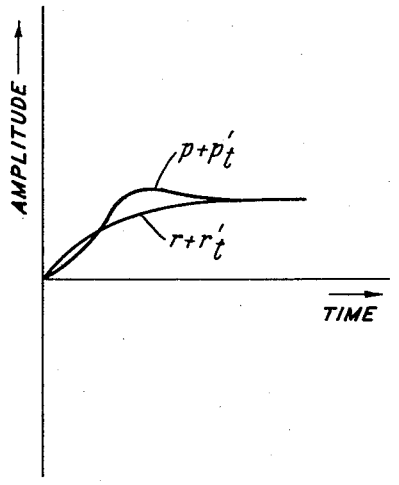

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FIG. 8A

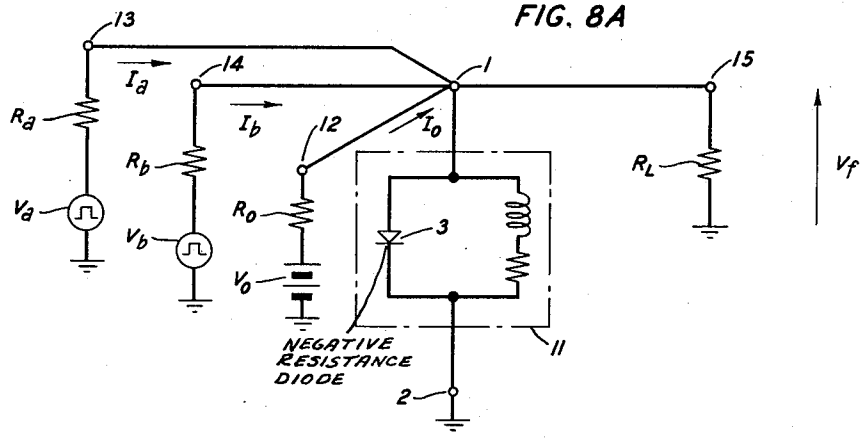
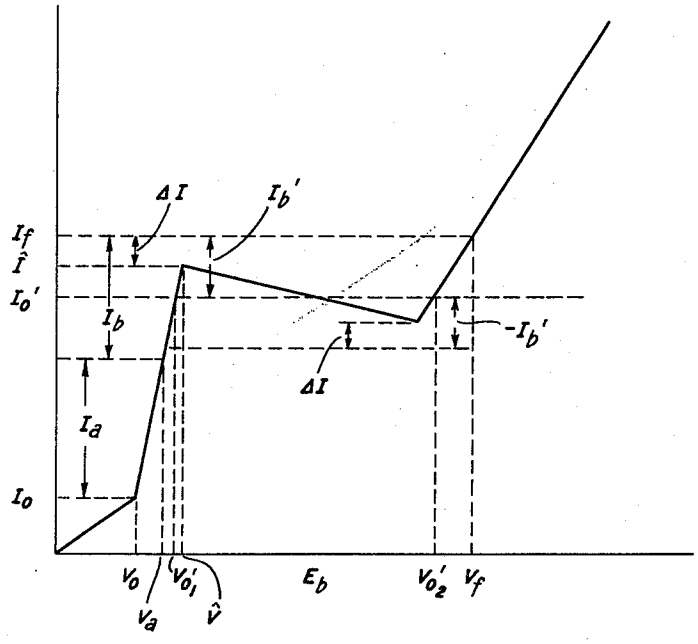


FIG. 8B



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NEGATIVE RESISTANCE DIODE BUILDING BLOCK FOR LOGIC CIRCUITRY

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FIG. 9A

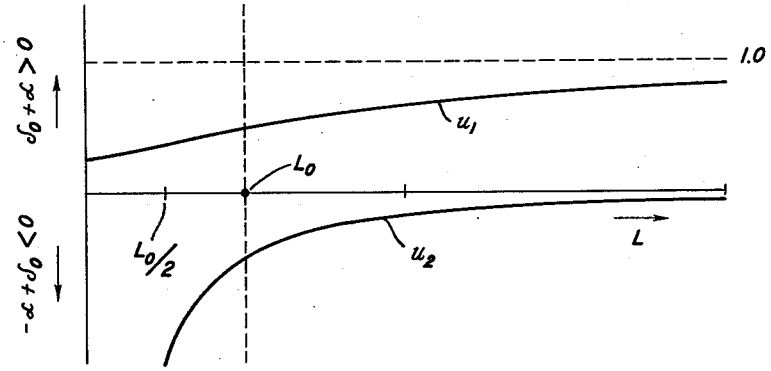

FIG. 9B

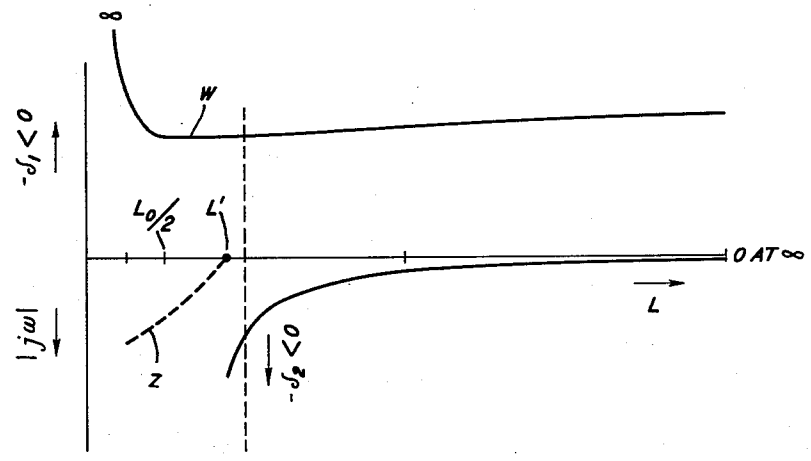

FIG. 9C

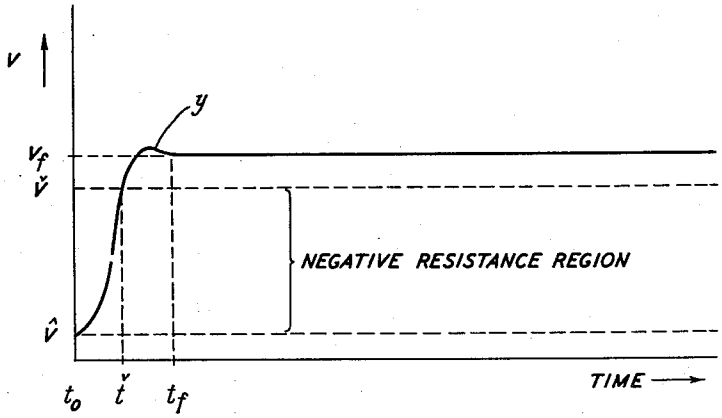

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FIG. 10

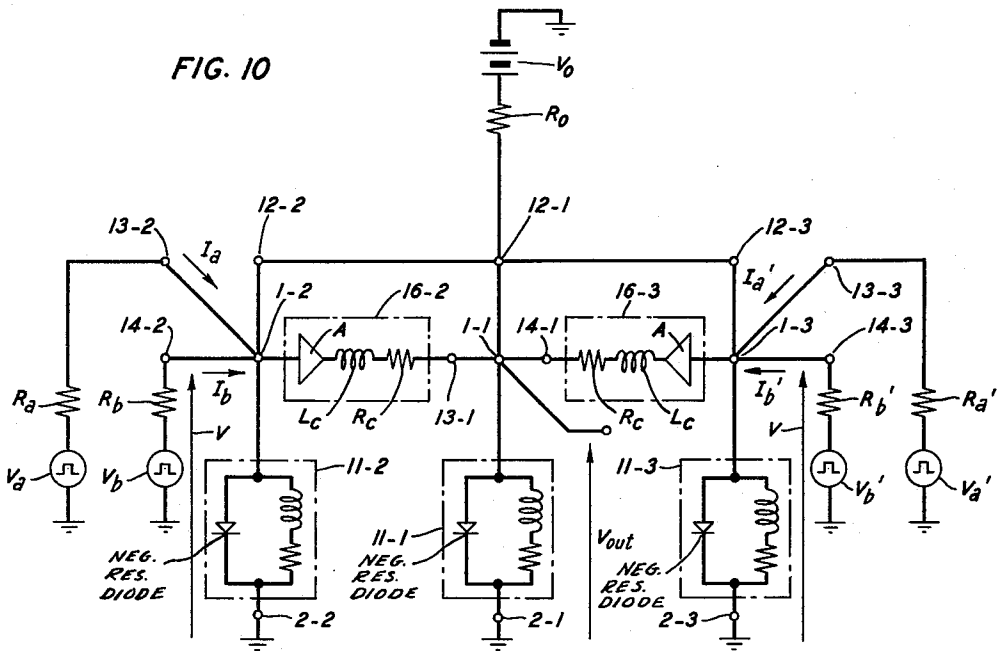
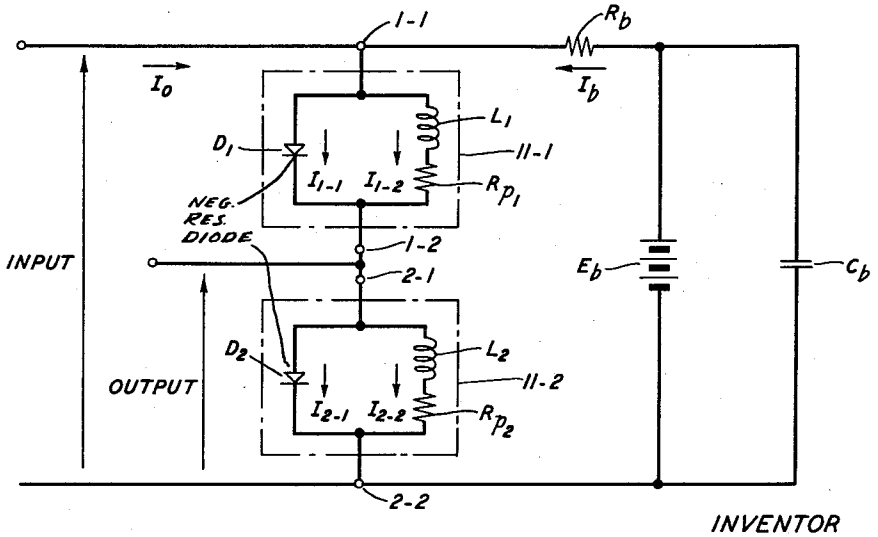


FIG. 11



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NEGATIVE RESISTANCE DIODE BUILDING BLOCK FOR LOGIC CIRCUITRY

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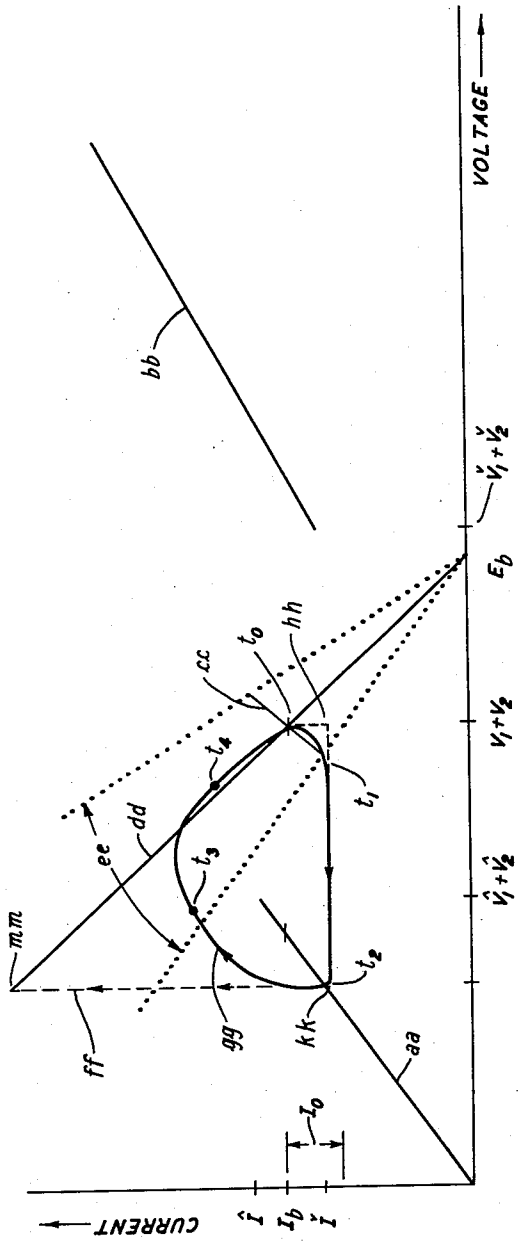

FIG. 12A

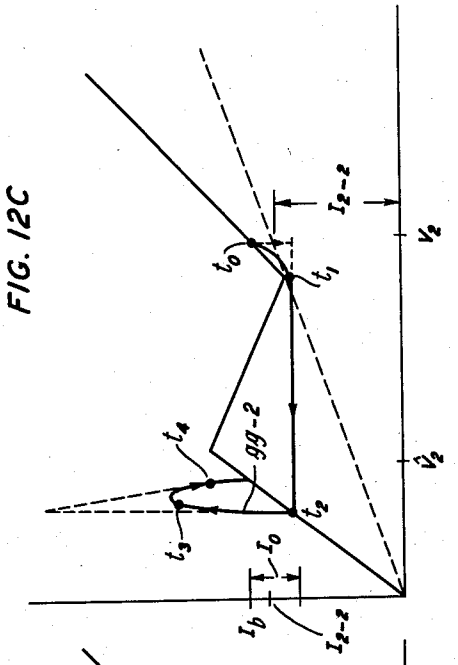

FIG. 12C

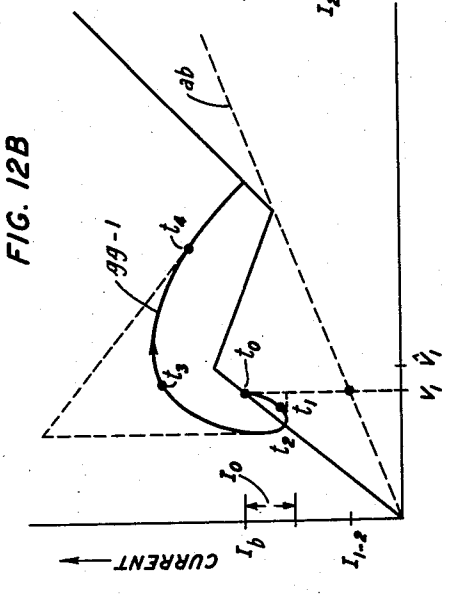

FIG. 12B

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FIG. 13

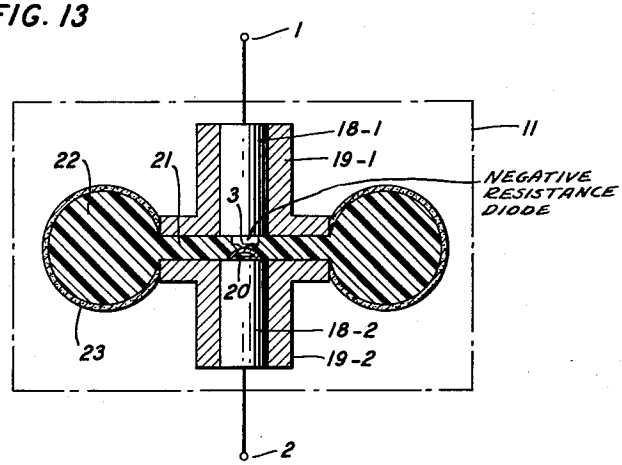
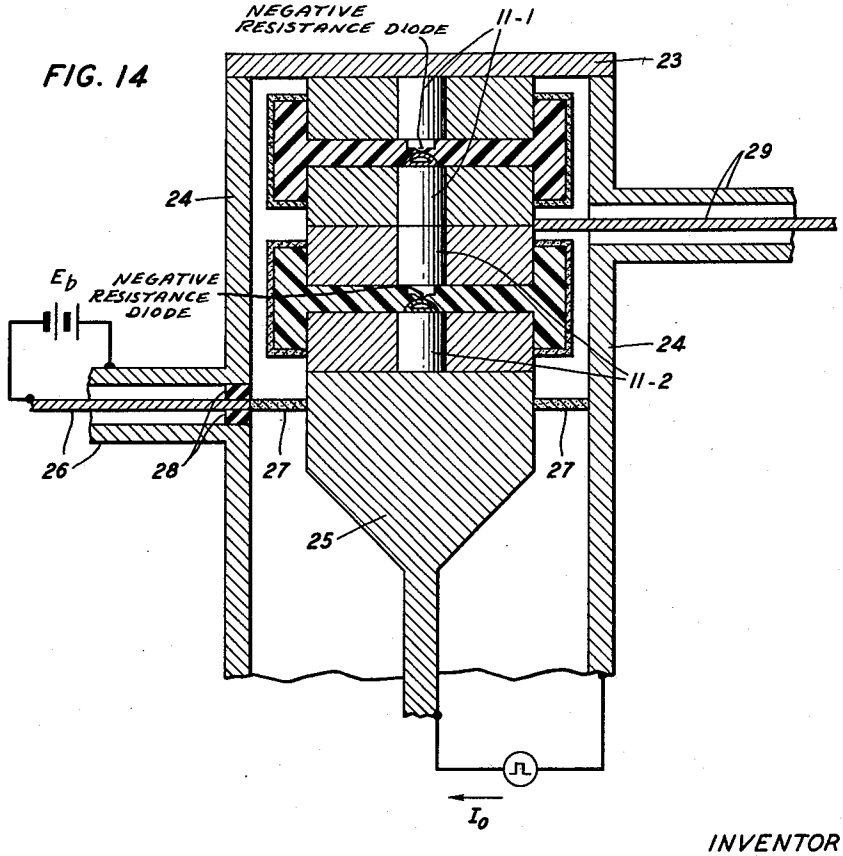


FIG. 14



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United States Patent Office

3,062,971

Patented Nov. 6, 1962

3,062,971

NEGATIVE RESISTANCE DIODE BUILDING BLOCK FOR LOGIC CIRCUITRY

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Filed Oct. 8, 1959, Ser. No. 845,274
21 Claims. (Cl. 307—88.5)

This invention relates to a building block for a widespread variety of circuit configurations and has for its general object the simplification of circuit design.

A further object of the invention is to facilitate the construction of ultrahigh frequency devices by realizing the building block in the form of a compact integral unit. Such a unit allows ease of replacement and minimizes space and power requirements. It is advantageously employed in miniaturized digital apparatus such as computers.

A still further object is to increase the capability and utility of bistable and gating circuits by the novel interconnection of two or more building blocks.

The building block of the present invention is characterized by having only two external terminals between which are only three elements: a negative resistance, voltage-controlled crystal diode, an inductance element and a resistor. The diode which is the central element of the building block has a current-voltage characteristic with three regions. In the first, which exhibits a positive resistance, an increase in voltage from zero is accompanied by an increase in current until a current maximum is reached. Then the characteristic enters its negative resistance portion so that a further increase in voltage is accompanied by a decrease in current until a current minimum is reached. At the latter point, the characteristic turns upward and thereafter, for further increase in the voltage, continuously displays a positive resistance. While a single value of current may have multiple voltages identified with it, there is but one current for a specified voltage so that the characteristic is said to be voltage-controlled.

A typical and appropriate diode for the building block is composed of two semiconducting materials with a narrow junction between them. Impurities are added to "dope" the materials in such a way as to produce a unique voltage-controlled negative resistance characteristic. The theory of the diode is more fully explained in a report of Leo Esaki in the Physical Review, 1958, vol. 109, page 603. The narrow junction which makes possible the negative resistance at high frequencies has associated with it a relatively high capacitance. Nevertheless, the high frequency limit of the diode is not solely a function of the capacitance. It is dependent on the negative resistance-capacitance product which may be controlled by proper "doping." Switching speeds manyfold higher than formerly possible with negative resistance devices are now attainable.

The integral unit of the invention is produced by placing a negative resistance diode of the voltage-controlled type in parallel with the series combination of an inductance element and a resistive element. The magnitudes of the resistive and inductive elements depend upon the particular use to which the block is put and are discussed in detail below in conjunction with the novel embodiments proposed.

For low frequency operation the building block is made up of lumped circuit elements. At ultrahigh frequencies it is a composite structure. In one type a resinous material is placed between two holders which serve as a mount for a semiconductor diode. As the holders are brought physically close together, the resin is extruded from between them to form at their outer

edges a disk-like solid of revolution. The series combination of distributed resistance and inductance results from depositing on the surface of the solid of revolution a resistive layer which encircles the holders at the level of the gap between them. The inductance may be altered by adjusting the geometry of the surface, or by changing the composition of the resin. It may be made variable by including magnetically polarizable ferrite elements within the resinous solids formed.

The manner in which the invention accomplishes the above-mentioned objects can be more clearly apprehended from a consideration of the descriptions of a few preferred embodiments which are to be considered in conjunction with the drawings, in which:

FIG. 1 is a diagram of a typical negative resistance, voltage-controlled diode which is a central constituent of the present invention;

FIG. 2 is a set of curves portraying actual and idealized characteristics for the diode of FIG. 1;

FIG. 3 is an "equivalent" circuit diagram for explaining the operation of the diode of FIG. 1;

FIG. 4 is a schematic circuit diagram of the building block of the invention;

FIG. 5*a* is an idealized equivalent circuit diagram for the building block operated in its negative resistance condition;

FIG. 5*b* is an idealized equivalent circuit diagram for the building block operated in its positive resistance condition;

FIG. 6 is a set of curves illustrating the way in which the direct current characteristics of the building block are affected by changes in padding resistor magnitude;

FIG. 7*a* is a complex frequency domain for the building block operated in its negative resistance condition and is used in explaining the functioning of the invention;

FIG. 7*b* is the time domain corresponding to the complex frequency domain of FIG. 7*a*;

FIG. 7*c* is a complex frequency domain for the building block operated in its positive resistance condition and is used in explaining the functioning of the invention;

FIG. 7*d* is the time domain corresponding to the complex frequency domain of FIG. 7*c*;

FIG. 8*a* is a symbolic representation of a circuit embodying the invention, e.g., a bistable circuit or an AND gate;

FIG. 8*b* is a characteristic curve for the bistable or AND gate circuit of FIG. 8*a*;

FIG. 9*a* is a set of curves demonstrating the effect on pole location in the complex frequency domain of changes in inductance when the AND gate circuit of FIG. 8*a* is operated in its negative resistance condition;

FIG. 9*b* is a set of curves demonstrating the effect on pole location in the complex frequency domain for changes in inductance when the AND gate circuit of FIG. 8*a* is operated in its positive resistance condition;

FIG. 9*c* is a time response curve of the AND gate of FIG. 8*a* for typical parameters;

FIG. 10 is a symbolic representation of a circuit comprising a chain of two driving building blocks, each separately interconnected with a driven building block by a coupling impedance;

FIG. 11 is a schematic diagram of a bistable circuit formed by serially connecting two building blocks of the invention;

FIG. 12*a* is a composite characteristic curve for two serially connected building blocks illustrating the operation of the circuit of FIG. 11;

FIGS. 12*b* and 12*c* are characteristic curves for individual building blocks constituting the bistable circuit of FIG. 11;

FIG. 13 is a cross sectional view of a microwave embodiment of the building block of FIG. 4; and

FIG. 14 is a cross sectional view of a microwave embodiment of the bistable circuit of FIG. 11.

The invention may be best understood by beginning with a consideration of the voltage-controlled negative resistance diode around which the building block is formed.

The illustrative diode **3** of FIG. 1 is biased in its forward direction by a battery **4**, connected across terminals **1** and **2**, so that a wafer **5** of n-type germanium semiconductor is at a negative potential with respect to a "mesa" **6** of deposited metal. In the alloying process used to create the special characteristics of the diode a narrow p-n junction **7** is formed between the mesa **6** and the body **5** of the wafer. The battery **4** which supplies the voltage bias may be varied to obtain the characteristic curves of FIG. 2.

Referring to FIG. 2, there are two components constituting the current flowing in the forward direction. The first component, *a* of FIG. 2, is jointly attributable in part to the high field intensity associated with narrow p-n junctions and the high concentration of diode impurity atoms. It is produced by the seemingly anomalous penetration of the high energy barrier at the junction by lower energy carriers. Quantum mechanics teaches that there is always a calculable probability of finding such behavior within a restricted voltage interval. The narrower the diode junction, and the greater its impurity concentration, the higher is the probability of barrier penetration. Quantum mechanical phenomena are small scale, and there is a low critical voltage $\hat{V}$ (the symbol is chosen to indicate the presence of a peak in the current-voltage characteristic) beyond which this current component decreases with an increase in voltage so that there is a negative resistance between $\hat{V}$ and a voltage minimum $\check{V}$. Quantum mechanical operations take place at the maximum rate predicted by the theory of relativity, and are not limited by the slow transit times of conventional charge carriers. Now possible are devices which function in a fraction of the time formerly required for switching. The second component *b* begins to have an appreciable magnitude where the quantum mechanical current becomes negligible. It is of the typical "injection" variety and has an exponentially increasing curve. It is subject to transit time restrictions. Summation of the currents *a* and *b* gives a composite current *c* whose idealized N-shaped characteristic starts at the current-voltage origin V_o, I_o, reaches a maximum $\hat{V}$, $\hat{I}$, turns downward to a minimum $\check{V}$, I_o, and thereafter rises continuously with increasing voltage. The magnitude of the positive resistance between points V_o, I_o, and $\hat{V}$, $\hat{I}$, is the reciprocal of the slope of the line segment between them. Other resistive magnitudes are similarly calculated. The shape of the N and the points of maximum and minimum current may be adjusted by controlled doping of the diode materials.

The idealized characteristic *c* allows constructing the equivalent circuit of FIG. 3 for piece-wise linear analysis. Between break points where the slope of the characteristic *c* in FIG. 2 abruptly changes, linear equations apply. Switches **8–1**, **8–2** and **8–3**, respectively, control positive resistor R_{01}, positive resistor R_{02}, and negative resistor $-R$. In addition the condenser C represents the self-capacitance of the diode **3** in FIG. 1 to account for the A.-C. behavior of the diode in contrast with its D.-C. behavior. If the strength of the current source **4** between terminals **1** and **2** of diode **3** in FIG. 1 is gradually increased from zero, the locus of operation in FIG. 2 begins at V_o and follows a portion of the closed path *d* until $\hat{V}$ is reached, always remaining on the D.-C. operating curve. At $\hat{V}$ a slight increase in current requires a transition in voltage from V to V_f. Empirically, it is known that the transition does not occur instantaneously as it would in a purely resistive circuit, rather a finite time interval is required during which capacitor

C is being charged. At $\check{V}$ the entire current $\hat{I}$ flows into $-R$, and none of it goes into C. The situation is reversed at V where none of the current I flows into $-R$ and all of it goes into C. The rate at which the transition takes place depends on the magnitude of the current I_c flowing into C according to the well-known relation:

$$\frac{dV}{dt}=\frac{I_c}{C} \tag{1}$$

where

I_c=the difference between current of the characteristic *c* and that of locus *d*,

$\frac{dV}{dt}$=the rate of change of voltage with respect to time, and

C=capacitance of the condenser.

It is apparent that the voltage changes at its maximum rate at $\check{V}$.

More common than the gradual increase in current along locus *d* in FIG. 2 is the abrupt change in driving current from I_0 to $\hat{I}$ occasioned by a pulse or unit step. The locus of operation follows path *e* of FIG. 2. Initially, the entire current flows into condenser C causing it to charge rapidly. Thereafter C charges at a decreasing rate, becoming zero at V. The remainder of the operation parallels that previously described. Should the driving current be suddenly removed, or the pulse have terminated at V_f, $\hat{I}$ drops to I_0 and C discharges until V_o is reached.

The building block which lies at the root of the present invention is constructed as shown in FIG. 4. Diode **3** of FIG. 1 is shunted across its terminals **1** and **2** by the series combination of a padding resistor R_p and an inductor L.

If the magnitude of R_{01} in FIG. 3 equals that of R_{02}, only two equivalent circuits are needed to completely describe the operation of an idealized building block. When the building block is operated in its negative resistance condition, FIG. 5*a* is pertinent. The characteristic impedance Z_9 appears between terminals **1** and **2** of FIG. 4, and may be written:

$$Z_9=\frac{\frac{s}{C}+\frac{R_p}{LC}}{s^2+\left(\frac{R_p}{L}-\frac{1}{CR}\right)s-\left(\frac{R_p}{LCR}-\frac{1}{LC}\right)} \tag{2}$$

where

C=magnitude of the diode capacitance,
R=magnitude of the diode negative resistance,
R_p=magnitude of padding resistor,
L=magnitude of inductance,

and $s=\sigma+j\omega$ refers to the complex frequency variable. For the building block operated with its positive resistance conditions assumed identical, resistance R_0 is substituted for R_{01} and R_{02} in FIG. 3, and the equivalent circuit of FIG. 5*b* applies. It differs from FIG. 5*a* by the substitution of R_0 for $-R$. The impedance Z_{10} between terminals **1** and **2** of FIG. 4 becomes:

$$Z_{10}=\frac{\frac{s}{C}+\frac{R_p}{LC}}{s^2+\left(\frac{R_p}{L}+\frac{1}{CR_0}\right)s+\left(\frac{R_p}{LCR_0}+\frac{1}{LC}\right)} \tag{3}$$

where R_0=diode positive resistance and other symbols are as for Equation 2. The parameters for Equations 2 and 3 are taken as constants to permit linear analysis. In actuality, capacitor C, for example, changes with increasing voltage, but it does not do so appreciably.

It is apparent that the addition of padding resistor R_p in the schematic circuit diagram of FIG. 4 will alter the idealized direct current characteristic *c* of FIG. 2. In-

ductance L can have no effect because its impedance for any direct current signal is identically zero, but under conditions of transient operation it affects the rate at which the building block changes state. Since resistor R_p is connected in shunt with diode 3 of FIG. 4 the steady voltage appearing at its terminals must always equal that of the diode. Consequently, a composite direct current characteristic for the building block of FIG. 4 may be obtained by adding the currents through resistor R_p and the diode resistor for any given value of voltage. Resultant characteristics for three magnitudes of R_p are plotted in FIG. 6. When the magnitude of R_p is less than that of $-R$, the composite characteristic f nowhere exhibits negative resistance. When the magnitude of R_p is equal to the magnitude of $-R$, as in curve g, the negative resistance region is replaced by a straight line segment parallel with the voltage axis. Theoretically, the transition from low voltage point $\hat{V}$ to high voltage point $\check{V}$ could be made with a signal approaching zero magnitude, but the time for switching would not be optimal. Resistor R_p must be sufficiently large to preserve enough composite negative resistance to give fast switching but it simultaneously must be small enough to allow a change of state with a moderate driving pulse. A satisfactory compromise is depicted in curve h for which the magnitude of R_p is given by $|R_p|=4/3|-R|$. This latter curve may be used to illustrate switching along a locus h' when the quiescent building block current is I_o. A driving pulse, I_f-I_o, would exceed $\hat{I}-I_o$ by an incremental current ΔI, and the locus of changes would be similar to that already described in conjunction with FIG. 2. Starting at quiescent voltage V_o the condenser C begins to charge until $\hat{V}$ is reached and only the incremental current ΔI is flowing through C. Thereafter, the voltage continues to increase along locus h' to terminal voltage V_f, where all of the current divides between diode positive resistor R_0 and building block padding resistor R_p, and C is fully charged.

The information obtainable from FIG. 6 is primarily limited to the direct current effect of padding resistor R_p on the building block of FIG. 4. For the influence of inductor L on the rate at which changes of voltage state take place, reference must be made to the separate domains of FIGS. 7*a* through 7*d* dealing with the operation of the building block in its conditions of positive and negative resistance. In the former condition, so-called poles, designated by x's in the complex frequency domain of FIG. 7*a*, are determined from the roots of Equation 2. The roots are in the form:

$$s=\sigma_0\pm j\omega=\sigma_0\pm j\sqrt{\beta-\sigma_0^2} \tag{4}$$

where

$$\sigma_0=\frac{1}{2}\left(\frac{1}{CR}-\frac{R_p}{L}\right) \tag{5}$$

$$\beta=\frac{1}{LC}\left(1-\frac{R_p}{R}\right) \tag{6}$$

and other symbols are as for Equation 2. Since the magnitude of resistor R_p will always be greater than that of diode resistor $-R$, β in Equation 6 will always be negative so that:

$$s=\sigma_0\pm\sqrt{\sigma_0^2+|\beta|}=\sigma_0\pm\alpha \tag{7}$$

where $|\beta|$ is the magnitude of β in Equation 6. Consequently, there will always be two abscissa positions for each set of circuit parameters. The extreme variation resulting from a change in industance L is shown in FIG. 7*a*. On the one hand, for zero industance the poles are k and k'. With increasing industance, k moves in the direction of increasing σ until it reaches the limiting value m where the industance is infinite. Simultaneously, k' moves to m'. The corresponding response to an applied unit step of current is indicated in the time domain of FIG. 7*b*. For zero inductance pole k' produces a decaying exponential k'_t with exponent $(-\alpha+\sigma_0)$ which is summed with the increasing exponential of k_t with exponent $(\alpha+\sigma_0)$ yielding $k+k'_t$ after subtraction of the unit step in keeping with the requirement of zero response at the beginning of the excitation period. A marked improvement in rise time is apparent in curve $m+m'_t$ for pole locations m and m'.

When the building block is operated in its positive resistance condition, the roots of Equation 3 give pole locations which must always lie in the left half of the complex frequency domain in FIG. 7*c*. The roots are in the form:

$$\sigma'_0+j\omega'=\sigma'_0\pm j\sqrt{\beta'-\sigma'^2_0} \tag{8}$$

where σ'_0 and β' are the same as for σ_0 and β except for the replacement of $-R$ by R_0. As inductance L increases, σ'_0 becomes smaller along with $j\omega'$ as demonstrated by the shift from positions o and o' to p and p', the time response for the latter being given by $p+p'_t$ in the time domain of FIG. 7*d*. Further increase in L causes the poles to coalesce at q where $\beta'=\sigma'^2_0$. A still further increase in L produces a migration of split poles in opposite directions along the $-\sigma$-axis until the limiting positions r and r' are reached for infinite inductance. The corresponding response to a unit step of current is $r+r'_t$ in FIG. 7*d*.

The effect of inductance on switching speed is best demonstrated in conjunction with a single building block which performs logic functions. FIG. 8*a* illustrates a building block connected to serve as an AND gate or as a bistable network, depending on parameter selection. For AND gating a summation of input current pulses greater than a predetermined maximum causes the output voltage of the gate to suddenly change from a low to a high magnitude.

In FIG. 8*a* four distinct leads, **12**, **13**, **14** and **15**, are connected to terminal **1** of building block **11**. Terminal **12** allows the application of a biasing current I_o from a voltage source V_o through a resistor R_o of large magnitude. Terminals **13** and **14** are similarly connected to pulsing sources of current I_a and I_b, respectively. Output voltage V_f is measured at terminal **15** across a large resistor R_L, preferably of infinite resistance as would be provided by the input terminals of an isolation amplifier. The magnitude of the biasing source I_o is selected to place the operation of the AND gate at a low voltage operating point V_o, shown at an abrupt change accounting for any increased curvature in the slope of the positive resistance characteristic of FIG. 8*b*. Current sources I_a and I_b are chosen so that when both are activated the total AND gate current will exceed $\hat{I}$ and allow a switching transition to the output voltage V_f. When the activating pulses I_a and I_b terminate, the building block returns to its stable equilibrium at voltage V_o. If only current source I_a is activated the building block will be driven to the point V_a, I_0+I_a on the characteristic of FIG. 8*b*, the voltage being not much greater than V_o, the condition for no input signal. The characteristic for an AND gate should preferably be chosen to have a steep slope between V_o, I_o and $\hat{V}$, $\hat{I}$.

With slight modifications the configuration of FIG. 8*a* demonstrates bistability if the activating current I_a is reduced to zero and bias current I_o is gradually raised to I'_o giving the quiescent output voltage V'_{o1} at terminal **15**. A driving current pulse of I'_b brings about a change of voltage state to V'_{o2} where it remains even after reduction of current I'_b to zero. In similar fashion a negative pulse $-I'_b$ causes a restoration of the original equilibrium voltage V'_{o1}. By making changes in the magnitude of R_0 circuits of varying states of stability may be produced according to well-known techniques.

As has been suggested by the domain diagrams of FIGS. 7*a*–7*d* the rapidity of switching of the AND gate or bistable circuit of FIG. 8*a* is controlled by pole positions which depend on the magnitude of inductor L. When the building block is operated in its negative resistance condition, governed by Equation 7, curve u_1 in FIG.

9*a* for positive poles given by $\sigma=\sigma_0+\alpha$ and curve u_2 for negative poles given by $\sigma=\sigma_0-\alpha$ indicate a pole nitude of the inductor L is made larger. The rate of improvement in switching speed, being related to

$$\frac{1}{\sigma}$$

is most rapid in the interval:

$$L<L_0=CR_pR \tag{9}$$

where symbols are as for Equation 2 and L_o is the inductive magnitude for which $\sigma_0=0$. For the limiting value L_o the second derivative of the reciprocal of switching speed with respect to inductance is substantially zero. Beyond L_o, curves u_1 and u_2 of FIG. 9*a* asymptotically approach a limiting value. By contrast in FIG. 9*b*, for the building block in its positive resistance condition, there are two sets of negative poles in the interval:

$$L>L' \tag{10}$$

where L' equals the inductance for which $\beta'=\sigma'_0{}^2$. In the remainder of the graph there is a single pole with negative component σ_1 of locus *w* accompanied by an imaginary component $j\omega$ whose locus *z* is shown dotted. Evidently, there is little gain in choosing an inductive magnitude for the building block much greater than that of inductance L_0 the second derivative of the reciprocal of switching changes. Furthermore, large inductance is often accompanied by resistance effects making for difficulty in maintaining an optimal padding resistance R_p. For magnitudes of inductance smaller than L_o the decaying transient of the positive resistance region has oscillatory behavior giving a voltage overshoot during switching. Nevertheless, the overshoot is often not troublesome for moderate magnitudes of L, since pole locations near the $-\sigma$-axis, as at *p* and *p'* of FIG. 7*c*, indicate low frequency.

Another factor in the transient buildup is the size of the current pulse. It is a multiplicative coefficient of the exponential terms making up the solution. By way of illustration, the transient response for a building block constructed from typical parameters is given in FIG. 9*c*. The magnitude of L has been taken by reference to FIGS. 9*a* and 9*b* as $\frac{1}{2}L_o$ or in a representative case $2(10^{-10})$ henries. Other parameters are

$$R_0 = 1 \text{ ohm}$$

$$-R=-3 \text{ ohms}$$

$$C=\frac{10^{-10}}{3} \text{ farads}$$

and

$$R_p=4 \text{ ohms}$$

For the purpose of determining the switching pattern of FIG. 9*c* the current of the building block in FIG. 8*a* will be assumed just below $\hat{I}$ in FIG. 8*b* when a switching pulse of ΔI is applied at $t=0$. When $\Delta I=1$ milliampere, the switching voltage begins at $\hat{V}$ in FIG. 9*c* and proceeds through the negative resistance region until it reaches V at *t* after 0.9 millimicrosecond. Had ΔI been as great as 10 milliamperes the elapsed time would have been reduced to 0.3 millimicrosecond. The kind of rising transient involved may be understood by reference to $t+t'_t$ of FIG. 7*b* which is the response for the pole location of the present example. At $\check{V}$ the building block enters its positive resistance condition so that pole locations *p* and *p'* of FIG. 7*c* apply, with time response $p+p'_t$ giving the curve extending between $\check{V}$ and V_f of FIG. 9*c*. There is a slight overshoot *y* attributable to the oscillatory nature of the response. It is only two percent of the over-all response and V_f is reached after an additional 0.2 millimicrosecond for $\Delta I=1$ milliampere, making the total switching time $t_f=1.1$ millimicroseconds. With $\Delta I=10$ milliamperes the total time required to reach V_f is reduced to about 0.45 millimicrosecond. It must be concluded that even the selection of a nonoptimal L allows the building block to change its voltage state during an extremely short time interval if other parameters are chosen according to the restrictions previously considered.

The utility of the single AND gate of FIG. 8*a* may be extended by having other AND gates serve as current sources I_a and I_b. This is illustrated in FIG. 10 where a portion of an AND gate chain has been formed by separately interconnecting driving building blocks **11–2** and **11–3** with a driven building block **11–1** through coupling networks **16–2** and **16–3**. The driven building block **11–1** is recognizable as the AND gate of FIG. 8*a* whose mode of operation has already been discussed. The chain may be extended indefinitely by supplying each driving block at its input current terminals with supplementary driving blocks.

If the coupling network is chosen to be only the coupling resistor R_c, rapid switching is assured if there is a composite negative resistance R' at terminals **1–2** and **1–3**. Assuming that neither driving building block appreciably loads the other, this requires:

$$\frac{1}{R'}=\frac{R_0+R_p}{R_0R_p+R_pR_c+R_cR_0}+\frac{1}{R_p}-\frac{1}{R}<0 \tag{11}$$

or

$$\frac{1}{R}>\frac{R_0+R_p}{R_0R_p+R_pR_c+R_cR_0}+\frac{1}{R_p}$$

or

$$R_c>\frac{RR_p}{R_p-R}-\frac{R_0R_p}{R_0+R_p}$$

where

R'=magnitude of composite negative resistance at terminal **1–2** or **1–3**,

R=magnitude of diode negative resistance of either driving building block,

R_c=coupling resistance of impedance interconnecting driving and driven building blocks,

R_0=positive resistance for building block diode having equal resistive slopes in all positive resistance conditions, and

R_p=padding resistance of each driving building bloc.

Equation 11 is derived by calculating the total current through a driving building block and R_c in terms of the input voltage V.

Should the driving building blocks interact with each other, a second condition accounts for the presence of two coupling impedances feeding the driven building block:

$$R_c>2\left(\frac{RR_p}{R_p-R}\right) \tag{12}$$

where all symbols are as for Equation 11.

Furthermore, if the drives are through voltage sources a composite negative resistance at the input terminals of the driving building blocks is preserved provided:

$$\frac{1}{R_a}+\frac{1}{R_b}+\frac{1}{R_o}<\frac{1}{R'} \tag{13}$$

where

R'=magnitude of composite negative resistance at terminal **1–2** or **1–3**, and

R_a, R_b, R_0=internal resistance of voltage sources V_a, V_b, V_0, respectively.

To minimize the restrictions on parameters imposed by the resistor R_c, an isolating intermediate amplifier A or a coupling inductor L_c may be chosen as the only element of the coupling network in FIG. 10. An amplifier suitable for rapid switching, such as a maser or similar microwave device, prevents undesirable interaction of the building blocks and allows each driving unit to activate a multiple of driven ones. A coupling inductor also avoids direct current loading, though it is accompanied by a time delay in the appearance of an output voltage across driven

building blocks, thus giving the AND gate chain the effect of a delay line.

The versatility of the building blocks may be further demonstrated by connecting a multiple number of them serially to produce a multistable circuit. When only two of them are placed in series the result is the bistable circuit of FIG. 11. In contrast with the earlier bistable circuit of FIG. 8*a*, pulses in one direction only can effect an interchange of building block voltage states at the close of a switching interval. The biasing resistor R_b taken in combination with battery E_b is appropriately adjusted to place the operating steady state in the middle of a composite characteristic according to techniques discussed below. Capacitor C_b serves to bypass battery E_b for high frequency currents and helps maintain constant potential at the battery terminals. It is important that the source of driving pulses be placed directly across the serial combination of the building blocks in order to minimize power requirements. The constituents of the individual building blocks are selected in accord with requirements previously presented. In block **11–1** current I_{1-1} flows through diode D_1. I_{1-2} is the current in the shunt branch containing L_1 and R_{p1}. I_{2-1} flows in diode D_2 while current I_{2-2} is in the shunt branch containing L_2 and R_{p2}. I_b is furnished by battery E_b and the pulse current has an amplitude I_o.

Restrictions on the selection of auxiliary parameters and the mode of switching operation are demonstrated in FIGS. 12*a*–12*c* for the special case when both building blocks are identical. FIG. 12*a* shows the composite characteristic of two building blocks whose individual characteristics are represented respectively by FIG. 12*b* for block **11–1** and FIG. 12*c* for block **11–2**. Since the two blocks are in serial connection the same current must flow through both and the composite characteristic is obtained by summing the voltages produced by a given current. Region *aa* of the composite characteristic applies when both blocks are in a low voltage state. By contrast region *bb* is applicable when both blocks are in a high voltage state. The narrow region *cc* extending between Î and Ǐ is operative when one block is in its high voltage state and the other is in its low voltage state. If the building blocks were other than identical, there would be more than one region such as *cc*. To be bistable the circuit of FIG. 12*a* must have its load line *dd* adjusted to intersect segment *cc*. Once a given biasing voltage E_b has been selected R_b is restricted to the sector *ee* and its magnitude is given by the reciprocal of the slope of the line chosen. Of course, E_b may be shifted along axis V. An increase reduces the power requirements of the battery but simultaneously limits the possible values of R_b. On the other hand, a decrease in the strength of E_b increases the power requirements. By way of example, E_b and R_b have been chosen at intermediate positions. In the steady state the total current flowing through both of the building blocks is equal to I_b, given by the intersection of segment *cc* and load line *dd* at voltage V_1+V_2. Superficially, it would appear that the voltages of the two building blocks should be equal, but the load line R_b intersects the composite characteristic in its negative resistance region. There will be voltage fluctuations until the individual building blocks have reached positions of stable equilibrium in their positive resistance regions. For the load line selected this can occur only if one building block is at low voltage V_1 and the other is at high voltage V_2. During disequilibrium the building block whose voltage is changing at the greatest rate approaches stabilization in the high voltage condition and constrains the other to approach a low voltage state. In building block **11–1**, for which FIG. 12*b* is applicable with the commencement of switching at time t_0, the current I_b divides between the branch containing R_{p1} and diode D_1. The amount passing through R_{p1} is obtained from the linear graph *ab* whose slope is

$$\frac{1}{R_{p1}}$$

At V_1 it is I_{1-2}. For building block **11–2**, whose voltage state is shown in FIG. 12*c*, I_b places the equilibrium voltage at V_2 at the beginning of the switching period t_0. The current through R_{p2} equals I_{2-2}.

The mechanism of switching is best understood from a consideration of loci *ff* and *gg* in FIG. 12*a*. When a negative switching pulse I_o is applied the voltage of the circuit must remain momentarily constant because of the intrinsic capacitance associated with each of the building blocks and the presence of inductor L. If the pulse has a perfectly vertical leading edge, the current through the building blocks must change instantaneously by dropping to point *hh* on locus *ff*. Thereafter, there is a transition along a segment of constant current until both building blocks are in their low voltage state at *kk* if the applied pulse is of sufficient duration. When the ideal pulse is removed, the intrinsic capacitances of both building blocks prevent an instantaneous change in voltage and the building block current tends to increase along a segmet of constant voltage until it meets load line *dd* at *mm*. The locus then moves along the load line until it intersects the composite characteristic where equilibrium in re-established. In practice the driving pulse departs from ideal and the inductors L_1 and L_2 prevent instantaneous changes in the currents flowing through them, with the result that the actual locus during the switching cycle more nearly resembles *gg*. The time sequence is approximated on the loci at five points, t_0 through t_4. Corresponding points are indicated on the switching patterns in FIGS. 12*b* and 12*c* for the individual building blocks. Ideal loci are designated *ff*–**1** and *ff*–**2** and the actual loci are marked *gg*–**1** and *gg*–**2**. The building block inductors play important parts in controlling the change of state during switching. When both diodes have been driven to their low voltage state at *kk* the current in L_2 is greater than that in L_1 because it was initially greater and the tendency of an inductor is to maintain its current flow unchanged. At the moment of switching t_0 the current I_{2-2} through L_2 was very much larger than I_{1-2} through L_1. At time t_2, just before removal of the switching pulse, the current I_{1-1} through diode D_1 must be greater than I_{2-1} through diode D_2, but the voltages across both diodes will be nearly equal only if the circulating current from the discharge of the diode intrinsic capacitor is greater in D_2 than in D_1. When the switching pulse is removed circuit equilibrium requires a restoration of the steady state current I_b. Both diode intrinsic capacitors are able to accommodate instantaneous changes of current, but the net flow in the capacitor of D_1 must be greater than in the capacitor of D_2 since the same current must flow through both building blocks and the currents in the inductive branches resist change. As a result and as shown by Equation 1, the rate of voltage change as measured by the magnitude of current flowing in each diode intrinsic capacitor is intially greater in building block **11–1** than in building block **11–2**, so that the former rapidly makes the transition to the high voltage state and constrains the latter to a low voltage equilibrium, thereby completing the switching cycle.

To realize its full potential for rapid switching, the building block of FIG. 4 must be able to function as a microwave circuit component. As is well known, distributed parameters become the high frequency counterpart of the lumped elements which define circuit behavior at low frequencies, and special precautions must be taken to prevent unwanted impedance effects. In the representative high frequency embodiment **11** of FIG. 13 diode **3** is positioned between two holders **19–1** and **19-2** which act as terminals **1** and **2** of the building block. The diode is mounted at the base of metal pin **18–1** and the combination is inserted into a channel in the holder **19–1** until the diode mesa is in touching contact with a dia-

phragm 20 at the apex of a pin 18–2 inserted into a similar channel in the holder 19–2. This arrangement assures a point contact between the diaphragm and the diode. To make the inductance between the terminals and the diode negligible, the holders must be placed physically as close together as possible, being separated only by a thin dielectric film. This simultaneously increases the capacitance across the diode but not significantly compared with its intrinsic magnitude. Other techniques for minimizing holder inductance are considered in a co-pending application, Dacey-Wallace, Serial No. 855,426, filed November 25, 1959. The thin film is provided by an epoxy resin chosen with a high enough viscosity that it retains its cohesiveness. In the representative model constructed and tested a resin manufactured and sold under the name "Bondmaster M620" was used.

As the holders are pressed together the resin is extruded from the gap between them at their outer periphery and expands into a toroidal solid of revolution which may be made as large as needed for a specific structure. It may be dissymmetrically machined to various geometries and the resin itself may have materials added to alter the electrical characteristics of the circuit. Since the toroidal surface spans from one holder to another a resistive coating deposited on it will be directly across the terminals of the building block. Each incremental arc of the coating provides part of the path for an inductive circulating current which is impeded by the resistive nature of the coating. The incremental inductance and resistance may be summed over the entire surface to produce the same effect at microwave frequencies that the series combination of an inductor and resistor has at low frequencies. It is also possible to produce a variable inductance, for example, by inserting a ferrite slab within the toroid and subjecting it to a variable magnetic bias field.

The high frequency embodiment of the building block is usable in a wide variety of circuits. Typical is the bistable circuit of FIG. 11 whose microwave embodiment is presented in FIG. 14 and whose mode of operation has been discussed previously.

In the coaxial section of FIG. 14 a short-circuit termination 23 caps one end of a cylindrical outer conductor 24. Two building blocks 11–1 and 11–2 are placed in series combination by being stacked one on top of the other and are interposed between the short-circuit termination 23 and a center conducting coaxial segment 25 of a coaxial section. As depicted, each building block differs from the prototype of FIG. 13 in having a toroid of rectangular, instead of elliptical, cross section. This permits a reduced diameter for the outer coaxial conductor 24. For simplicity in construction the combined building blocks may be manufactured as a single unit. To provide the equilibrium bias which places one building block in its low voltage state and the other in its high voltage state, a battery E_b is connected across the terminals of the feeder coaxial line 26. The inner conductor of the feeder abuts an annular resistive disk 27 which serves as bias resistor R_b. The disk is co-extensive with the surface of inner conductor 25 and provides a direct current link with battery E_b through both building blocks. Dielectric disk 28 extends between the inner and outer conductors of the feed line, and being a high frequency by-pass condenser C_b, its axial dimension is dependent on the wall thickness of outer coaxial conductor 23. At its open end the coaxial section is tapered to provide an impedance match with a source of pulsing current I_o which causes an interchange between the voltage states of the two building blocks after input pulses are applied and terminated. Adjustments, such as in the taper, may be made to offset the discontinuity effects occasioned by the presence of the annular resistive disk 27. The change in voltage state produced by current pulses I_o is monitored across an output coaxial line 29 whose center conductor joins the serially combined building blocks between their toroidal surfaces.

The configuration of FIG. 14 assures input pulsing, direct current bias and the availability of output directly across the diode building block 11–1 with minimum circuit complexity.

What is claimed is:

1. An electronic threshold switch, responsive to signals from an excitation source and a biasing source, which comprises a first terminal and a second terminal, a first branch extending between said terminals and containing a diode having a current-voltage characteristic manifesting a region of negative resistance between first and second regions of positive resistance, a first threshold between the first region of positive resistance and said region of negative resistance, and a second threshold between said region of negative resistance and the second region of positive resistance, said diode being set by a biasing signal for bistable operation in two alternative states of stable equilibrium, whereby an excitation signal carrying the operation of said diode beyond one of the thresholds initiates a transition from one state to another, and control means extending between said terminals, said control means comprising a padding resistor connected in shunt with said diode and proportioned to have a maximum resistive magnitude greater than the minimum resistive magnitude of said negative resistance for controlling the relative displacement of said first threshold from said second threshold to regulate the magnitude of said excitation signal which effects said transition, said padding resistor unavoidably operating, by itself, to cause a reduction in the speed of said transition, and reactive means connected in shunt with said diode and proportioned to offset said reduction.

2. A two-terminal switching network as defined in claim 1, adapted for employment at microwave frequencies, wherein said diode comprises a crystalline wafer in contact with opposed surfaces of the terminals, said surfaces being in close proximity to each other, and means for confining the resistive and reactive effects of said control means to the region between said surfaces.

3. A logic circuit comprising the network of claim 1, a source of bias current and a plurality of variable current sources connected in shunt with said network, each of said sources comprising the series combination of a resistor of large magnitude and a voltage source, said bias current source being proportioned to place said network in stable equilibrium at a low voltage operating point, said several variable current sources being so proportioned that only the simultaneous presence of all of the plurality exceeds a threshold current thereby causing a rapid transition of said network from a low voltage state to a high voltage state, and means for detecting said transition.

4. The logic circuit of claim 3 in which the inductance of said two-terminal network is of a prescribed magnitude greater than that satisfying the following equation:

$$\beta' = \sigma'_0{}^2$$

where

$$\beta' = \frac{1}{LC}\left(1+\frac{R_p}{R_0}\right)$$

$$\sigma_0{}'^2 = \frac{1}{4}\left(\frac{1}{R_0 C}+\frac{R_p}{L}\right)^2$$

R_0=positive resistance for building block diode,
R_p=magnitude of padding resistor,
L=inductive magnitude of reactive means, and
C=magnitude of the diode capacitance,

thereby to assure a nonoscillatory overshoot accompanying said rapid voltage transition.

5. The logic circuit of claim 3 wherein said inductive means comprises an inductor so proportioned that its inductance L is dependent upon the diode capacitance C, padding resistance R_p and negative resistance magnitude R in substantial accordance with the formula:

$$L=CR_pR$$

whereby the second derivative of the reciprocal of switching speed with respect to inductance is substantially zero so that an increase in said switching speed from an increase in said inductance beyond said limit is offset by a decrease in said switching speed from an increase in said padding resistance.

6. A circuit to perform logic functions comprising a plurality of driving components each having a network as defined in claim 1 in parallel with at least two sources of driving current, at least one driven component having a network as defined in claim 1, means for supplying bias currents to all of said components, and coupling means interconnecting each one of said driving components with said driven component whereby changes of voltage states of said driving components cause like changes of voltage state in said driven component.

7. Apparatus as defined in claim 6 wherein said coupling means comprises a series resistor R_c of predetermined magnitude whereby a composite negative resistance is presented at the input terminals at any one of said components.

8. Apparatus as defined in claim 6 wherein said coupling means comprises a resistor R_c proportioned to satisfy the relation:

$$R_c>\frac{RR_p}{R_p-R}-\frac{R_0R_p}{R_0+R_p}$$

whereby rapid switching is assured when no driving component is loaded by any other,

where

R=magnitude of the diode negative resistance,
R_0=positive resistance for building block diode, and
R_p=magnitude of padding resistor.

9. Apparatus as defined in claim 6 wherein said coupling means comprises a resistor R_c proportioned to satisfy the relation:

$$R_c>2\left(\frac{RR_p}{R_p-R}\right)$$

where R and R_p are, respectively, the magnitude of the diode negative resistance and the magnitude of the padding resistance thereby to assure rapid switching despite the loading of any one driving component by any other.

10. Apparatus as defined in claim 6 wherein said coupling means comprises an isolation amplifier.

11. Apparatus as defined in claim 6 wherein the driving current source of each of said driving components comprises a voltage source connected in series with a resistor of magnitude R_d proportioned according to the relationship:

$$R_d>2R'$$

where R'=magnitude of the composite negative resistance presented at the terminals of each of said driving components as loaded by every other one of said components.

12. A bistable switching circuit comprising a first branch wherein first and second networks as defined in claim 1 are connected in series with each other thereby having the same current flowing through both to produce a composite characteristic with a first region of positive resistance in which both of said networks are in a low voltage state, a second region of positive resistance in which both of said networks are in a high voltage state and a third region therebetween extending between a current minimum and a current maximum in which one of said networks is in a low voltage state and the other is in a high voltage state; a second branch, in shunt with said first branch wherein a biasing resistor is connected in series with a source of bias voltage thereby causing said bistable circuit to be in equilibrium in said third region whereby said first network is in a high voltage state and said second network is in a low voltage state; and a third branch, in shunt with said first branch, having pulsing means for momentarily reducing said current in said first branch whereby said first network is driven to its low voltage state for which its inductive current exceeds that of said second network thereby causing, on deactivation of said pulsing means, the rate of change of voltage in said second network to exceed that of said first network so that said networks must interchange their voltage states.

13. Apparatus as defined in claim 12 wherein the magnitude of said resistor is equal to the reciprocal of the line segment on said composite characteristic originating at the voltage of said bias and intersecting said third region within extremities delimited by said current maximum and said current minimum.

14. A switching network comprising a first terminal, a second terminal, a first branch extending between said terminals and containing only a crystal diode having a voltage-controlled region of negative resistance —R between first and second regions of positive resistance R_{01} and R_{02}, a current maximum between said first region of positive resistance R_{01} and said region of negative resistance —R, and a current minimum between said region of negative resistance —R and said second region of positive resistance R_{02}, means for biasing said diode for bistable operation, whereby said diode adopts either a low voltage state of stable equilibrium in said first region of positive resistance R_{01} or a high voltage state of stable equilibrium in said second region of positive resistance R_{02}, and a second branch extending between said terminals and containing a padding resistor whose resistive magnitude R_p is greater than that of said diode negative resistance —R, thereby controlling the magnitude of the difference between said current maximum and said current minimum and regulating the magnitude of excitation current which effects a rapid voltage transition from either one of said regions of positive resistance to the other, and means for controlling the rate of said rapid voltage transition, said means comprising an inductor, having an inductance L, connected in series with said padding resistor, whereby the natural frequencies δ_0 and β for the portion of said transition occurring in said region of negative resistance and the natural frequencies δ'_0 and β' for those portions of said transition occurring in said regions of positive resistance are given by the relations:

$$\delta_0=\frac{1}{2}\left(\frac{1}{-RC}+\frac{R_p}{L}\right)$$

$$\beta=\frac{1}{LC}\left(1+\frac{R_p}{-R}\right)$$

$$\delta'_0=\frac{1}{2}\left(\frac{1}{R_0C}+\frac{R_p}{L}\right)$$

$$\beta'=\frac{1}{LC}\left(1+\frac{R_p}{R_0}\right)$$

where C is the magnitude of the diode capacitance, R_0 is R_{01} in said first region of positive resistance, R_0 is R_{02} in said second region of positive resistance and other symbols are as defined above.

15. Apparatus as defined in claim 14 wherein said inductor is of magnitude dependent upon a prescribed time constant of said network operating in its negative resistance condition substantially according to the relation:

$$\tau_1=\frac{1}{\sigma_0+(\beta+\sigma_0^2)^{1/2}}$$

where τ_1=time constant of a rising exponential wave during switching through said negative resistance condition.

16. Apparatus as defined in claim 14 wherein said inductor is of magnitude dependent upon a prescribed time

constant of said network operating in its positive resistance condition substantially according to the relation:

$$\tau_2=\frac{1}{\sigma'_0+(\beta'+\sigma'_0{}^2)^{1/2}}$$

where τ_2=time constant of a rising exponential wave during switching through said positive resistance condition, and $\sigma'_0{}^2>\beta'$.

17. Apparatus as defined in claim 14 wherein said inductor is of magnitude dependent upon a prescribed time constant of said network operating in its positive resistance condition substantially according to the relation:

$$\tau_3=\frac{1}{\sigma'_0}$$

where τ_3=time constant of a rising exponential wave during switching through said positive resistance condition,

$$\sigma'_0{}^2\leqslant\beta'$$

and other symbols are as for claim 4.

18. An integral high frequency building block for performing logic functions comprising a crystal diode mounted between first and second distinct terminal holders, said holders being closely spaced from each other by a dielectric film thereby to assure a minimal inductance of the distributed parameter type between said diode and the outer peripheries of said holders in the surfaces of said film, a dielectric body spanning the spacing between said holders and in touching contact therewith only at said peripheries said body being an extrusion of said film between said holders, inductive and resistive means on the surface of said body comprising a coating of the distributed parameter type whereby controlled amounts of inductance and resistance are effectively connected in series across said terminals of said building block, said controlled amount of inductance being significantly greater than said minimal inductance.

19. A high speed switching unit which comprises a crystalline wafer having a negative resistance of the voltage-controlled type, two mounting plates disposed in substantially parallel arrangement and in contact, respectively, with opposite faces of said wafer, a body of solid low-loss dielectric material surrounding said wafer, substantially filling the remaining space between said plates, and extending beyond the peripheries of said plates, the configuration of the surface of said body being that swept out by the rotation, through a full revolution about an axis perpendicular to the opposite faces of said wafer, of a key-hole shaped figure lying in a plane including said perpendicular axis, and a film of conductive material of preassigned resistivity overlying the entire surface of said body that is not included between said plates and in electrical contact, at its edges, with the peripheries of said plates, whereby said body, with its resistive film, manifests the properties of distributed resistance and inductance, connected to said plates and in parallel with said wafer.

20. A switching network which comprises two like, similarly poled, bistable circuits connected in series between a first terminal and a second terminal, each of said circuits comprising two parallel branches, the first branch of each circuit containing only a crystal diode, the second branch of each circuit containing only an inductor and a padding resistor, connected in series, each of said diodes having a current-voltage characteristic of the voltage-controlled type, having a current maximum for a lower voltage V_1, a current minimum for a higher voltage V_2, a negative resistance branch joining said maximum to said minimum, a first positive resistance branch for voltages less than said lower voltage and a second positive resistance branch for voltages above said higher voltage, means for applying across said first and second terminals a bias voltage V_b of a magnitude substantially equal to

$$V_b=V_1+V_2$$

whereby one of said diodes adopts a first stable state in which its voltage is less than V_1 and the other diode adopts a second stable state in which its voltage is greater than V_2, the currents flowing through said series-connected circuits being alike, each of said resistors being proportioned to reduce the slope of the negative resistance branch of the current-voltage characteristic of its shunt-connected diode to a preassigned low value, connections for applying a voltage pulse to said first and second terminals of a polarity and magnitude to initiate a shift of one of said diodes from the state it occupies toward the state occupied by the other diode, each of said inductors being proportioned to impede abrupt changes of the current through its series-connected resistor, whereby a shift of the state of said last-named one diode to the state of the other diode is accompanied by an opposite shift of the state of said other diode to the state occupied by said one diode.

21. A microwave bistable switching circuit comprising a cylindrical outer conductor, a short-circuit termination at one end thereof, the series combination of two integral high frequency building blocks as defined in claim 18 mounted coaxially with said outer conductor between said short-circuit termination and a coaxial inner conductor, a resistive disk interposed between said inner and outer conductors, a feeder coaxial line joining said cylindrical outer conductor at a right angle thereto and having its inner conductor in contact with said disk whereby a voltage source across said feeder line causes a biasing current to circulate through said series combination of building blocks thus placing one of said blocks in its high voltage state and the other in its low voltage state, a dielectric disk between the conductors of said feeder line and presenting at high frequencies a by-pass capacitance across said voltage source, a unidirectional source of current pulses between said inner and outer conductors, a tapered section of coaxial line between said source of pulses and said disk providing matching means to compensate for discontinuities occasioned by the presence of said disk, and means for utilizing the rapid voltage transition from one state to another affected by the application of said current pulses, said means comprising a coaxial line joining said cylindrical outer conductor at a right angle thereto and having its inner conductor abutting said series combination of building blocks between the toroidal surfaces thereon.

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