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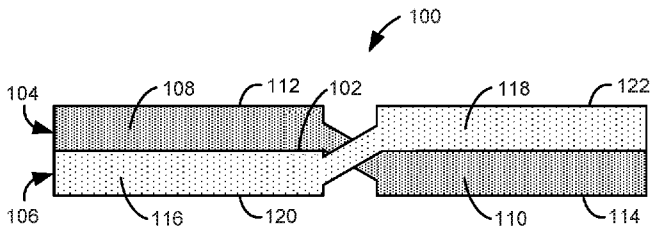


Fig. 1

(57) Abstract: A device includes a P-N junction comprising a monolithic N-type semiconductor layer coupled to a monolithic P-type semiconductor layer. The monolithic N-type semiconductor layer includes a first portion and a second portion. The first portion has a first surface and the second portion has a second surface facing away from the first surface. The monolithic P-type semiconductor layer includes a third portion and a fourth portion. The third portion has a third surface and the fourth portion has a fourth surface facing away from the third surface.

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P-TYPE SEMICONDUCTOR LAYERS COUPLED TO N-TYPE SEMICONDUCTOR LAYERS

Background

[0001] Displays may use light emitting diodes (LEDs) as the light source for each pixel of the display. Sensors may include an array of photon sensing diodes. LEDs and photon sensing diodes include a P-N junction between an anode and a cathode of the device. LEDs emit light in response to being forward biased. If an LED is reverse biased, no light is emitted.

Brief Description of the Drawings

[0002] Figure 1 is a side view illustrating one example of a device including a P-N junction.

[0003] Figure 2 is a side view illustrating another example of a device including a P-N junction.

[0004] Figure 3 is a schematic diagram illustrating one example of an equivalent circuit for the device of Figure 2.

[0005] Figures 4A and 4B illustrate one example of a device including a P-N junction prior to twisting.

[0006] Figures 5A-5C illustrate one example of the device of Figures 4A and 4B after twisting.

[0007] Figure 6 is a side view illustrating another example of a device including a P-N junction prior to twisting.

[0008] Figure 7 is a top view illustrating one example of a device after twisting.

[0009] Figure 8 is a side view illustrating another example of a device including a P-N junction prior to twisting.

[0010] Figure 9 is a top view illustrating one example of an array of diode pairs.

[0011] Figure 10 is a top view illustrating one example of a pixel of an array.

[0012] Figure 11 is a side view illustrating one example of a pixel of an array.

[0013] Figures 12A and 12B are flow diagrams illustrating one example of a method for fabricating a diode pair.

Detailed Description

[0014] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific examples in which the disclosure may be practiced. It is to be understood that other examples may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present disclosure is defined by the appended claims. It is to be understood that features of the various examples described herein may be combined, in part or whole, with each other, unless specifically noted otherwise.

[0015] Display devices may be fabricated by first fabricating a light emitting diode (LED) array, such as a micro-LED array or a nano-LED array, on a semiconductor or glass substrate. Each LED may then be lifted off the semiconductor substrate and picked and placed onto a transistor of a thin-film-transistor (TFT) array substrate. The LEDs may then be bonded to the TFT array substrate and inspected to make sure each LED was placed such that each LED will be forward biased during operation of the display. Pick and place technologies may be a barrier to micro-LED and nano-LED displays due to low throughput and/or expensive processes. For example, there may be difficulties in handling small die size LEDs and controlling the LED die orientation, difficulties in achieving LED pick and place assembly tolerances, and difficulties in selectively picking and placing the LEDs, which increases post placing process time and expense.

[0016] Accordingly, disclosed herein is a twisted diode pair, such as an LED pair or a photon sensing diode pair. Two diodes having opposite orientations are formed by twisting a monolithic N-type semiconductor layer coupled to a monolithic P-type semiconductor layer. In operation, one of the diodes may be

forward biased while the other one of the diodes may be reverse biased. Accordingly, each diode pair may be picked and placed to fabricate a display device or sensor device without having to orient each diode pair prior to placement. In this way, no matter how the diode pair is placed, one of the diodes will be forward biased during operation.

[0017] As used herein "monolithic" is defined as fabricated as a single structure.

[0018] As used herein "facing away" is defined as facing opposite directions or facing non-parallel directions (e.g., normal vectors for the surfaces are not parallel).

[0019] Figure 1 is a side view illustrating one example of a device 100 including a P-N junction 102. P-N junction 102 includes a monolithic N-type semiconductor layer 104 coupled to a monolithic P-type semiconductor layer 106. Monolithic N-type semiconductor layer 104 includes a first portion 108 and a second portion 110 physically connected to the first portion 108. The first portion 108 has a first surface 112 and the second portion 110 has a second surface 114 facing away from the first surface 112. Monolithic P-type semiconductor layer 106 includes a third portion 116 and a fourth portion 118 physically connected to the third portion 116. The third portion 116 has a third surface 120 and the fourth portion 118 has a fourth surface 122 facing away from the third surface 120. In one example, the first surface 112 may be parallel to the third surface 120, and the second surface 114 may be parallel to the fourth surface 122. The first surface 112 may also be parallel to the fourth surface 122, and the second surface 114 may also be parallel to the third surface 120.

[0020] In one example, as will be described in more detail below, monolithic N-type semiconductor layer 104 and monolithic P-type semiconductor layer 106 form a first light emitting diode (LED) (e.g., micro-LED, nano-LED) having a first orientation and a second LED having a second orientation opposite to the first orientation. In another example, monolithic N-type semiconductor layer 104 and monolithic P-type semiconductor layer 106 form a first photon sensing diode having a first orientation and a second photon sensing diode having a second orientation opposite to the first orientation.

[0021] Figure 2 is a side view illustrating another example of a device 130 including a P-N junction 102. Device 130 is similar to device 100 previously described and illustrated with reference to Figure 1, except that device 130 includes a first contact 132, a second contact 134, a third contact 136, and a fourth contact 138. The first contact 132 is electrically coupled to the first surface 112 of the first portion 108 of the monolithic N-type semiconductor layer 104. The second contact 134 is electrically coupled to the second surface 114 of the second portion 110 of the monolithic N-type semiconductor layer 104. The third contact 136 is electrically coupled to the third surface 120 of the third portion 116 of the monolithic P-type semiconductor 106. The fourth contact 138 is electrically coupled to the fourth surface 122 of the fourth portion 118 of the monolithic P-type semiconductor 106.

[0022] Device 130 may include Si, group III-IV elements, organic materials, 2D materials, and/or other semiconductor materials. The monolithic N-type semiconductor layer 104 and the monolithic P-type semiconductor layer 106 have a relatively moderate to large resistivity, such as tens or hundreds of ohms per square meter. For a sheet like P-N junction 102, the active current flows in the localized area near the contacts (i.e., between third contact 136 and first contact 132 and between fourth contact 138 and second contact 134). The remaining portions of the monolithic N-type semiconductor layer 104 and the monolithic P-type semiconductor layer 106 are connected through a large parasitic resistance. Due to the large parasitic resistance, the P-N junction device 130 includes a reverse biased diode in parallel with a forward biased diode even though first portion 108 of monolithic N-type semiconductor layer 104 is physically connected to second portion 110 of monolithic N-type semiconductor layer 104 and third portion 116 of monolithic P-type semiconductor layer 106 is physically connected to fourth portion 118 of monolithic P-type semiconductor layer 106.

[0023] Figure 3 is a schematic diagram illustrating one example of an equivalent circuit 150 for the device 130 of Figure 2. Equivalent circuit 150 includes a first diode 152 and a second diode 154. The anode of first diode 152 is electrically coupled to a first node 156, and the cathode of first diode 152 is electrically

coupled to a second node 158. The anode of second diode 154 is electrically coupled to the second node 158, and the cathode of second diode 154 is electrically coupled to the first node 156. Therefore, first diode 152 has a first orientation and second diode 154 has a second (i.e., opposite) orientation to the first orientation.

[0024] First diode 152 includes first contact 132, first portion 108 of monolithic N-type semiconductor layer 104, third portion 116 of monolithic P-type semiconductor layer 106, and third contact 136 of Figure 2. Second diode 154 includes second contact 134, second portion 110 of monolithic N-type semiconductor layer 104, fourth portion 118 of monolithic P-type semiconductor layer 106, and fourth contact 138 of Figure 2. Node 156 is provided by electrically coupling second contact 134 to third contact 136 via, for example, a first electrode. Node 158 is provided by electrically coupling first contact 132 to fourth contact 138 via, for example, a second electrode.

[0025] Figures 4A and 4B illustrate one example of a device 200 including a P-N junction 102 prior to twisting. Figure 4A illustrates a top view of device 200, and Figure 4B illustrates a cross-sectional view of device 200. An N-type semiconductor layer 104 is formed on a P-type semiconductor layer 106 to provide a layer stack. The N-type semiconductor layer 104 and the P-type semiconductor layer 106 may be formed via printing, via photolithography, deposition, and/or etching processes, or via other suitable processes.

[0026] Figures 5A-5C illustrate one example of a device 210 after twisting the device 200 of Figures 4A and 4B. Figure 5A illustrates a top view of device 210, Figure 5B illustrates a cross-sectional view of the portion of device 210 indicated in Figure 5A, and Figure 5C illustrates a cross-sectional view of the portion of device 210 indicated in Figure 5A. As shown in Figure 5A, device 200 is twisted or folded in the central region of the device to provide device 210 having two diodes (i.e., a diode pair) with opposite orientations. While a single twist or fold is illustrated in Figure 5A, in other examples device 210 may have multiple twists or folds as long as the resulting device includes a diode pair having opposite orientations. In this example, the twist results in an L-shaped device 210. As shown in Figure 5B, a first diode includes a P-N junction 102 with the

N-type semiconductor layer 104 on the upper side and the P-type semiconductor layer 106 on the lower side. As shown in Figure 5C, a second diode includes a P-N junction 102 with the P-type semiconductor layer 106 on the upper side and the N-type semiconductor layer 104 on the lower side.

[0027] In one example, the N-type semiconductor layer 104 and the P-type semiconductor layer 106 may be twisted mechanically, such as by using a tool. In another example, the N-type semiconductor layer 104 and the P-type semiconductor layer 106 may be twisted by applying thermal energy to the N-type semiconductor layer and the P-type semiconductor layer. In yet another example, the N-type semiconductor layer 104 and the P-type semiconductor layer 106 may be twisted by applying an electrical field or a magnetic field to the N-type semiconductor layer 104 and the P-type semiconductor layer 106. The N-type semiconductor layer 104 and the P-type semiconductor layer 106 may also be twisted by fabricating the N-type semiconductor layer 104 and the P-type semiconductor layer 106 at an elevated temperature and with different stresses in each layer. In this case, when the device cools down, the different stresses in the layers will cause the device to twist.

[0028] Figure 6 is a side view illustrating another example of a device 230 including a P-N junction 102 prior to twisting. Device 230 is similar to device 200 previously described and illustrated with reference to Figures 4A-4B, except that device 230 includes a first contact 132, a second contact 134, a third contact 136, and a fourth contact 138. The first contact 132 is electrically coupled to the upper left side of N-type semiconductor layer 104, and the second contact 134 is electrically coupled to upper right side of N-type semiconductor layer 104. The third contact 136 is electrically coupled to the lower left side of P-type semiconductor layer 106, and the fourth contact 138 is electrically coupled to the lower right side of P-type semiconductor layer 106. The first contact 132 is opposite to and faces away from the third contact 136, and the second contact 134 is opposite to and faces away from the fourth contact 138.

[0029] In this example, the first contact 132 and the second contact 134 are electrically coupled to the N-type semiconductor layer 104 and the third contact

136 and the fourth contact 138 are electrically coupled to P-type semiconductor layer 106 prior to twisting the device. First contact 132, second contact 134, third contact 136, and fourth contact 138 may be formed via printing (e.g., inkjetting Ag), via photolithography, deposition, and/or etching processes, or via other suitable processes.

[0030] Figure 7 is a top view illustrating one example of a device 240 after twisting. In one example, device 240 is formed by twisting the device 230 of Figure 6 with first contact 132, second contact 134 (not visible in Figure 7), third contact 136 (not visible in Figure 7), and fourth contact 138 already attached. In another example, device 240 is formed by forming first contact 132, second contact 134, third contact 136, and fourth contact 138 on the already twisted device 210 of Figures 5A-5C. Accordingly, first contact 132, second contact 134, third contact 136, and fourth contact 138 may be formed prior to twisting the device or after twisting the device.

[0031] Figure 8 is a side view illustrating another example of a device 300 including a P-N junction 302 prior to twisting. Device 300 includes a single layer graphene (SLG) layer 304, a P-type Tungsten diselenide (WSe_2) layer 306, and a hexagonal boron nitride (h-BN) layer 308. P-type WSe_2 layer 306 is formed on h-BN layer 308, and SLG layer 304 is formed on P-type WSe_2 layer 306. Device 300 may then be twisted and a first contact 132, a second contact 134, a third contact 136, and a fourth contact 138 may be formed either before or after the twisting to provide a twisted diode pair. In this example, each layer of device 300 may be printed.

[0032] To achieve efficient electroluminescence, a P-N junction simultaneously injects electrons and holes that recombine to generate a photon emission. Vertically stacked 2D heterostructures like device 300 may be used for this type of application to increase interface area. Optically generated electron hole pairs in Molybdenum disulfide (MoS_2) or other similar 2D materials form stable exciton states even at room temperature because of the extremely large Coulomb interactions in atomically thin 2D materials. Rapid carrier leakage in thin vertical semiconductors may limit electroluminescence efficiency so multilayered doped stacks could be of great advantage. This may help indirect bandgap materials

achieve better efficiency than direct bandgap monolayer materials. Based on the Aluminum oxide (Al_2O_3), P-type Gallium Nitride (pGaN), and nMX_2 devices, this may be easily achieved. Quantum light emitting diodes may be achieved using single layer graphene combined with a TMD, such as p-doped WSe_2 and hexagonal boron nitride as an insulator as in device 300. These may act as quantum light devices (optically active layered semiconductors), which can provide photon generation in the visible spectrum. The stable exciton plays a role in the optical properties of single layered 2D materials such as MoS_2.

[0033] Quantum yield (QY), which is a ratio of the number of photons that a material emits compared to the number of photons absorbed, may be greatly improved in these 2D structured devices by using chemical doping such as liquid ion gating techniques. Ionic liquid gating using super acids may help improve efficiency and performance of multi stacked heterostructured devices. Quantum yield of MoS_2 has been found around 0.1%, but with TFSI treatment about 30% may be achieved. Other chemical doping using TCNQ, F4TCNQ as p-type dopant and NADH n-type dopant may also be useful in structured optical devices.

[0034] Figure 9 is a top view illustrating one example of an array 400 of diode pairs 240. Diode pairs 240 were previously described and illustrated with reference to Figure 7. The contacts are not illustrated in Figure 9 for simplicity. Each diode pair 240 may be placed without having to orient each diode pair, since in either orientation one diode will be forward biased and the other diode will be reverse biased. The diode pairs 240 may be arranged in any suitable number of rows and/or columns to provide an array having the desired size. In this example, each pixel 402 includes a single diode pair 240. In other examples, however, each pixel 402 may include more than one diode pair 240. Each diode pair may include an LED pair such that array 400 provides a display, or each diode pair may include a photon sensor diode (e.g., photodiode) pair such that array 400 provides a sensor.

[0035] Figure 10 is a top view illustrating one example of a pixel 410 of an array. In one example, pixel 410 may provide each pixel 402 of array 400 of Figure 9. In this example, each pixel 410 includes a plurality of diode pairs 240. Within

pixel 410, the diode pairs 240 may be placed without having to orient each diode pair, since in either orientation one diode will be forward biased and the other diode will be reverse biased.

[0036] Figure 11 is a side view illustrating one example of a pixel 420 of an array. Pixel 420 includes a substrate 422, a first electrode 424, a second electrode 426, and a diode pair 130 as previously described and illustrated with reference to Figure 2. First electrode 424 is coupled to substrate 422 and electrically coupled to second contact 134 and third contact 136 of diode pair 130. In another embodiment, first electrode 424 may be electrically coupled to first contact 132 and fourth contact 138 of diode pair 130. Second electrode 426 is electrically coupled to first contact 132 and fourth contact 138 of diode pair 130. In another embodiment, second electrode 426 may be electrically coupled to second contact 134 and third contact 136 of diode pair 130. First electrode 424 and second electrode 426 may be made of a transparent electrically conductive material, such as Indium tin oxide (ITO), or another suitable material. In one example, pixel 420 may be a pixel of a display, such that each diode pair 130 includes a first LED having a first orientation and a second LED having a second orientation opposite to the first orientation. In another example, pixel 420 may be a pixel of a sensor, such that each diode pair 130 includes a first sensor having a first orientation and a second sensor having a second orientation opposite to the first orientation.

[0037] Pixel 420 may be used for each pixel 402 in array 400 of Figure 9 to provide an array of first electrodes 424, where each first electrode 424 is electrically coupled to a first contact 132 and a fourth contact 138 of a diode pair 130 or to a second contact 134 and a third contact 136 of a diode pair 130. In this case, an array of second electrodes 426 are opposite to the array of first electrodes 424, where each second electrode 424 is electrically coupled to a second contact 134 and a third contact 136 of a diode pair 130 or to a first contact 132 and a fourth contact 138 of a diode pair 130. Therefore, a first portion of the array of first electrodes 424 may be electrically coupled to a first contact 132 and a fourth contact 138 of a diode pair 130, and a second portion of the array of first electrodes 424 may be electrically coupled to a second

contact 134 and a third contact 136 of a diode pair 130. Likewise, a first portion of the array of second electrodes 426 may be electrically coupled to a first contact 132 and a fourth contact 138 of a diode pair 130, and a second portion of the array of second electrodes 426 may be electrically coupled to a second contact 134 and a third contact 136 of a diode pair 130. In one embodiment, the array of first electrodes 424 may be coupled to a thin-film-transistor (TFT) array formed on substrate 422 to individually control each pixel 420.

[0038] Figures 12A and 12B are flow diagrams illustrating one example of a method 500 for fabricating a diode pair. As shown in Figure 12A, at 502 method 500 includes forming an N-type semiconductor layer. In one example, forming the N-type semiconductor layer comprises printing the N-type semiconductor layer. At 504, method 500 includes forming a P-type semiconductor layer coupled to the N-type semiconductor layer. In one example, forming the P-type semiconductor layer comprises printing the P-type semiconductor layer.

[0039] At 506, method 500 includes twisting the N-type semiconductor layer and the P-type semiconductor layer to form the N-type semiconductor layer to have a first portion and a second portion, the first portion having a first surface and the second portion having a second surface facing away from the first surface and to form the P-type semiconductor layer to have a third portion and a fourth portion, the third portion having a third surface and the fourth portion having a fourth surface facing away from the third surface. In one example, twisting the N-type semiconductor layer and the P-type semiconductor layer includes applying thermal energy to the N-type semiconductor layer and the P-type semiconductor layer. In another example, twisting the N-type semiconductor layer and the P-type semiconductor layer includes applying an electrical field or a magnetic field to the N-type semiconductor layer and the P-type semiconductor layer.

[0040] As shown in Figure 12B, at 508 method 500 may further include forming a first contact electrically coupled to the first surface. At 510, method 500 may further include forming a second contact electrically coupled to the second surface. At 512, method 500 may further include forming a third contact

electrically coupled to the third surface. At 514, method 500 may further include forming a fourth contact electrically coupled to the fourth surface.

[0041] Although specific examples have been illustrated and described herein, a variety of alternate and/or equivalent implementations may be substituted for the specific examples shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the specific examples discussed herein. Therefore, it is intended that this disclosure be limited only by the claims and the equivalents thereof.

CLAIMS

1. A device comprising:

a P-N junction comprising a monolithic N-type semiconductor layer coupled to a monolithic P-type semiconductor layer,

wherein the monolithic N-type semiconductor layer includes a first portion and a second portion, the first portion having a first surface and the second portion having a second surface facing away from the first surface, and

wherein the monolithic P-type semiconductor layer includes a third portion and a fourth portion, the third portion having a third surface and the fourth portion having a fourth surface facing away from the third surface.

2. The device of claim 1, further comprising:

a first contact coupled to the first surface;

a second contact coupled to the second surface;

a third contact coupled to the third surface; and

a fourth contact coupled to the fourth surface.

3. The device of claim 1, wherein the monolithic N-type semiconductor layer and the monolithic P-type semiconductor layer form a first light emitting diode (LED) having a first orientation and a second LED having a second orientation opposite to the first orientation.

4. The device of claim 1, wherein the monolithic N-type semiconductor layer and the monolithic P-type semiconductor layer form a first photon sensing diode having a first orientation and a second photon sensing diode having a second orientation opposite to the first orientation.

5. The device of claim 1, wherein the first surface is parallel to the fourth surface and the second surface is parallel to the third surface.

6. A device comprising:

an array of diode pairs, each diode pair comprising:

a monolithic N-type semiconductor layer having a first portion and a second portion, the first portion having a first surface and the second portion having a second surface facing away from the first surface;

a monolithic P-type semiconductor layer coupled to the monolithic N-type semiconductor layer, the monolithic P-type semiconductor layer having a third portion and a fourth portion, the third portion having a third surface and the fourth portion having a fourth surface facing away from the third surface;

a first contact coupled to the first surface;

a second contact coupled to the second surface;

a third contact coupled to the third surface; and

a fourth contact coupled to the fourth surface; and

an array of first electrodes, each first electrode electrically coupled to a first contact and a fourth contact of a diode pair or to a second contact and a third contact of a diode pair.

7. The device of claim 6, further comprising:

an array of second electrodes opposite to the array of first electrodes, each second electrode electrically coupled to a second contact and a third contact of a diode pair or to a first contact and a fourth contact of a diode pair.

8. The device of claim 6, wherein a first portion of the array of first electrodes are electrically coupled to a first contact and a fourth contact of a diode pair and a second portion of the array of first electrodes are electrically coupled to a second contact and a third contact of a diode pair.

9. The device of claim 6, wherein each diode pair comprises a first light emitting diode (LED) having a first orientation and a second LED having a second orientation opposite to the first orientation.

10. The device of claim 6, wherein each diode pair comprises a first sensor having a first orientation and a second sensor having a second orientation opposite to the first orientation.

11. A method for fabricating a diode pair, the method comprising:

forming an N-type semiconductor layer;

forming a P-type semiconductor layer coupled to the N-type semiconductor layer; and

twisting the N-type semiconductor layer and the P-type semiconductor layer to form the N-type semiconductor layer to have a first portion and a second portion, the first portion having a first surface and the second portion having a second surface facing away from the first surface and to form the P-type semiconductor layer to have a third portion and a fourth portion, the third portion having a third surface and the fourth portion having a fourth surface facing away from the third surface.

12. The method of claim 11, further comprising:

forming a first contact electrically coupled to the first surface;

forming a second contact electrically coupled to the second surface;

forming a third contact electrically coupled to the third surface; and

forming a fourth contact electrically coupled to the fourth surface.

13. The method of claim 11, wherein twisting the N-type semiconductor layer and the P-type semiconductor layer comprises applying thermal energy to the N-type semiconductor layer and the P-type semiconductor layer.

14. The method of claim 11, wherein twisting the N-type semiconductor layer and the P-type semiconductor layer comprises applying an electrical field or a magnetic field to the N-type semiconductor layer and the P-type semiconductor layer.

15. The method of claim 11, wherein forming the N-type semiconductor layer comprises printing the N-type semiconductor layer, and

wherein forming the P-type semiconductor layer comprises printing the P-type semiconductor layer.

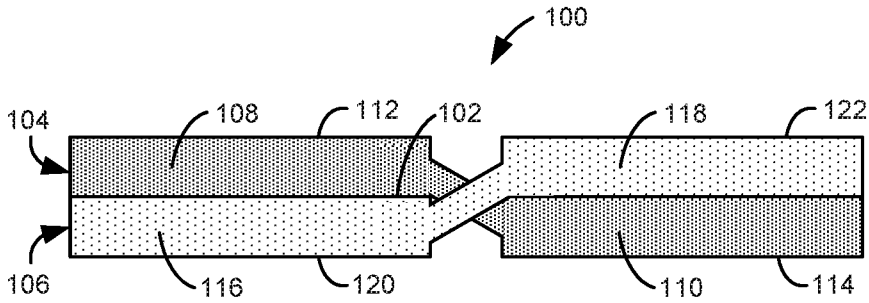


Fig. 1

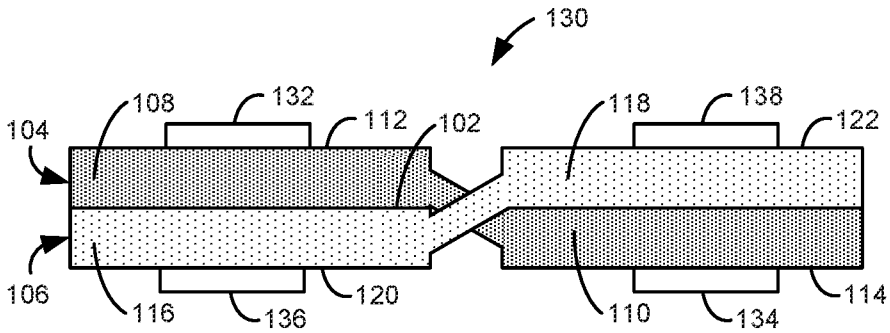


Fig. 2

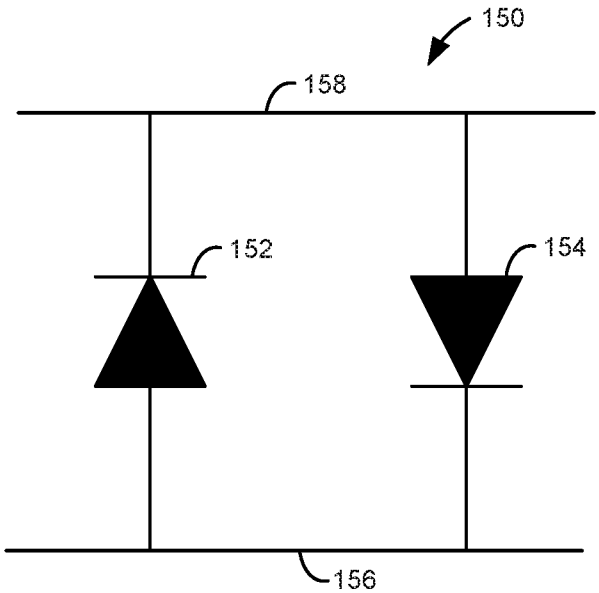


Fig. 3

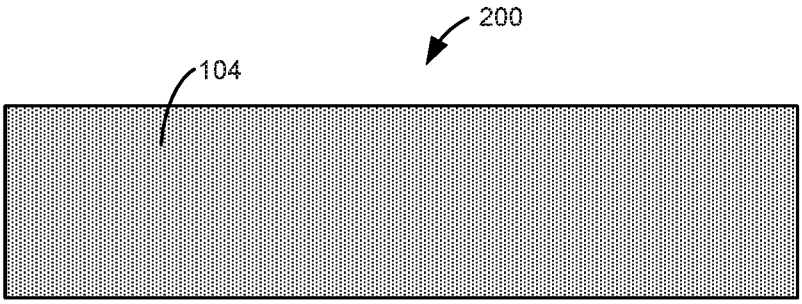


Fig. 4A

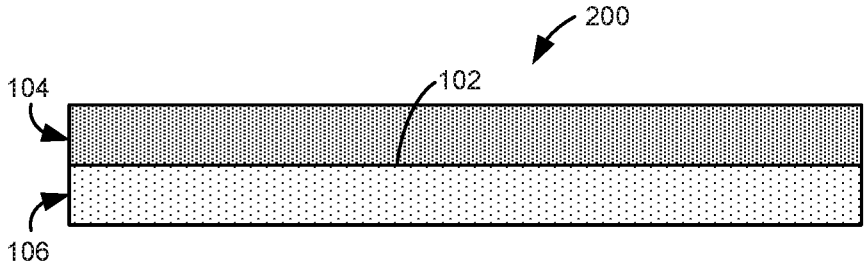


Fig. 4B

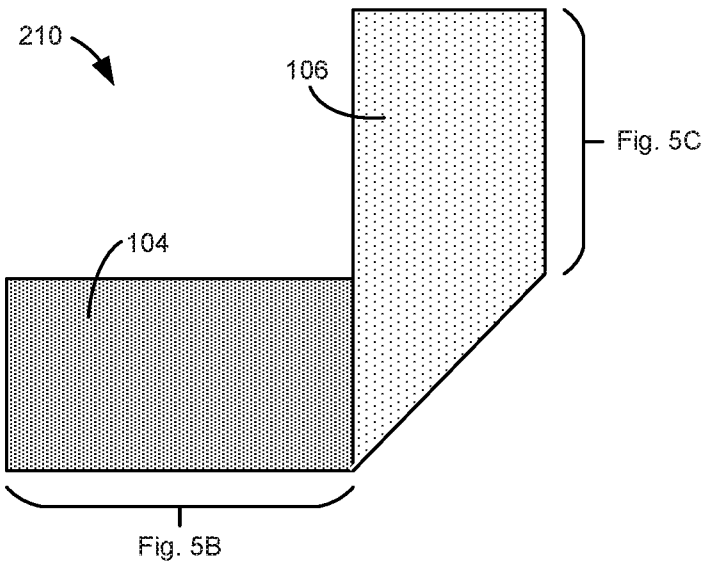


Fig. 5A

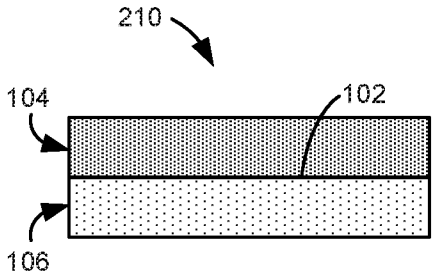


Fig. 5B

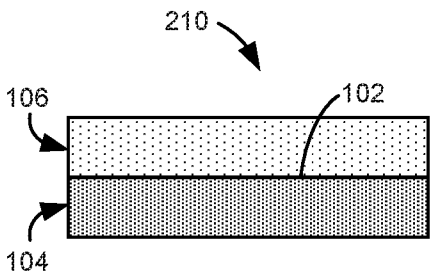


Fig. 5C

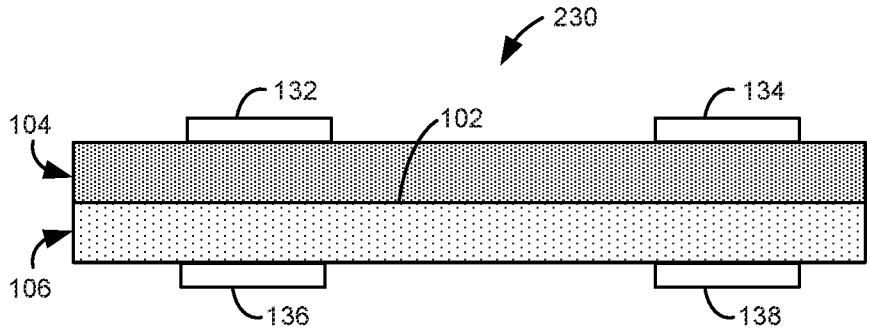


Fig. 6

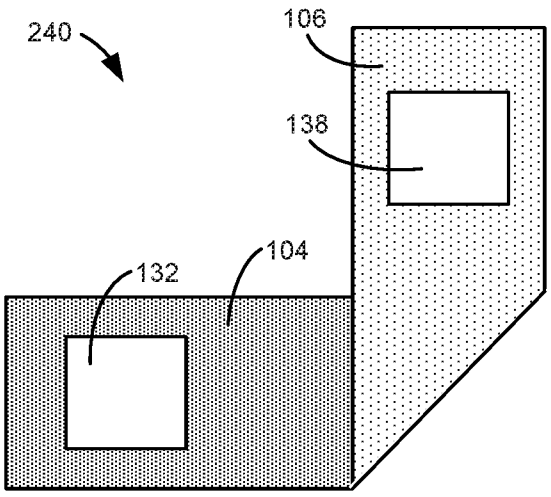


Fig. 7

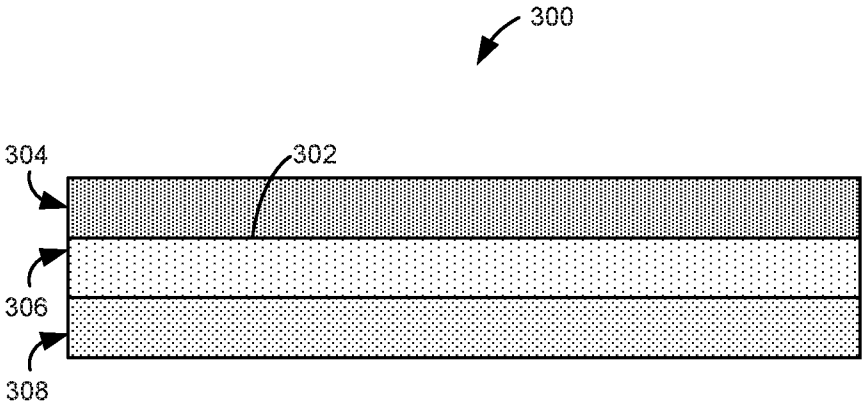


Fig. 8

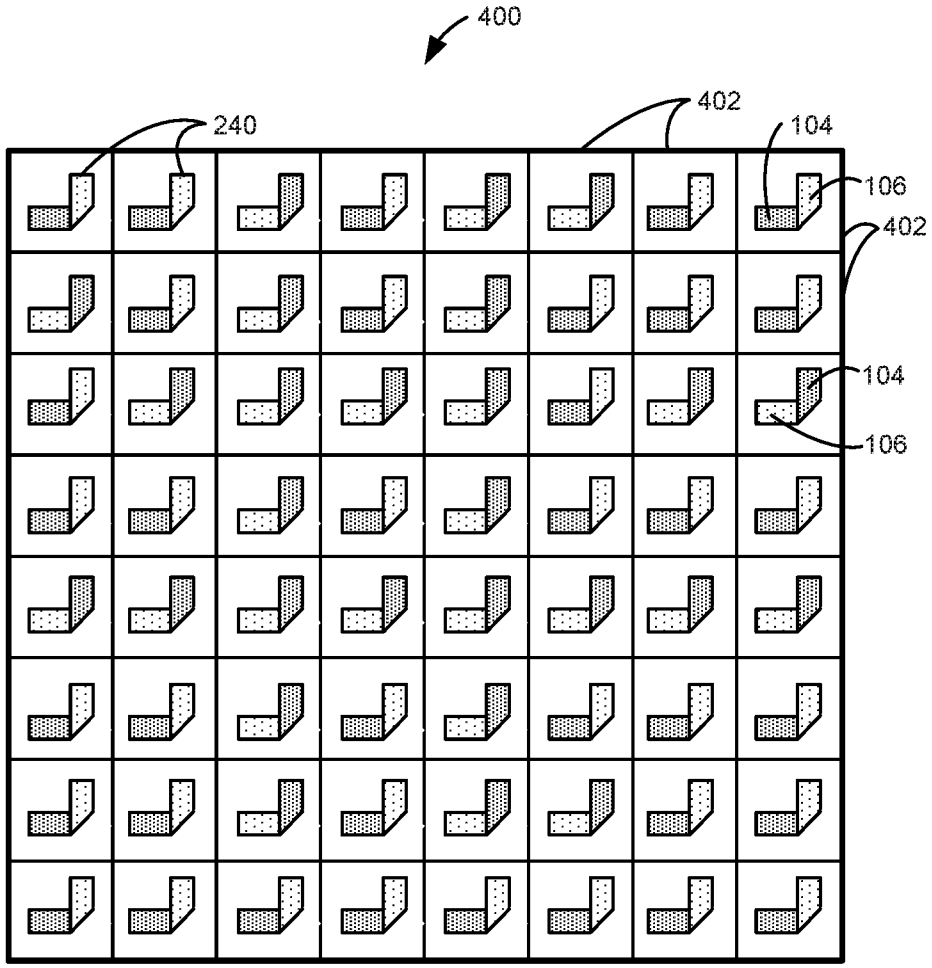


Fig. 9

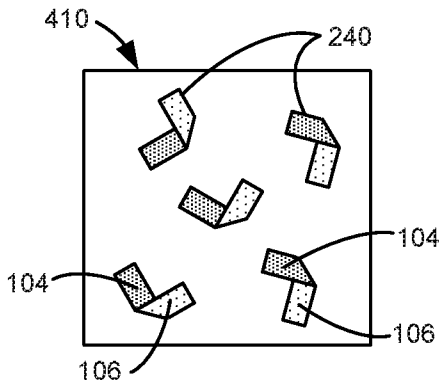


Fig. 10

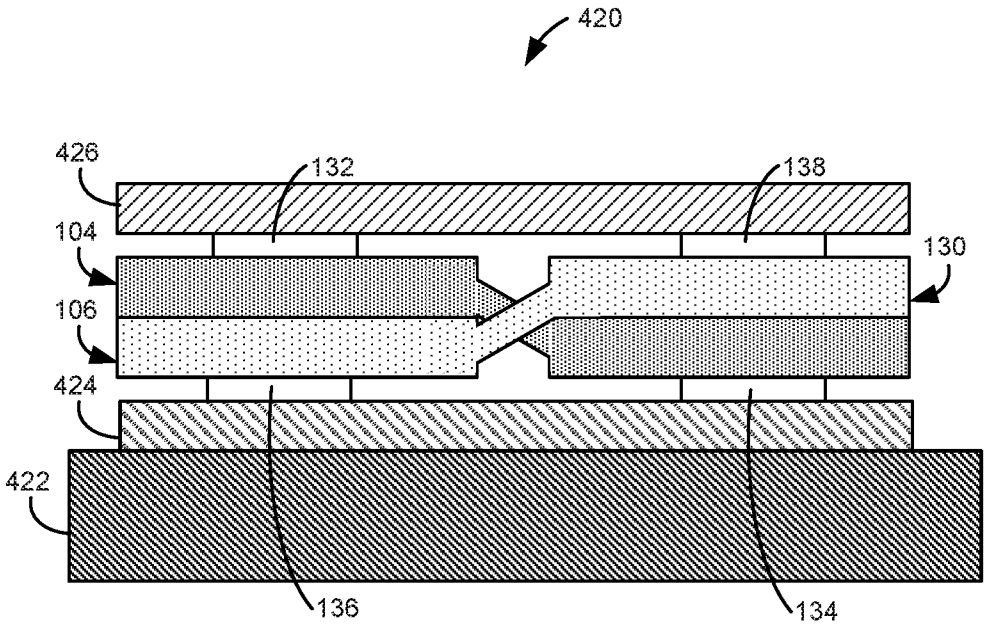


Fig. 11

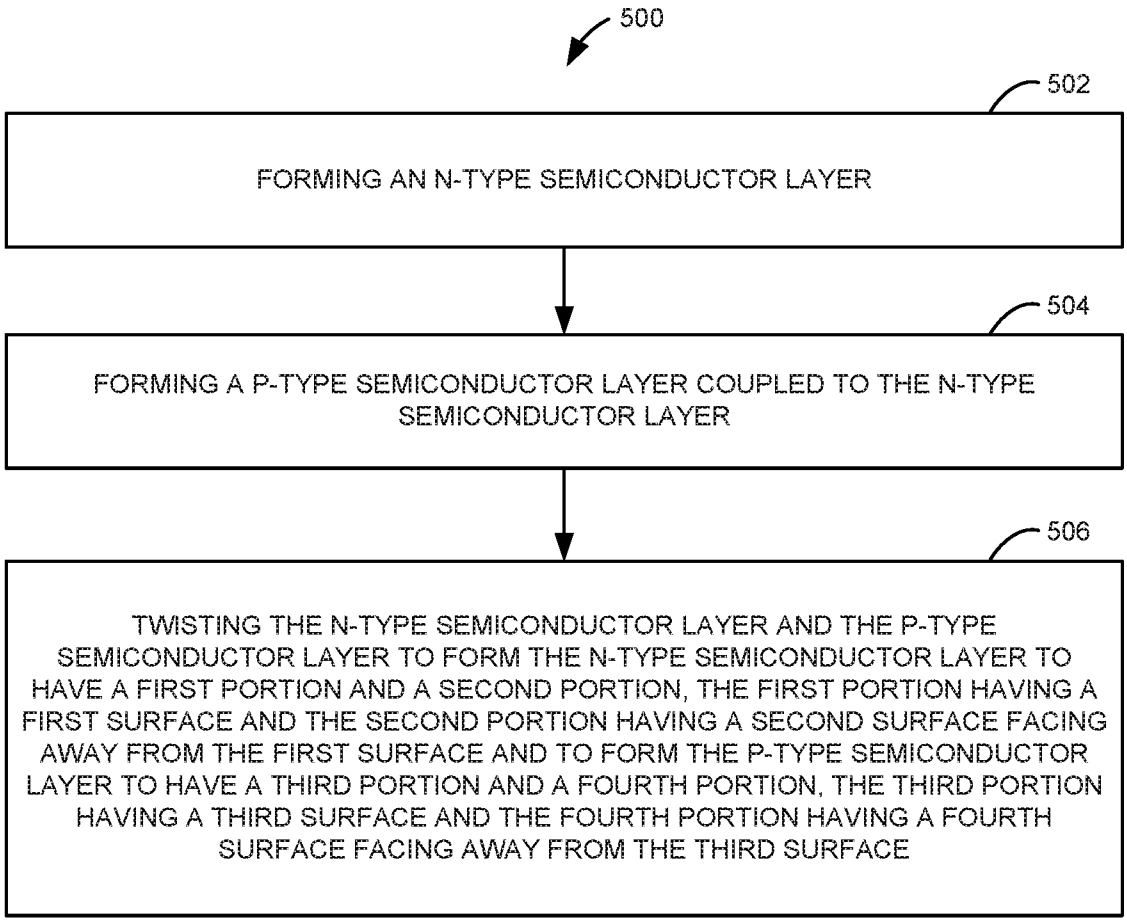

500
502
FORMING AN N-TYPE SEMICONDUCTOR LAYER
504
FORMING A P-TYPE SEMICONDUCTOR LAYER COUPLED TO THE N-TYPE SEMICONDUCTOR LAYER
506
TWISTING THE N-TYPE SEMICONDUCTOR LAYER AND THE P-TYPE SEMICONDUCTOR LAYER TO FORM THE N-TYPE SEMICONDUCTOR LAYER TO HAVE A FIRST PORTION AND A SECOND PORTION, THE FIRST PORTION HAVING A FIRST SURFACE AND THE SECOND PORTION HAVING A SECOND SURFACE FACING AWAY FROM THE FIRST SURFACE AND TO FORM THE P-TYPE SEMICONDUCTOR LAYER TO HAVE A THIRD PORTION AND A FOURTH PORTION, THE THIRD PORTION HAVING A THIRD SURFACE AND THE FOURTH PORTION HAVING A FOURTH SURFACE FACING AWAY FROM THE THIRD SURFACE

Fig. 12A

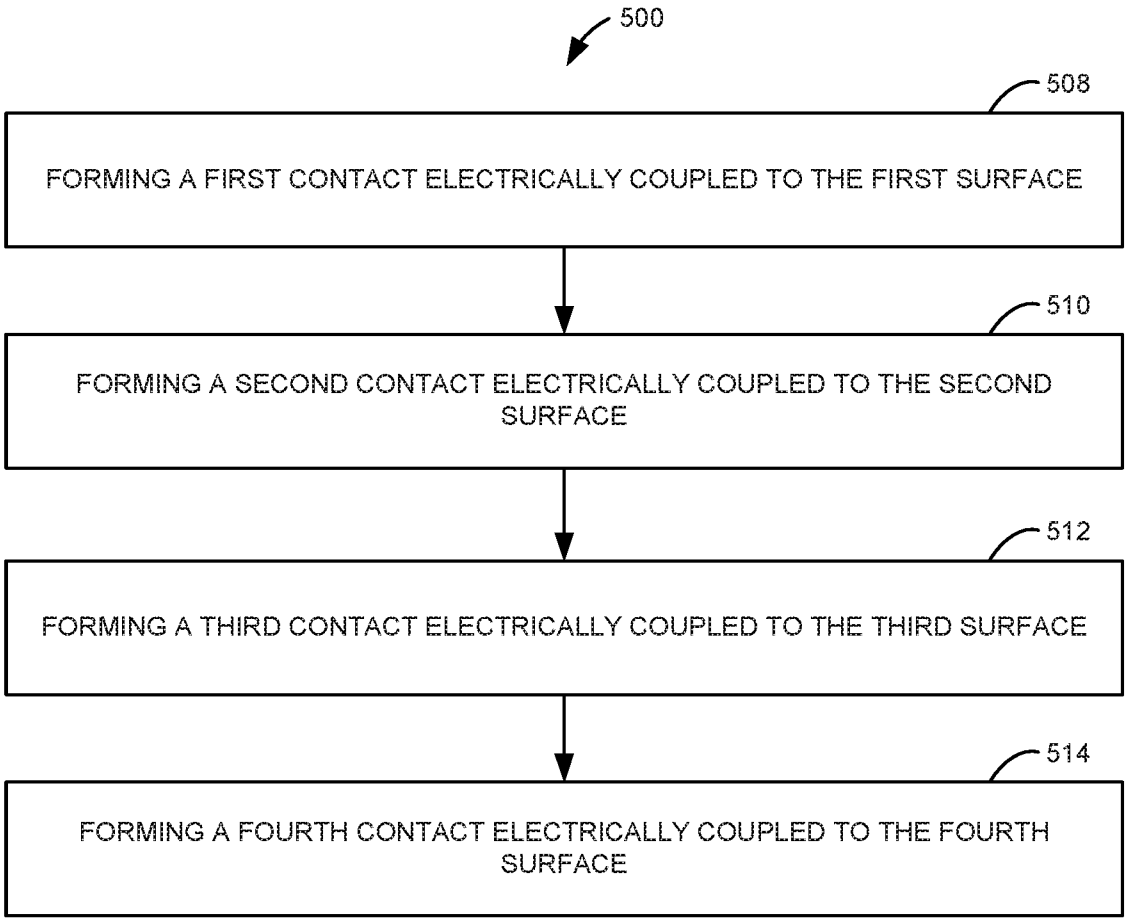

500
508
FORMING A FIRST CONTACT ELECTRICALLY COUPLED TO THE FIRST SURFACE
510
FORMING A SECOND CONTACT ELECTRICALLY COUPLED TO THE SECOND SURFACE
512
FORMING A THIRD CONTACT ELECTRICALLY COUPLED TO THE THIRD SURFACE
514
FORMING A FOURTH CONTACT ELECTRICALLY COUPLED TO THE FOURTH SURFACE

Fig. 12B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2018/047189

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/20 *(2010.01)*
H01L 31/042 *(2014.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/04, 21/18, 21/20, 21/328, 21/329, 21/68, 27/00, 27/02, 27/04, 27/08, 27/082, 31/00, 31/02, 31/0216, 31/04, 31/042, 33/00, 33/02, 33/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0241356 A1 (EPISTAR CORPORATION) 18.10.2007	1-15
A	US 2015/0371974 A1 (X-CELEPRINT LIMITED) 24.12.2015	1-15
A	US 2017/0110637 A1 (LG INNOTEK CO., LTD) 20.04.2017	1-15

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2019 (29.04.2019)	16 May 2019 (16.05.2019)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	M. Karsanova Telephone No. (499) 240-25-91