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- (71) Applicant: DECA TECHNOLOGIES, INC. [US/US];
7855 S. River Parkway STE 111, Tempe, Arizona 85284 (US).
- (72) Inventor; and
- (71) Applicant : SCANLAN, Christopher [US/US]; 350 W
Yellowstone Way, Chandler, Arizona 85248 (US).

- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
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[Continued on next page]

- (54) Title: FULLY MOLDED FAN-OUT

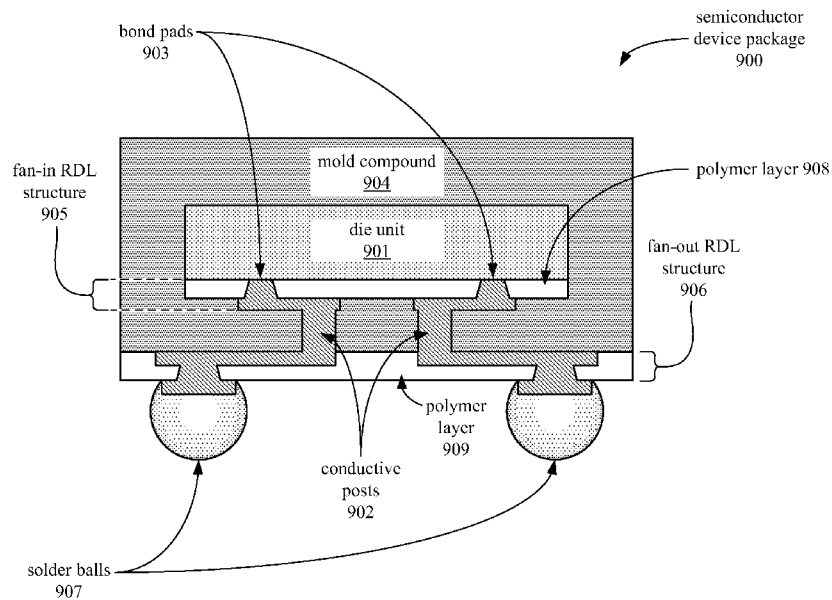
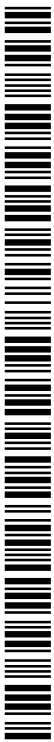


FIGURE 9

[Continued on next page]



Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

(88) Date of publication of the international search report:

18 June 2015

Published:

— *with international search report (Art. 21(3))*

(57) Abstract: A method for manufacturing a device package may include constructing a spacer element coupled with a surface of a semiconductor die unit, where the spacer element is configured to create a gap between the semiconductor die unit and a surface of a carrier, and encapsulating the semiconductor die unit within a mold compound, where the encapsulating includes introducing the mold compound into the gap.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 12/72164

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/56 (2013.01)

USPC - 257/738

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H01L 21/56 (2013.01)

USPC - 257/738

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 257/738; 257/E21.511; 257/E23.069; 438/108

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatBase; Google Patent; Google Scholar.

Search terms used: semiconduct* chip* die electron* packag* mold* epox* resin cover surround encapsulat* wafer level WLP scale WSP reconstit* wafer chip WLCSP ball grid array bga flip-chip fan out fan in SCANLAN

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2003/0092217 A1 (Coyle) 15 May 2003 (15.05.2003), FIG. 3, Fig. 5A, Fig. 5C; Para.[0028], [0033], [0037]-[0047], [0052]	1, 2, 5-7, 11-18, 20 ----- 3, 4, 8-10, 19
Y	US 2006/0275949 A1 (Farnworth et al.) 07 December 2006 (07.12.2006), Fig. 22C, para. [0143], [0157], [0294]	3, 8-10
Y	US 2011/0202896 A1 (Scanlan et al.) 18 August 2011 (18.08.2011), para. [0003], [0022], [0025], [0026]	4, 19
A	US 2003/0027373 A1 (Distefano et al.) 06 February 2003 (06.02.2003), entire reference	1-20
A	US 2011/0156250 A1 (Goh et al.) 30 June 2011 (30.06.2011), entire reference	1-20
A	US 2010/0052135 A1 (Shim et al.) 04 March 2010 (04.03.2010), entire reference	1-20
A	US 5,548,091 A (DiStefano et al.) 20 August 1996 (20.08.1996), entire reference	1-20

Further documents are listed in the continuation of Box C.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 20 April 2013 (20.04.2013)	Date of mailing of the international search report 13 MAY 2013
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 12/72164

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

-- see extra sheet

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US 12/72164

Continuation of Box No. III -- Observations where unity of invention is lacking

Group I: Claims 1-11: A method, comprising: constructing a spacer element coupled with a surface of a semiconductor die unit, wherein the spacer element is configured to create a gap between the semiconductor die unit and a surface of a carrier; and encapsulating the semiconductor die unit within a mold compound, wherein the encapsulating comprises introducing the mold compound into the gap.

Group II: Claims 12-20: A semiconductor device package, comprising: a semiconductor die unit; a plurality of conductive posts electrically coupled with one or more bond pads on an active surface of the semiconductor die unit; and mold compound substantially covering the active surface of the semiconductor die unit, wherein the conductive posts are electrically coupled by a redistribution layer (RDL) to conductive material exposed outside the mold compound.

The inventions listed in the above-mentioned groups do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Groups I and II lack unity of invention, because even though the inventions of these groups require the technical features of a structure coupled with a surface of a semiconductor die unit and encapsulating the semiconductor die unit within a mold compound, these technical features are not a special technical features as they do not make a contribution over the prior art, in view of US 2011/0156250 A1 to Goh et al., which discloses a structure coupled with a surface of a semiconductor die unit (para [0008], [0014] solder bumps on an active surface in a flip chip configuration) and encapsulating the semiconductor die unit within a mold compound (para [0014], [0018]).

Further,

Group I includes the special technical feature of a gap between the semiconductor die unit and a surface of a carrier, not found in Group II.

Group II includes the special technical feature of a redistribution layer, not found in Group I.

Groups I-II therefore lack unity under PCT Rule 13 because they do not share a same or corresponding special technical feature.