Dec. 2, 1969 G. YANISHEVSKY 3,482,239

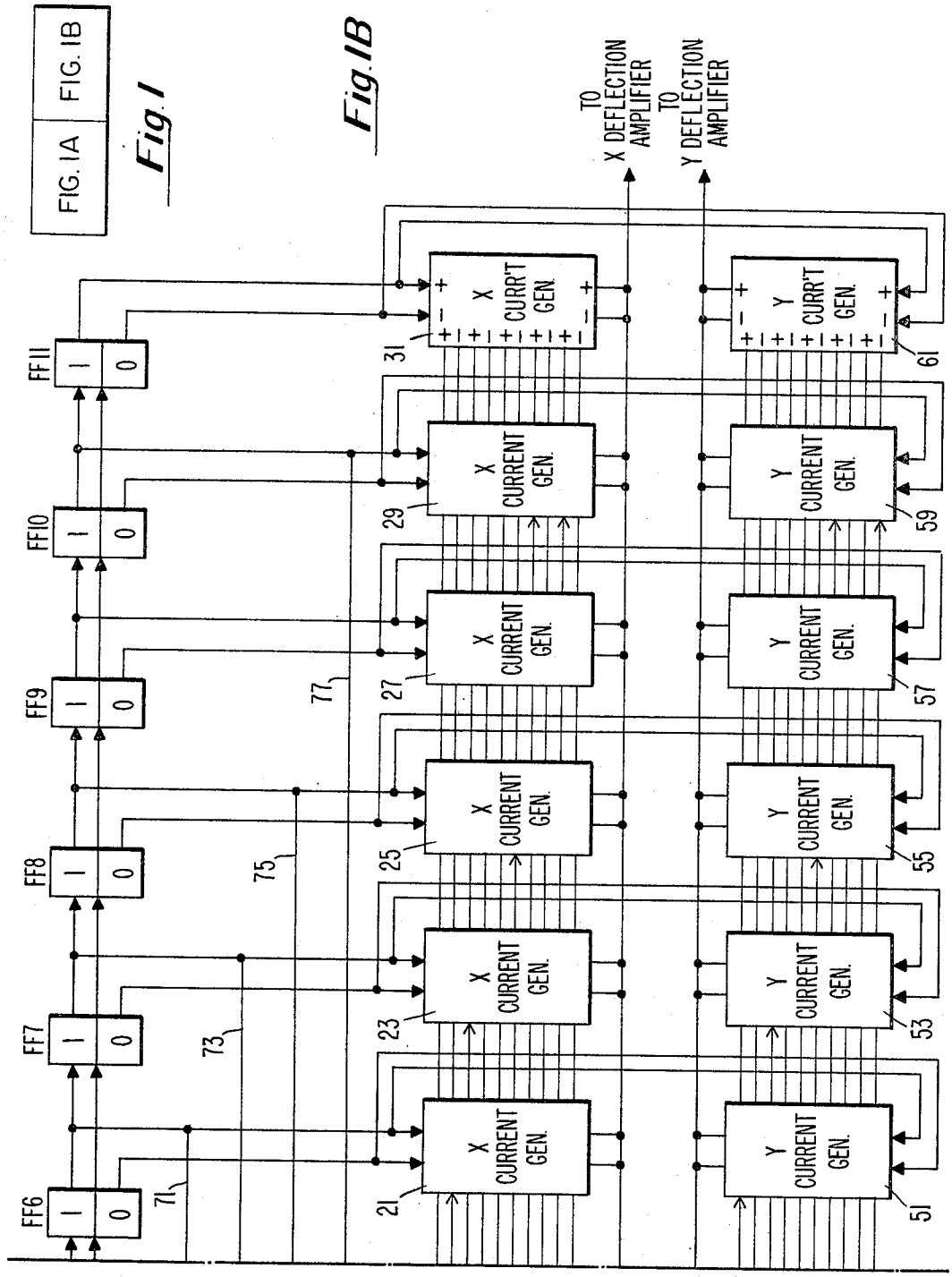
RESISTOR MATRIX SYMBOL GENERATOR

Filed May 27, 1966 5 Sheets-Sheet 1

FIG. 1A FIG. 1B

Fig. 1

Fig. 1B



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RESISTOR MATRIX SYMBOL GENERATOR

Filed May 27, 1966 5 Sheets-Sheet 2

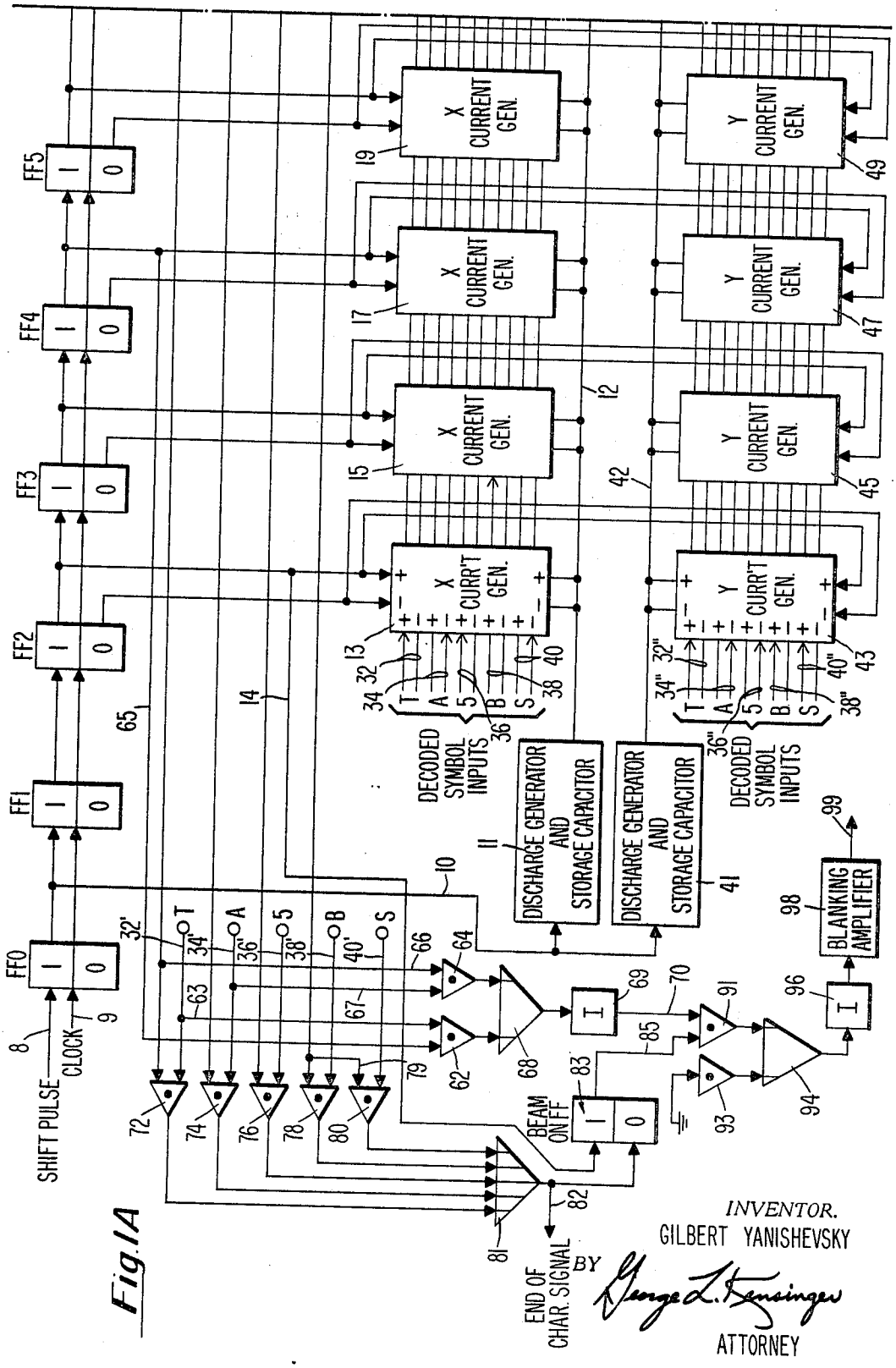


Fig. 1A

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Dec. 2, 1969 G. YANISHEVSKY 3,482,239
RESISTOR MATRIX SYMBOL GENERATOR
Filed May 27, 1966
5 Sheets-Sheet 3

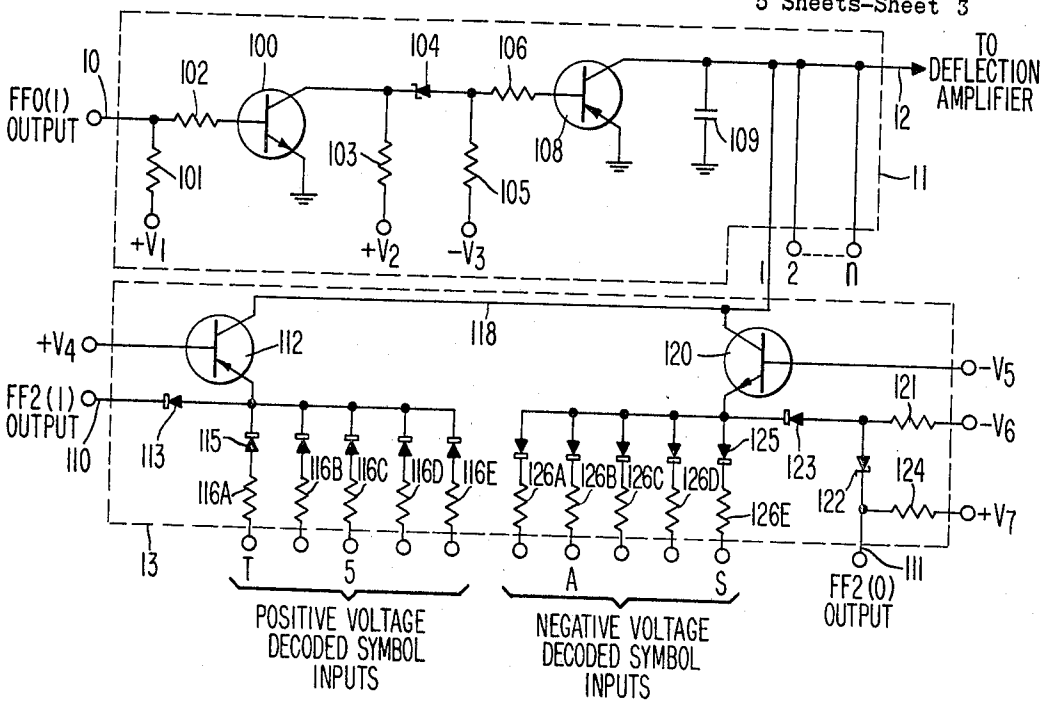


Fig. 2

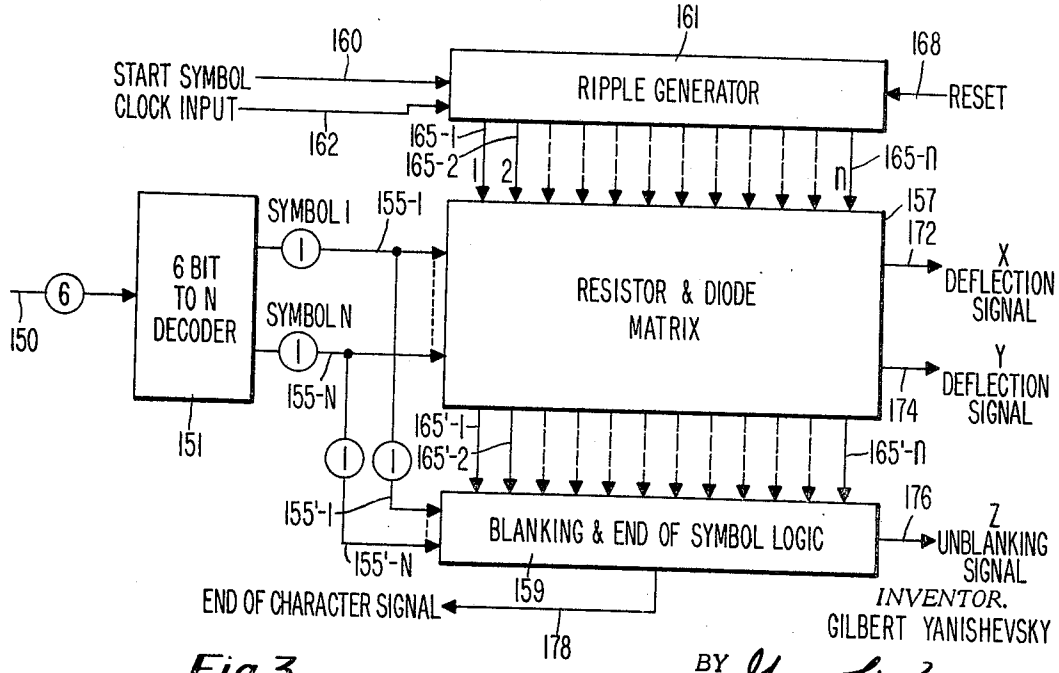


Fig. 3

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RESISTOR MATRIX SYMBOL GENERATOR

Filed May 27, 1966 5 Sheets-Sheet 4

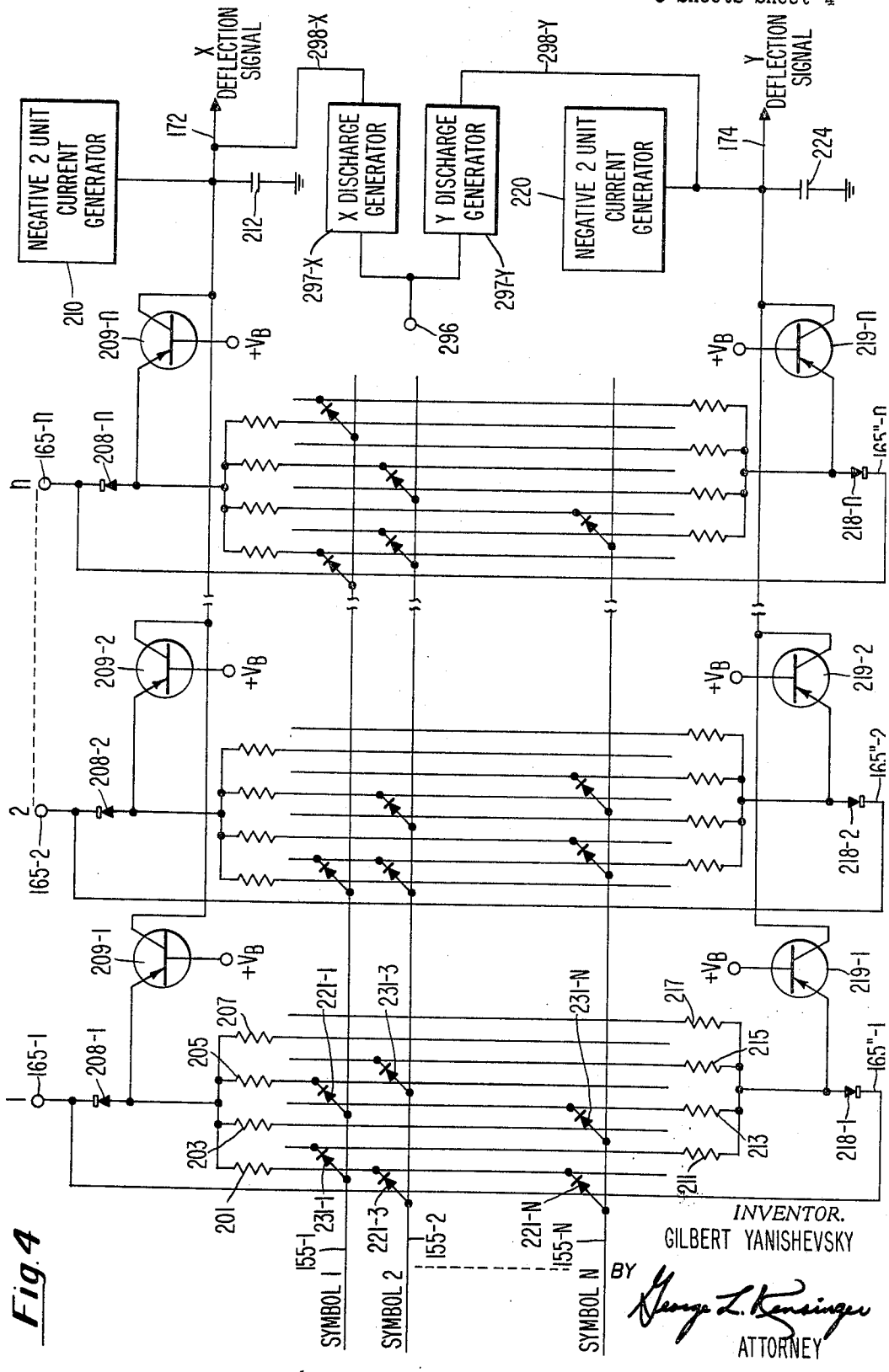


Fig. 4

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RESISTOR MATRIX SYMBOL GENERATOR

Filed May 27, 1966 5 Sheets-Sheet 5

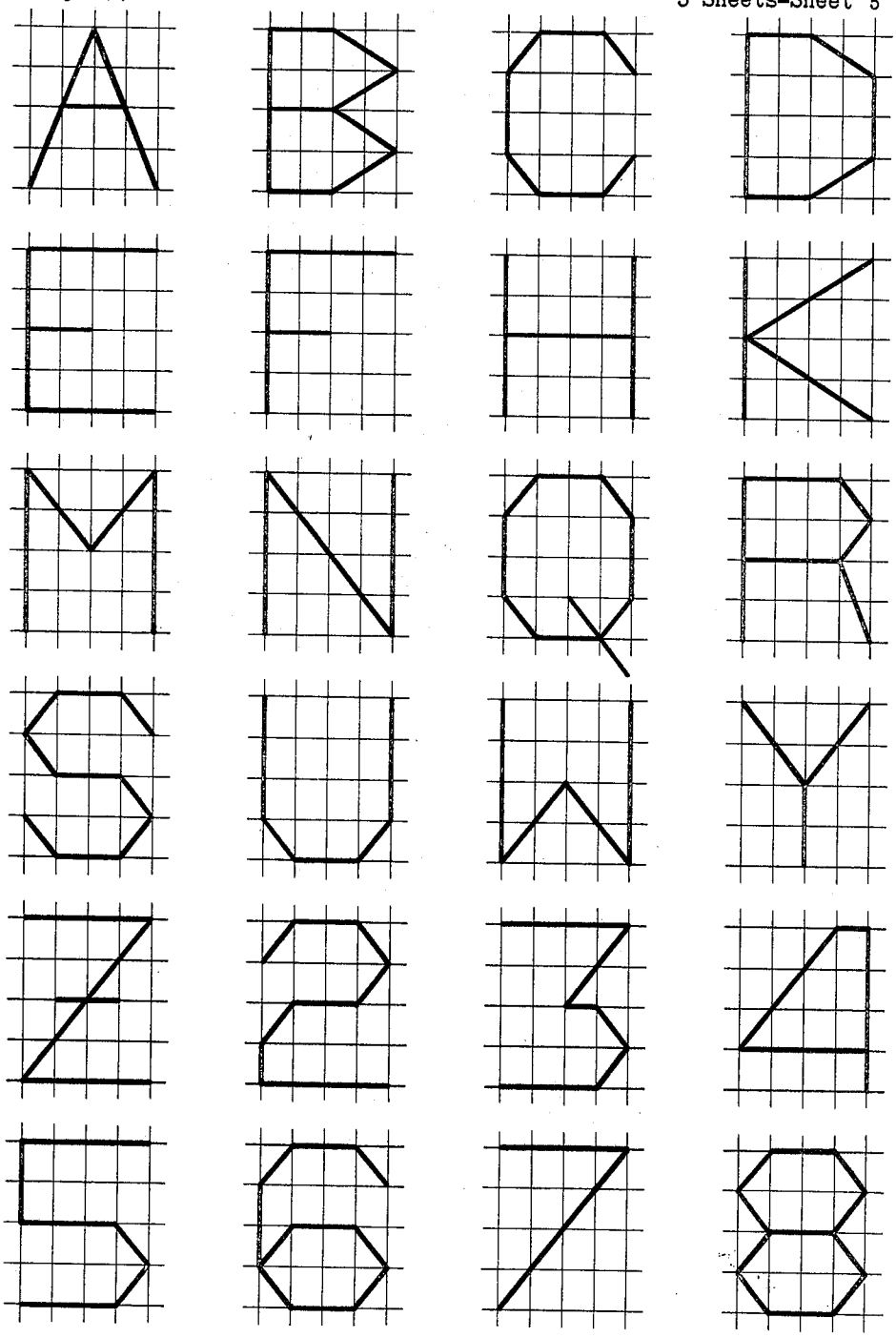


Fig.5

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3,482,239

RESISTOR MATRIX SYMBOL GENERATOR

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Filed May 27, 1966, Ser. No. 553,362
Int. Cl. G08b 23/00; H01j 29/70
U.S. Cl. 340—324 12 Claims

ABSTRACT OF THE DISCLOSURE

Resistor matrix symbol generators which include a plurality of sequentially activated stroke generators each controlled by preselected resistors or combinations of resistors to generate a signal representative of a segment of predetermined characters and symbols to be generated and displayed.

This invention relates to the generation of electrical signals for representing successive line segments of characters or symbols to be visually displayed or for defining a plurality of stylus, pointer or tool movements in apparatus such as displays or record-controlled machine tools. More specifically, the subject invention relates to the generation of electrical signals to be utilized in the visual display of line- or vector-approximated symbols or characters for displaying the output of various electronic apparatus such as electronic data processing systems.

The improvements recently made in electronic data processing systems and in various electronic communication apparatus such as input-output devices and real-time monitoring systems have increased the required operating speeds of visual displays for communicating output information. Two such visual display means are cathode ray tube displays and rectilinear coordinate plotting devices.

Various techniques of generating the character- or symbol-defining electrical signals for such display means have been developed. The generation of dot position signals from selected ones of an array or matrix of signal translating devices is utilized in various cathode ray tube displays. Another technique has utilized electrical signals for defining characters from spots or segments of a plurality of rasters as in television-type cathode ray tube displays. The dot-type matrix approximation of characters produces displays of relatively poor quality in that the outline of the generated symbols is discontinuous, making them tiresome to read. The television-type display of symbols and characters upon a field of resters is, complex and discontinuous to a certain degree, as well as being limited in its definition or resolution of the symbol forming lines.

A third technique for symbol generation utilizes line or vector generation apparatus for defining line segments for the approximation of symbol outline or form. One such technique utilizes a matrix of bistable devices such as square hysteresis loop magnetic cores. each column or row of which is designated for generating an electrical signal for a particular segment of the character or symbol to be displayed. Read-out is accomplished by resetting the cores, gating together the pulse outputs from the cores and applying the resultant current pulses to current integrating circuits for obtaining electrical signals of different durations corresponding to various lengths of line segments. This technique is subject to the disadvantage of high cost, however, due to the large number of bistable devices required and due to the high cost of fabrication and wiring, particularly when bistable magnetic cores are utilized as the bistable elements. This

technique is also complex in that it requires gating and pulse current integrating circuit means for each line segment. Switching is also slow when magnetic cores are employed and this technique requires that time be provided for both setting and resetting the cores in the generation of each symbol or character. Further disadvantages of this technique are that large switching currents are necessary if cores are utilized, particularly when it is attempted to increase the speed of switching in the generator.

Line or vector generation of symbols and characters visual display has also been accomplished by utilizing diode matrix symbol generators as described in the copending Halsted United States patent application, Ser. No. 277,796, entitled "Symbol Generating Apparatus," filed on May 3, 1963, and transistor matrix symbol generators as described in the Yanishevsky United States patent application, Ser. No. 379,936, entitled "Character Generator Apparatus Including Function Generator Employing Memory Matrix," filed July 2, 1964. Reference is also made to the copending Bacon United States patent application, Ser. No. 394,495, entitled "Complex Pattern Generation Apparatus," filed on Sept. 4, 1964. These patent applications are assigned to the assignee of the present application. These techniques are high in cost as a result of the large number of diodes or transistors required and as a result of the complexity of the gating and control circuitry required for timing and controlling the display of the character segments. Some of these line generating apparatus required the generation of signals representative of the polar angle at which the line segments were to be oriented, while others described line segments in accordance with specified ordinates and abscissas of points to which line segments were to be drawn from specified points of origin in a system of fixed rectilinear coordinate axes.

Accordingly, it is an object of the subject invention to provide simple, low cost, line-approximation symbol generating apparatus capable of high-speed operation yet requiring relatively low operating power and capable of providing electrical signals which will produce high quality character and symbol approximations in visual display systems.

Another object of the subject invention is to simplify matrix generation of electrical signals representative of character line segments in visual display apparatus for reducing the cost of such generation apparatus.

A further object of the present invention is to provide a plurality of successively operated line-segment generation means for defining symbol- or character-forming lines which requires a greatly reduced number of active elements such as transistors and diodes per generated line segment, is low in cost and power requirements and is capable of greatly increased speeds of operation.

A still further object of the invention is to generate line or vector signals for line segment approximation of symbols employing constant current swtiching with little capacitive load on drivers for greatly increasing the speed of operation of such generators and for reducing the power requirements thereof.

In accordance with the above-mentioned objects there is provided a resistor matrix symbol generator comprising a plurality of input conductors, a plurality of variable electric current stroke generators having a plurality of input terminals coupled to selected ones of the plurality of input conductors through unidirectional and resistive means of preselected magnitudes, energy storage means coupled for receiving signals from the electric current stroke generators, and timing means for successively enabling different ones of said variable electric current generators in synchronism with information signals received on said plurality of input conductors.

In one embodiment of the present invention there is provided a resistor mtarix symbol generator for generating electrical stroke signals representative of line segments for approximating the configuration of a plurality of different characters comprising a plurality of pairs of input conductors, each pair having a conductor for receiving positive encoded electrical pulses and a conductor for receiving negative encoded electrical pulses for each of said characters; a plurality of variable amplitude electrical stroke signal generators comprising positive and negative current generators each being coupled to selected ones of said positive and negative conductors of said input conductor pairs, respectively; electrical energy storage means coupled to the outputs of the positive and negative current generators of each of the variable amplitude electrical signal generators; discharge means for discharging said energy storage means; and timing pulse generating means for successively initiating operation of said variable amplitude signal generators and for periodically enabling operating of said discharge means.

In the preferred embodiment of the present invention there is provided a resistor matrix symbol generator for generating successive electrical signals representative of line segments or vectors for describing any of a plurality of different characters or symbols comprising a plurality of input signal conductors each being assigned to a different symbol to be described; a plurality of variable electric current stroke generators having a plurality of input circuits for receiving character input signals, different input circuits causing different levels of conduction in said current generators upon receiving an input signal; unidirectional means coupling selected ones of said input signal conductors to at least one of said input circuits of said variable current stroke generators; electric energy storage means coupled to the output terminal of each of said variable current stroke generators; constant current generation means coupled to the junction of said variable current generators and said energy storage means; and timing means coupled to each of said variable current generators for successively enabling conduction of said current generators in synchronism with the desired rate of development of stroke signals.

Reference is made to each of the above-identified patent applications for definition of terms used in the present patent application and for the disclosure therein of the manner of and of means for connecting symbol generating apparatus in cathode ray tube display systems. Reference is also made to an article by Charles Halsted appearing in the April 1966 issue of Electronic Industries magazine at pages 62 through 66, for an explanation of the terminology and of the mechanics and techniques of the display of characters and symbols from electrical signals in various display systems. Reference thereto is also made for the details of the manner of approximating symbols by line segments in visual displays and for details of the manner of connecting symbol generators analogous to those of the present invention to cathode ray tube visual displays in display or subscriber systems and in various visual monitoring systems.

Further objects and advantages of the present invention will be appreciated from a reading of the following detailed description of the invention with reference to the accompanying drawings, wherein:

FIGURE 1 is a format diagram illustrating the manner in which the drawings of FIGURES 1A and 1B are to be fitted together to form a block diagram of a resistor matrix symbol generator according to the subject invention;

FIGURE 2 is an electrical schematic circuit diagram of a variable amplitude electric current generator and of a discharge generator and storage capacitor of the resistor matrix symbol generator illustrated in FIGURE 1;

FIGURE 3 is a schematic block diagram of a preferred embodiment of the resistor matrix symbol generators of the subject invention;

FIGURE 4 is an electrical schematic circuit diagram of the resistor matrix symbol generator illustrated in FIGURE 3; and

FIGURE 5 is an illustration of selected symbols and characters formed by the line approximation technique of the subject invention.

Referring more specifically to the schematic block diagram of FIGURE 1, as formed by fitting together the drawings of FIGURES 1A and 1B, a resistor matrix symbol generator is illustrated having a plurality of pairs of input conductors **32** through **40** for receiving electrical signals representative of characters or symbols to be displayed. A positive pulse signal and a negative pulse signal are applied to different ones of the conductors of a selected symbol or character input conductor pair for initiating the generation of electrical signals for describing a selected character. The positive and negative character pulse signals are also applied to terminals **32'** through **40'** for the selective enabling of the blanking control decoding gates **62** and **64** and the end of character decoding gates **72** through **80** for aiding the development of character-describing signals. Only one polarity of each of the character input signal pairs need be applied to gates **62**, **64** and **72** through **80**, the choice between the positive or the negative of each of the character input signal pairs depending upon the polarity of signals required for opening these gates.

A plurality of variable amplitude X current stroke generators **13** through **31** having a plurality of pairs of positive and negative input terminals are coupled to either the positive or negative conductor of selected ones of input conductor pairs **32** through **40**. The outputs of the X current generators establish the abscissas of the line segments generated for each of the characters in a system of fixed rectilinear ordinates. Each of the X current generators is comprised of a positive and a negative current generator, an enabling control terminal, positive and negative input circuits, and positive and negative output terminals respectively, as will be described later with reference to FIGURE 2. Each of the character input conductor pairs is connected to only as many of the current generators as is necessary for completely describing the configuration of the associated character.

The connection of the character input conductors to only certain ones of the current generators is illustrated in FIGURE 1 by the use of an arrowhead on one of each of the conductor pairs at either the positive or the negative terminals of the first and the last current generators that is required for generating each of the representative characters. For example, the T input conductor pair is connected to each of the X current generators **13**, **15**, **17**, **19** and **21** but not to the remainder of them. The A input conductor pair is connected to each of the conductors **13** through **23** but not to the remainder. The 5 input conductor pair is connected to X current generators **13** through **25**. The B input conductor pair is connected to each of the X current generators **15** through **29** and the S input conductor pair is connected to X current generators **13** through **29**. None of the character or symbol input conductor pairs illustrated are connected to the last X current generator **31**. Accordingly, the end of character signal for the T symbol is taken on conductor **71** from the enabling input conductor of X current generator **21**, the end of character control signal for the A character is taken on conductor **73** from the enabling conductor of X current generator **23**, the end of character control signal for the 5 character on conductor **75** connected to the enabling conductor of X current generator **25**, and the end of character signal for the B and S characters are taken on conductors **77** and **79**, respectively, from the enabling input conductor to X current generator **29**. These end of character sig-

nals are delivered respectively, to end of character decoding AND gates **72** through **80**, as shown.

A similar plurality of variable amplitude Y current stroke generators **43** through **61** each including positive and negative current generators are provided for the Y-component or ordinate in a system of rectilinear coordinates of the line segments representative of the character or symbol configurations to be displayed. The Y current generators **43** through **61** have a plurality of positive input terminals, an enabling terminal and an output terminal for each positive current generator and a plurality of negative input terminals, an enabling and an output terminal for each negative current generator as do the X current generators. Likewise, one of each of the character input conductor pairs is connected to as many of the Y current generators **43** through **61** as is necessary for defining all of the character line segments. Only Y current generators **43** through **51** are required for forming the T symbol, Y current generators **43–53** being required for the A signal, Y current generators **43–55** being required for the 5 symbol, and Y current generators **43–59** being required for defining the line segments for the B and S symbols. Y current generator **61** is not utilized for forming any of the representative characters of FIGURE 1.

A shift register or ripple generator composed of flip-flops FF0 through FF11 is connected for receiving shift pulse control signals on input conductor **8** and clock pulse signals on input conductor **9** and for providing successive enabling signals to the current generators. The "one" side of flip-flop FF0 is connected to conductor **10** for delivering a control signal to discharge generators and storage capacitors **11** and **41** for discharging the storage capacitors prior to the forming of each new character or symbol. The output of the flip-flop FF1 is used only to trigger flip-flop FF2, the switching period of FF1 thus allowing additional time for the discharge of the storage capacitor.

The "one" and "zero" output of flip-flop FF2 are supplied to the positive and negative enabling terminals, respectively, of the X and Y current generators **13** and **43** and the "one" and "zero" outputs of each of the succeeding flip-flops FF3 through FF11 are connected to the positive and negative enabling terminals respectively, of X current generators **15** through **31** and Y current generators **45** through **61**. Both the positive and the negative output terminals from each of the X current generators **13** through **31** are connected to conductor **12** which is connected to discharge generator and storage capacitor **11** for developing electrical ramp signals for controlling the X deflection of a beam or pointer in a display system. Both the positive and the negative output terminals of the Y current generators **43** through **61** are connected to conductor **42** which is connected to discharge generator and storage capacitor **41** for supplying electrical ramp signals for Y deflection control in visual display means. The outputs from flip-flop FF1 are not separately utilized in order to provide two clock pulse times in which to effect discharging of the storage capacitors by the output of flip-flop FF0 via conductor **10** so that the initial starting point of the line segments generated by the current generators will be at reference potentials which may be independently supplied to the conductors **12** and **42**.

Referring more particularly to the electrical schematic circuit diagram of FIGURE 2, representative variable amplitude electric current generator **13** is shown electrically connected by conductor **118** to representative discharge generator and storage capacitor **11**, the discharge generator and storage capacitor having a plurality of additional input terminals **2** through *n* for connection to the remainder of the X current generators of the symbol generator of FIGURE 1. Consistent with the showing in FIGURE 1, the X current generator **13** receives enabling inputs from the "one" and "zero" outputs of flip-flop FF2 at terminals **110** and **111**, respectively, and receives inputs from selected ones of the character input conductors. The discharge generator and storage capacitor **11** likewise is controlled by the "one" output of flip-flop FF0 via conductor **10** and provides its output on conductor **12** for providing X deflection control in a visual display system.

The X current generator **13** is comprised of a positive and a negative current generator. The positive current generator consists of a PNP transistor **112**, the emitter of which is connected to the anode of diode **113**, the cathode of which is connected to terminal **110** for receiving enabling signals from the "one" output of flip-flop FF2, and to the cathode of diodes **115**, the anodes of which are connected to different resistors **116**A through **116**E, respectively, for receiving positive voltage decoded character input signals. The negative current generator consists of an NPN transistor **120**, the emitter of which is connected to the cathode of diode **123** and to the anodes of diodes **125**, the cathodes of which are connected to different input resistors **126**A through **126**E, for receiving negative voltage decoded symbol input signals. The positive and negative current generators are coupled at the collectors of the transistors and connected by conductor **118** to discharge generator and storage capacitor **11** at the junction of conductor **12** and one plate of capacitor **109**. The anode of diode **123** is connected to one end of resistor **121**, the other end of which is connected to reference voltage $-V_6$ and to the anode of reference diode **122**. The cathode of reference diode **122** is connected to one end of resistor **124**, the other end of which is connected to reference potential $+V_7$, and to terminal **111** for receiving enabling signals from the "zero" output of flip-flop FF2. The base of positive current generating transistor **112** is connected to reference potential $+V_4$ and the base of negative current generating transistor **120** is connected to reference potential $-V_5$. Representative character input signals for the T and the 5 symbols are provided to the positive current generator input circuit and representative character input signals for the A and S symbols are applied to the input circuit of the negative current generator.

The discharge generator consists of an NPN transistor **100** connected in cascade with a PNP transistor **108**, the collector of which is connected to one plate of grounded storage capacitor **109** and to output conductor **12**. Control signals from the "one" output of flip-flop FF0 are received on conductor **10** which is connected to resistors **101** and **102**. The other end of resistor **101** is connected to reference voltage $+V_1$; the other end of resistor **102** is connected to the base of transistor **100**. The collector of transistor **100** is coupled to reference potential $+V_2$ through resistor **103** and to the cathode of reference diode **104**. The anode of reference diode **104** is coupled to reference potential $-V_3$ through resistor **105** and to the base of transistor **108** through resistor **106**. The emitters of both transistors **100** and **108** are grounded, as is the second plate of capacitor **109**.

The value of each of resistors **116** and **126** of the positive and negative current generators is selected to limit the current in the transistor to which it is connected to a level which corresponds to a particular line segment length upon receiving a character input signal. There may be a separate resistor **116** and diode **115** connected to each of the X and Y positive current generators and a separate resistor **126** and diode **125** connected to each of the X and Y negative current generators for each character to be described or one or more of the resistor and diode input circuits of the generators may be shared by several characters which require the same line-representing electric current from the associated generator. It is also noted that since both groups of the current generators shown in FIGURE 1 are operated successively with only one current generator in each group conducting at any instant of time, the number of positive current generator and negative current generator transistors may be greatly reduced. One

transistor of proper rating may be utilized for all of the positive X current generators and one such transistor could serve for all of the negative X current generators. A similar reduction in the number of transistors employed may be accomplished in the positive and negative Y current generators.

The application of a positive voltage decoded symbol input causes the transistor **112** to conduct and add positive charge to storage capacitor **109**, thus resulting in a positive-going electrical ramp signal on output conductor **12**. The application of a negative voltage decoded symbol input causes representative negative current generating transistor **120** to conduct and charge storage capacitor **109** negatively and thereby provide a negative-going electrical ramp signal on output conductor **12** for deflection control in visual display means. Although any input signal applied to the input conductors **32** through **40** and the corresponding conductors **32''** through **40''** appears upon an input terminal of all of the current generators to which it is connected, only the X and Y positive current generators receiving an enabling signal from the "one" output of a triggered shift register flip-flop will conduct, and only one X and one Y negative current generator will be enabled by the "zero" output of the same flip-flop. The application of an input signal level on one of the character input conductor pairs causes successive electrical ramp signals to be developed on output conductors **12** and **42** as storage capacitors **11** and **41** are successively charged positively or negatively as successive X and Y current generators are enabled by the clock pulse signals.

Each successive current stroke generator which is connected for receiving the applied charatcer input signal conducts and causes the charge on the storage capacitor to which it is connected to change either positively or negatively. Both storage capacitors maintain as the base potential level for the succeeding line segment electric signal the level of energy storage established therein by each current generator until a succeeding current generator is operated or the capacitors are discharged. In this manner the output voltages developed on conductors **12** and **42** are stepped in potential by each successive clock pulse without returning to zero potential whereby a full range of characters, symbols and other configurations can be described by the generated electrical signals. The application of a control signal to the discharge generators through conductor **10** removes any remaining charge on the storage capacitors atfer generation of each character. The storage capacitors are therefore fully discharged between the generation of successive characters. It is noted that the size of the storage capacitors is dependent upon the chosen magnitude of the charging currents and upon the frequency of operation of the symbol generator.

A blanking control signal is generated by the apparatus of FIGURE 1 through the operation of Beam On flip-flop **83** and blanking control decoder AND gates **62** and **64**. In such a blanking scheme the visual indicator of a display system is normally blanked or disabled and is rendered visible for each character by a signal from the "one" output of flip-flop FF2 through conductor **14** which sets the Beam On flip-flop **83** and enables AND gate **91** through conductor **85**. The other input to AND gate **91** on conductor **70** initially renders the gate conductive until AND gate **62** or **64** is opened and OR gate **68** and inverter **69** are operated. The output level of gate **91** is transmitted through OR gate **94** and inverted by inverter **96** before being applied to blanking amplifier **98** and subsequently to the blanking controls of a display means. The display beam is initially held blanked by grounded input gate **93** which is connected to an input of OR gate **94** and is unblanked or made visible upon the setting of Beam On flip-flop **83** by a control signal from the "one" output of flip-flop FF2 for each character to be described.

A visual display indicator can be blanked temporarily by opening AND gate **62** or **64**, or can be blanked indefinitely by resetting Beam On flip-flop **83**. The reset terminal of flip-flop **83** is coupled through OR gate **81** to the output terminals of AND gates **72** through **80**, the input terminals **32'** through **40'** of which are connected to receive the corresponding character input signals and to receive the enabling signals of the last current generator utilized for the corresponding characters through conductors **71**, **73**, **75**, **77** and **79** respectively. The opening of one of the gates **72** through **80** provides an end of character signal on conductor **82** through OR gate **81** as well as resetting the Beam On flip-flop **83** and indefinitely blanking the display beam through gates **91** and **94**, inverter **96** and blanking amplifier **98**. The display beam is temporarily or momentarily blanked while retracing or repositioning the display beam or indicator by connecting the inputs of an AND gate **62**, **64** to the character input signal and to the "one" output of a selected one of the shift register flip-flops. The outputs of representative blanking control decoding AND gates **62** and **64** which correspond, respectively, to blanking for the T symbol and the A symbol are connected through OR gate **68** and inverter **69** to an input terminal of AND gate **91** through conductor **70**. The opening of one of the blanking control decoding AND gates **62** or **64** produces a signal which is inverted in element **69** for disabling AND gate **91** during the period of a clock pulse.

It is noted that blanking control can also be performed in the symbol generator of FIGURES 1 and 2 by the blanking techniques disclosed in the above-identified Yanishevsky, Halsted or Bacon patent applications or other techniques known in the art. Also, multilevel blanking control may be accomplished in the apparatus of FIGURE 1 by providing a third set of current generators having resistor and diode input circuits for receiving input signals from conductors **32** through **40** or **32''** through **40''** and having terminals for receiving enabling control signals from the shift register flip-flops. The blanking signal generators could each consist of only one current generator of a chosen polarity since two polarities of blanking are not required. Both positive and negative current generators could be utilized however, if greater flexibility and range of blanking control signals is desired. By proper selection of the magnitude of the resistors in the input circuit, a wide range of levels of blanking could be provided for compensating for different writing speeds which result from writing line segments of different lengths in a display during uniform periods of time. The outputs of such blanking control signal generators would be connected to an output conductor for providing signals to control the intensity of the display indication of display means.

The number of different length of line segments that are generated, and therefore the degree of approximation of character and symbols as well as the size of the symbol repertoire that may be attained is limited by the number of current generators that are utilized. The apparatus shown may be modified for increasing the symbol repertoire or describing more complex configurations by adding additional X and Y current generators, additional corresponding flip-flops in the shift register, and different input resistors to the current generators. This adaptability provides extreme flexibility of the resistor matrix symbol generator of the subject invention.

FIGURE 3 illustrates a schematic block diagram of the preferred embodiment of the resistor matrix symbol generator of the present invention. In this embodiment, a Resistor & Diode Matrix **157** is connected for receiving character input signals on input conductors **155–1** through **155–N** and for providing X deflection and Y deflection signals on output conductors **172** and **174**, respectively. These signals correspond to successive line segments for describing the characters of the repertoire upon being enabled by signals on conductors **165–1** through **165–*n***. The character input signals supplied on conductors **155–1** through **155–N** may be developed by decoder **151** from input pulse groups received on input conductors **150**. These character input signals are supplied to Resistor & Diode Matrix **157** via conductors **155–1** through **155–N**

and to Blanking & End of Symbol Logic **159** via conductors **155'–1** through **155'–N**.

The blanking and end of symbol logic produces successive unblanking signal levels on output conductor **176** upon being successively enabled by signals received on conductors **165'–1** through **165'–*n*** and produces an end of character signal on conductor **178** upon decoding an end of character condition for any of the input character signals. The enabling signals provided to both the resistor and diode matrix and the blanking end of symbol logic are provided by Ripple Generator **161**, the operation of which is enabled by a start signal on conductor **160** and is successively stepped by clock signals on conductor **162**. The ripple generator can be reset by application of a control signal to reset terminal **168** to which the end of character signal developed on conductor **178** is applied.

The Resistor & Diode Matrix **157** of FIGURE 3 illustrated in detail in the electrical schematic circuit diagram of FIGURE 4. In this figure are illustrated current stroke generators for producing electrical signals corresponding to the first, second and *n*th. line segments for describing the characters and symbols. The X current stroke generator of the first segment consists of PNP transistor **209–1** and four input circuits consisting of resistors **201, 203, 205** and **207** one or more of which may be connected by one of diodes **221–1** through **221–N** to the character input conductors **155–1** through **155–N**, and is enabled by a signal on conductor **165–1** through diode **208–1**. The Y current stroke generator for the first character segment consists of PNP transistor **219–1**, the emitter of which is connected to one end of input resistors **211, 213, 215** and **217**, one or more of which may be connected by one of diodes **231–1** through **231–N** to selected ones of the character input conductors **155–1** through **155–N** and is enabled by a signal on conductor **165'–1** through diode **218–1**.

Similarly, the second X current stroke generator consists of PNP transistor **209–2** having a plurality of parallel input resistors connected to the emitter thereof and being enabled by a signal on conductor **165–2** through diode **208–2**. The Y current stroke generator for the second character segment consists of PNP transistor **219–2** having input resistors connected to the emitter thereof and being enabled by a signal on conductor **165''–2** through diode **218–2**. And lastly, the *n*th. segment X current generator consists of PNP transistor **209–*n*** having a plurality of input resistors and being enabled by a signal on conductor **165–*n*** through diode **208–*n*** and the *n*th. stroke Y current generator consists of transistor **219–*n*** having a plurality of input resistors and being enabled by a signal on conductor **165''–*n*** through diode **218–*n***. The collectors of each of the X current generating transistors **209–1** through **209–*n*** are electrically connected to output conductor **172**, to one side of grounded storage capacitor **212** and to the output terminal of negative current generator **210**, for supplying X component or abscissa electrical deflection control signals for display means. The collectors of each of the Y current generating transistors **219–1** through **219–*n*** are electrically connected to output conductor **174**, to one plate of grounded storage capacitor **224** and to the output of negative current generator **220** for developing electrical deflection control signals for the Y component or ordinate of each of the character line segments. The base electrode of the transistors **209–1** through **209–*n*** and **219–1** through **219–*n*** are coupled to reference potential $+V_B$ and the other plate of the storage capacitors **212** and **224** are grounded.

Also electrically connected to the X storage capacitor is X Discharge Generator **297–X** through **298–X** which is shown connected to output conductor **172**. The Y storage capacitor **224** is similarly electrically connected to Y Discharge Generator **297–Y** through conductor **298–Y** which is shown connected to the output terminal of Negative Current Generator **220**. These discharge generators are both actuated before, or immediately upon receiving, each character input signal for discharging the storage capacitors. The common control circuit **296** of the discharge generators may be connected to conductor **160** of FIGURE 3 for receiving the start symbol simultaneously with the Ripple Generator **161**, if desired. The discharge generators may be circuits similar to the discharge generator disclosed in FIGURE 2, or may be any of the capacitor discharge circuits well-known in the art.

In the operation of the resistor matrix symbol generator of FIGURES 3 and 4, character input pulse groups received on conductors **150** are decoded by six-bit decoder **151** which may be any of the decoders well-known in the art. The decoded character signal is applied on one of conductors **155–1** through **155–N** to the Resistor & Diode Matrix **157** and through one of input conductors **155'–1** through **155'–N** to Blanking and End of Symbol Logic **159**. A start signal is supplied through conductor **160** to Ripple Generator **161** which may be any of the clocked generators or shift registers well-known in the art. The ripple generator is stepped by clock signals on conductor **162**, successively energizing conductors **165–1** through **165–*n*** which successively enables transistors **209–1** through **209–*n*** and transistors **219–1** through **219–*n***. Transistors **209–1** and **219–1** will conduct upon the receipt of a character input signal on one of conductors **155–1** through **155–N** and an enabling signal on conductor **165–1** if one or more diodes connect the former to one or more of emitter resistors **201** through **207** and resistors **211** through **217**, respectively. Each of the illustrated symbol lines 1 through N are shown having a diode connected to one of the emitter resistors of the transistor **209–1** and to one of the emitter resistors of transistor **219–1** which therefore will conduct currents to output conductors **172** and **174**, respectively, as may be seen from FIGURE 4.

Also connected to output conductors **172** and **174** are Negative 2 Unit Current Generators **210** and **220**, respectively, and grounded storage capacitors **212** and **224**. These negative current generators continuously supply a negative current of two units magnitude on the output terminals thereof and tend to charge the associated storage capacitors negative with respect to ground. Emitter resistors **201** through **207** of transistor **209–1**, and similarly, emitter resistors **211** through **217** of transistor **219–1**, are selected for conducting one, two, three and four units of current, respectively, through the associated transistor upon receiving an input character signal through one of diodes **221–1** through **221–N** and one of diodes **231–1** through **231–N**, respectively. The current in output conductors **172** and **174** conducted by transistors **209–1** through **209–*n*** and transistors **219–1** through **219–*n*** respectively, is opposed by the currents produced by the Negative 2 Unit Current Generators **210** and **220**. Thus, the receipt of a character input signal results in a net current on conductors **172** and **174** between minus two units of current and plus two units of current, depending upon which input resistors couple the selected character input conductor to the conducting transistors. These resultant currents on output conductors **172** and **174** charge the associated storage capacitors **212** and **224** either positively or negatively depending on the polarity of the current and produce electrical ramp signals whose shapes are determined by the effective RC time constants of the circuits. The amplitude of the ramp signals, which are proportional to the current magnitudes, determine the length of the line segment displayed.

The next clock pulse shifts Ripple Generator **161** and enables transistors **209–2** through conductor **165–2** and **165'–2**, respectively. The conduction of current in one or the other or both of these transistors causes the charge established on storage capacitors **212** and **224** by the conduction of the previous pair of transistors to be changed in accordance with the values of the emitter resistors which are coupled to the selected character input conductor. As shown, the I symbol line **155–1** at the second line

segment position is not connected to any of the emitter resistors of transistor **209–2** and conductor **155–N** is not connected to any emitter resistor of transistor **219–*n***. The enabling of successive pairs of transistors by Ripple Generator **161** will cause the successive generation of electrical ramp signals on output conductors **172** and **174** for X component or abscissa and Y component or ordinate deflection control is visual display means.

It is important to note that fewer emitter input resistors could be utilized in the matrix of FIGURE 4 since only the resistor values corresponding to one, two and three units of current need be supplied provided that more than one emitter resistor may be connected by a diode to certain of the character input conductors. In this manner, net output currents on output conductors **172** and **174** of the magnitudes of minus two, minus one, zero, plus one, plus two, plus three, and plus four units could be readily supplied if additional current magnitudes were desired for representing additional line segment lengths. It is also noted that since only one of transistors **209–1** through **209–*n*** and only one of transistors **219–1** through **219–*n*** conduct at any one instant of time, one transistor of proper rating could be utilized for all of the X current generators and one transistor could be utilized for all of the Y current generators. The size of the storage capacitor is dependent upon the selected magnitude of the charging currents in the circuit and upon the generator frequency which is determined by the recycling or symbol "refreshing" requirements of the display system.

Unblanking control and end of symbol detection in the resistor matrix symbol generator of FIGURE 3 may be accomplished by the techniques illustrated in the above-identified Yanishevsky, Halsted, or Bacon United States patent applications or may be effected by the blanking control technique illustrated in FIGURE 1 of the present patent application. Multilevel unblanking control and end of symbol detection may also be effected in the resistor matrix symbol generator of FIGURE 3 by the use of a third matrix of current generators having transistors corresponding to transistors **209–1** through **209–*n*** or **219–1** through **219–*n***. The transistors of the third matrix would be enabled by signals on input enabling conductors **165'–1** through **165'–*n*** and would receive character input signals on conductors **155–1** through **155–N**. A negative current generator would not be required for the unblanking control signal generator matrix since negative levels of blanking are not required, although a negative current generator could be utilized for increasing the number of levels of unblanking signals that are generated. Successive unblanking signal levels would be produced on output conductor **176** in synchronism with the X and Y deflection signals on output conductors **172** and **174** by such a matrix unblanking signal generation circuit. Each of input conductors **155'–1** through **155'–N** would be gated to one of the enabling control signals on conductors **165'–1** through **165'–*n*** for providing the end of character signal for each of the characters at appropriate clock times on output conductor **178**. The end of character signal would be applied to reset terminal **168** of the ripple generator for placing the resistor matrix symbol generator in condition for receiving a succeeding character input signal.

FIGURE 5 illustrates the configuration of representative characters and numerals which may be described by electrical signals produced by the preferred embodiment of the resistor matrix symbol generator of the invention shown in FIGURES 3 and 4. As may be seen from a careful study of FIGURE 5, each of these symbols is represented by a plurality of line segments having X component or ordinate units of either minus two, minus one, zero, plus one, or plus two and Y component or ordinate magnitudes of minus two, minus one, zero, plus one, or plus two. Of course, the vertical line segments are produced by a Y component or ordinate electrical signal only and horizontal segments are produced by X component or abscissa electrical signals only. The various diagonal segments are produced by appropriate combinations of X component or abscissa and Y component or ordinate electrical line segment-representing signals. Many other symbols, including characters, numerals or other configurations, may be represented by electrical signals produced by the resistor matrix generators of the subject invention and may be displayed on visual display means receiving signals therefrom. Also, additional line segment lengths may be provided if necessary for such additional configurations.

It is noted that the resistor matrix stroke generators of the subject invention need not include any energy storage means such as the storage capacitors illustrated in FIGURES 1, 2 and 4 if it is not necessary to maintain potential levels at the output of the generation apparatus between the generation of the successive stroke signals for reflecting the previously generated stroke signals. It is also noted that more than one of each of the current generators employed in the resistor matrix stroke generation apparatus of the invention may be made to conduct at the same time if it is desired to produce an output stroke signal which comprises cumulative signals of more than one of the current generators. It is also to be noted that the input circuits connected to each of the current generators and to the different input terminals thereof may be assigned substantially identical values of impedance and that more than one of the input circuits of any of the current generators may be connected to any of the character or symbol input selection conductors. It is further noted that the input circuits of the current generators employed in the matrix symbol and character generation apparatus of the subject invention may be characterized as being primarily of capacitive or inductive, as well as being of resistive impedance, in which cases the output stroke signals would be derived or sampled from an AND gate the inputs of which would be coupled for receiving signals from the current generators and a short strobing or sampling signal, for example.

I claim:

1. Impedance matrix symbol generation apparatus comprising:

a plurality of input conductors;

a different variable electric current generator for each successive stroke to be generated, each generator having a plurality of input terminals and an output terminal;

a plurality of unidirectionally conductive circuit means of preselected impedance values electrically coupling the input terminals of the stroke generators to selected ones of said input conductors;

stroke signal output means including storage means electrically coupled to the output terminals of all of said stroke generators; and

timing means coupled to each of said electric stroke generators for successively enabling conduction of selected ones of said stroke generators for the symbol to be generated.

2. The impedance matrix symbol generation apparatus of claim **1** wherein the circuit means each have predetermined resistance values and the variable electric current generators provide signals on the output terminals thereof responsive to the resistance of the corresponding circuit means.

3. The symbol generation apparatus of claim **2** characterized in that the resistance values of the circuit means electrically coupling the input terminals of the current generators to the input conductors have different multiples of a preselected value of resistance and the circuit means include series connected unidirectionally conductive devices therein.

4. The impedance matrix symbol generation apparatus of claim **1** further comprising means for generating unblanking signals on at least one output terminal thereof, coincident with the generated stroke signals, having a plurality of unblanking control means electrically coupled

to selected ones of said input conductors and to said timing means for being operated thereby.

5. The symbol generation apparatus of claim 4 further comprising means for generating an end-of-character signal upon the last stroke of each symbol effective to reset the timing means and thereby shorten the symbol generating period.

6. Resistor matrix symbol generation apparatus comprising:

a plurality of pairs of input conductors, each pair having a conductor for receiving positive encoded electrical selection signals and a conductor for receiving negative encoded electrical selection signals;

a different variable amplitude electrical signal generator for each successive stroke to be generated, having positive current generating means and negative current generating means each controlled by different resistors, the input terminals thereof being electrically coupled to selected ones of the positive signal input conductors and of the negative signal input conductors of said input conductor pairs, respectively;

stroke signal output means electrically coupled for receiving signals from said current generating means; and

timing signal generating means electrically connected to the stroke signal generators for enabling conduction of successive ones of said generators.

7. The resistor matrix symbol generation apparatus of claim 6 in which different input circuits electrically couple the different current generating means to the input conductors and are characterized by having different multiples of primarily resistive impedance and including series connected unidirectionally conductive devices.

8. The resistor matrix stroke generation apparatus of claim 6 further comprising means for generating unblanking signals on at least one output terminal thereof coincident with the generated stroke signals, having a plurality of unblanking control means electrically coupled to selected ones of said input conductors and to said timing means for being operated thereby.

9. Resistor matrix symbol generation apparatus comprising:

a plurality of input conductors each for receiving a different selection signal;

a different variable electric current generator for each successive stroke to be generated, each having at least one output terminal and a plurality of unidirectionally conductive input circuits electrically coupled to selected ones of said input conductors;

constant current generating means having an output terminal;

stroke signal output means including storage means electrically coupled to the output terminals of all of said stroke generators and to said constant current generating means; and

timing means coupled to each of said electric stroke generators for enabling conductive of selected ones of said stroke generators for the symbol to be generated.

10. The resistor matrix stroke generation apparatus of claim 9 wherein the stroke signal output means includes capacitive energy storage means and the current signals received thereby from the variable electric current stroke generators and from the constant current generating means are of opposite polarities.

11. The stroke generation apparatus of claim 10 characterized in that the resistance of the input circuits are different multiples of a primarily resistive impedance value and include series connected unidirectionally conductive devices.

12. The resistor matrix stroke generation apparatus of claim 9 further comprising means for generating unblanking signals on at least one output terminal thereof, coincident with the generated stroke signals, having a plurality of unblanking control means electrically coupled to selected ones of said input conductors and to said timing means for being operated thereby.

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