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[Continued on next page]

(54) Title: SELF-BIASING CURRENT REFERENCE

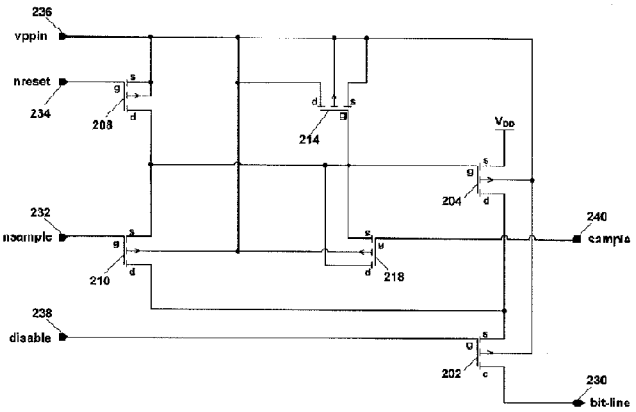

Figure 2

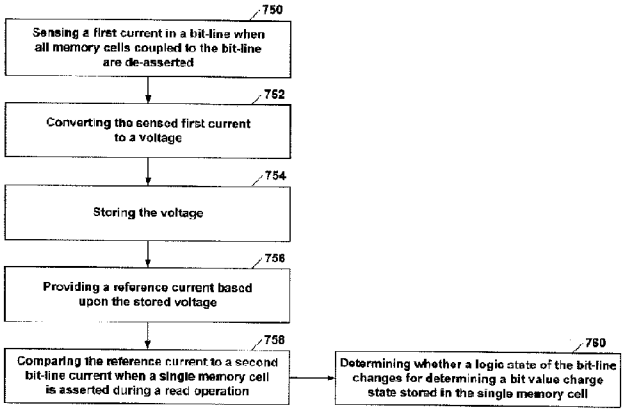

Figure 5

(57) Abstract: Current appearing on a bit-line with no memory cells asserted may be used during a bit-line pre-charge time before a read is performed so as to bias a gate-drain shorted PMOS pull-up device connected between the bit-line and a power supply at a VDD potential. The capacitance connected to the gate of this PMOS pull-up device may be used to "store" the resultant gate-source voltage when the drain is disconnected once the pre-charge time is completed. Once the read operation starts, the current of the PMOS pull-up device that has the "stored" resultant gate-source voltage is re-used as the reference for sensing the state of an asserted memory cell connected to the bit-line during the read operation thereof.

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SELF-BIASING CURRENT REFERENCE

RELATED PATENT APPLICATION

This application claims priority to commonly owned United States Provisional Patent Application Serial Number 61/702,338; filed September 18, 2012; entitled "Self-Biasing Current Reference," by David Francis Mietus, and is hereby incorporated by reference herein for all purposes.

TECHNICAL FIELD

The present disclosure relates to a self-biasing current reference, in particular, to a self-biasing current reference used in memory cells.

BACKGROUND

Electrically erasable and programmable read only memory (EEPROM) is a rewritable memory device that can hold its memory contents without power. EEPROMs are bit or byte addressable at the write level, which means either the bit or byte must be erased before it can be re-written. EEPROMs are typically used on circuit boards to store instructions and data. Referring to Figure 1, a "floating gate" holds the stored bit charge in the EEPROM. Complementary metal oxide semiconductor (CMOS) based transistor technologies are generally used and have a "floating gate" to hold the stored bit charge. When no charge is on the floating gate, the transistor acts normally, and a pulse on the control gate causes current to flow. When the floating gate is charged, this charge blocks the normal control gate action of the memory cell transistor, and current does not flow during a pulse on the control gate. Charging is accomplished by grounding the source and drain terminals and placing sufficient voltage on the control gate so that the charge tunnels through the oxide to the floating gate. A reverse voltage channeled from another transistor clears the floating gate charge by causing it to dissipate into the integrated circuit substrate.

Memory devices require high reliability. Technologies used to create, for example, serial EEPROM products can have limitations in the devices ability to read proper data out of the memory array. For example, excess "cell" leakage can minimize/eliminate the ability to distinguish between the "on" cell and "off" cell currents of an asserted memory cell being read. An offset can be caused by use of a "leaker" transistor connected to bit-line. Use of self-timed read schemes may allow for bit-line discharge before a read. Use of a read charge pump may minimize supply variations of "on" cell current.

Furthermore, the degradation of "on" cell current and/or uncontrolled/incorrect reference current levels limit sense amplifier performance. There is endurance related degradation of "on" cell current. Reference voltage/current levels used may vary excessively with the process used and/or does not track "on" cell current versus voltage supply and/or temperature. Bit-line leakage current cannot be compensated for by a fixed reference current.

SUMMARY

Therefore, a need exists in EEPROM memory products for improved immunity to endurance degradation of the memory cell current, eliminating external reference current and/or leakage compensation, improving circuit function by minimizing effects of leakage current at high temperatures, and enabling lower power operation by not requiring a bit-line to be precharged to the full V_{DD} potential during read operations.

According to an embodiment, a method for determining a charge state of a memory cell having a floating gate may comprise the steps of: sensing a first current in a bit-line when all memory cells coupled to the bit-line may be de-asserted; converting the first current to a voltage; storing the voltage; providing a reference current based upon the stored voltage; comparing the reference current with a second current in the bit-line when a single memory cell connected to the bit-line may be asserted during a read operation thereof; and determining a bit value charge state stored in the single memory cell from the comparison of the reference current with the second current.

According to a further embodiment of the method, the step of sensing the first current may comprise the step of coupling a gate and drain of a first transistor to the bit-line when all memory cells coupled to the bit-line may be de-asserted. According to a further embodiment of the method, the step of converting the first current to the voltage may comprise the step of generating the voltage across the gate and a source of the first transistor from the sensed first current. According to a further embodiment of the method, the step of storing the voltage may comprise the step of coupling the voltage across a gate and a connected together source-drain of a second transistor, wherein the voltage may be stored between a capacitance formed between a gate and source-drain of the second transistor. According to a further embodiment of the method, the step of storing the voltage may comprise the step of coupling the voltage across a capacitor. According to a further embodiment of the method, the step of providing

the reference current may comprise the step of generating the reference current with the first transistor based upon the voltage stored in the second transistor.

According to a further embodiment of the method, the step of providing the reference current may comprise the step of generating the reference current with the first transistor base upon the voltage stored in the capacitor. According to a further embodiment of the method, the step of comparing the reference current with the second current may comprise the step of monitoring the voltage of the bit-line associated with the memory cell after said memory cell has been asserted. According to a further embodiment of the method, the step of determining the bit value charge state stored in the single memory cell may comprise step of detecting the change in logic state or lack thereof of the bit-line associated with the asserted memory cell. According to a further embodiment of the method, the drain of the first transistor may be coupled to the bit-line and the source of the first transistor may be coupled to a power supply voltage, and the voltage stored in the second transistor biases the first transistor to provide the reference current. According to a further embodiment of the method, during a read operation of the asserted memory cell the stored voltage in the second transistor may be used in determining the reference current for sensing the bit value charge state of the asserted memory cell coupled to the bit-line. According to a further embodiment of the method, the first and second transistors may be p-type metal oxide semiconductor (PMOS) transistors. According to a further embodiment of the method, the first and second transistors may be n-type metal oxide semiconductor (NMOS) transistors.

According to another embodiment, an apparatus for determining a charge state of a memory cell having a floating gate may comprise: a first transistor having a gate and drain coupled to a bit-line and a source coupled to a power supply voltage when all memory cells coupled to the bit-line may be de-asserted, wherein a first current in the bit-line may be sensed; the first transistor converts the first current to a voltage; a second transistor stores the voltage; the first transistor provides a reference current based upon the stored voltage from the second transistor; wherein the reference current may be compared with a second current in the bit-line when a single memory cell connected to the bit-line may be asserted during a read operation thereof; and a bit value charge state stored in the single memory cell may be determined from the comparison of the reference current with the second current.

According to a further embodiment, the first current through the first transistor generates the voltage between the gate and a source of the first transistor. According to a further embodiment, the voltage may be stored between a capacitance formed between a gate and source-drain of the second transistor. According to a further embodiment, the voltage may be stored on a capacitor. According to a further embodiment, the reference current may be compared with the second current by means of the bit-line associated with the asserted memory cell. According to a further embodiment, the bit value charge state stored in the single memory cell may be determined by detecting the change in logic state or lack thereof of the bit-line associated with the asserted memory cell. According to a further embodiment, the first and second transistors may be p-type metal oxide semiconductor (PMOS) transistors. According to a further embodiment, the first and second transistors may be n-type metal oxide semiconductor (NMOS) transistors.

According to yet another embodiment, an apparatus for determining a charge state of a memory cell having a floating gate may comprise: a first transistor having a gate and drain coupled to a bit-line and a source coupled to a power supply voltage when all memory cells coupled to the bit-line may be de-asserted, wherein a first current in the bit-line may be sensed; the first transistor converts the first current to a voltage; a capacitor stores the voltage; the first transistor provides a reference current based upon the stored voltage from the capacitor; wherein the reference current may be compared with a second current in the bit-line when a single memory cell connected to the bit-line may be asserted during a read operation thereof; and a bit value charge state stored in the single memory cell may be determined from the comparison of the reference current with the second current.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present disclosure may be acquired by referring to the following description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a schematic cross-section diagram of an electrically erasable and programmable read only memory (EEPROM) transistor, according to the teachings of this disclosure;

Figure 2 illustrates a schematic diagram of a self-biasing current reference, according to a specific example embodiment of this disclosure;

Figure 3 illustrates a schematic diagram used to model the self-biasing current reference shown in Figure 2;

Figure 4 illustrates timing waveforms of the circuit shown in Figure 3 for both the "on" and "off" states of the asserted memory cell; and

Figure 5 illustrates a flow diagram for the application which utilizes the self-biasing current reference, according to a specific example embodiment of this disclosure.

While the present disclosure is susceptible to various modifications and alternative forms, specific example embodiments thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific example embodiments is not intended to limit the disclosure to the particular forms disclosed herein, but on the contrary, this disclosure is to cover all modifications and equivalents as defined by the appended claims.

DETAILED DESCRIPTION

According to various embodiments of this disclosure, the current present on an unasserted memory array bit-line may be sensed and stored as a voltage. This stored voltage may then be utilized to generate a reference current when sensing the state of an asserted memory cell during a read operation thereof. Furthermore, according to various embodiments, an improved circuit function may be provided by minimizing the effects of leakage current at high temperatures. Various embodiments enable lower power operation since the bit-line may be precharged to less than a V_{DD} potential during reads of the asserted memory cell.

According to various embodiments, the immunity to endurance degradation of memory cell current is improved and the need for external reference voltage, current and/or leakage compensation may be eliminated.

According to various embodiments, the current appearing on the bit-line with no memory cells asserted may be used during the bit-line pre-charge time before a read is performed to bias the gate-drain shorted PMOS pull-up device connected between the bit-line and the power supply at a V_{DD} potential. The capacitance connected to the gate of this PMOS pull-up device may be used to "store" the resultant gate-source voltage when the drain is disconnected once the pre-charge time is completed. Once the read operation starts, the

current of the PMOS pull-up device that has the "stored" resultant gate-source voltage is re-used as the reference for sensing the state of an asserted memory cell connected to the bit-line during the read operation thereof.

Referring now to the drawing, the details of a specific example embodiment is schematically illustrated. Like elements in the drawings will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix.

Referring to Figure 2, depicted is a schematic diagram of a self-biasing current reference, according to a specific example embodiment of this disclosure. Transistors 202, 204, 208, 210, 214 and 218 may be P-type metal oxide semiconductor (PMOS) transistors arranged and connected together as shown in Figure 2 and function together as follows: When all of the memory cells of an EEPROM memory array (not shown) attached to a bit-line 230 are de-asserted, current on the bit-line 230 is sensed by asserting a logic low ("0") on the nsample node 232 causing the gate and drain of transistor 204 to be coupled together via transistor 210. Current then flows through transistor 204, thereby generating a voltage that appears across the gate-source of transistor 214 which also functions as a "hold" capacitor for this voltage. It is contemplated and within the scope of this disclosure that N-type metal oxide semiconductor (NMOS) transistors may be used instead of the PMOS transistors, and one having ordinary skill in semiconductor and memory circuit design, and having the benefit of this disclosure, could design such a circuit using NMOS transistors.

When the nsample node 232 is de-asserted to a logic high ("1"), transistor 204 now acts as a current reference, wherein a reference current is determined by the voltage stored across the gate-source of transistor 214 acting as the "hold" capacitor. This reference current may then be compared against a current from a single asserted memory cell (not shown) connected to the bit-line node 230 during a read operation thereof. Depending upon the current from this asserted memory cell, the voltage appearing on the bit-line node 230 (drain of transistor 202) may be observed to change its logic state based on the ON (high current) or OFF (low current) state of this asserted memory cell, *e.g.*, bit-line node 230 at a first voltage level when the reference current is greater than the asserted memory cell current and at a second voltage level when the reference current is less than the asserted memory cell current. This operation is independent of the number of memory cells connected to the bit-line node

230 since the change in current that is observed is caused by the state change of the single memory cell that is being asserted, as explained more fully hereinafter.

When the nreset node 234 is asserted to a logic low, the transistor 208 may be used to discharge the gate terminal of transistor 204 to the V_{DD} potential present on the vppin node 236 during power cycling or to begin/end a read operation. Transistor 218, along with the sample signal on node 240, may be used as charge compensation to offset the "hold" step voltage that results from de-asserting transistor 210. This may be needed to insure that the reference current generated by transistor 204 is equal to or greater than the current that was originally present on the memory array bit-line node 230. Transistor 202 is optional but, preferably, can be used to isolate the high voltages present on the bit-line node 230 during write operations from the other transistors utilized according to various embodiments of this disclosure. Note that the "hold" capacitor comprising the gate-source of transistor 214 may alternatively be provided by using an actual capacitor, according to a specific example embodiment of this disclosure.

Referring to Figure 3, depicted is a schematic diagram used to model the circuit which utilizes the self-biasing current reference (circuit block 442) shown in Figure 2. Current source 446 is used to include the leakage current generated by other circuit blocks (not shown) that connect to the bit-line node 230. Transistor 448 is used to include the plethora of de-asserted memory cells connected to the bit-line node 230. Transistor 450 represents the single memory cell connected to the bit-line node 230 that is asserted, by means of wl node 452, for the read operation. Capacitor 454 is used to include the parasitic capacitance associated with the bit-line node 230.

Referring to Figure 4, depicted are the read operation timing waveforms associated with the circuit model shown in Figure 3 for both the “on” and “off” states of the asserted memory cell. The read operation begins when the nreset node 234 is briefly asserted to a logic low which discharges the gate terminal of transistor 204 to the V_{DD} potential present on the vppin node 236. This also serves to discharge any stored charge present on the gate terminal of transistor 214. The read operation continues by cycling nsample node 232 and sample node 240 which results in the current I_{store} being generated by transistor 204 via transistor 202 as determined by the stored charge present on the gate terminal of transistor 214. The value of I_{store} may be approximated as:

$$I_{store} \sim I_{446} + I_{448} + I_{450,de\text{-}asserted}$$

This also results in the bit-line node 230 being forced to a voltage that is below the V_{DD} potential present on the vppin node 236 as determined by the gate-source voltage present on transistor 204. Once the cycling of nsample node 232 and sample node 240 has completed, the wl node 452 is transitioned which asserts memory cell transistor 450. With memory cell transistor 450 asserted, the bit-line node 230 will now respond in one of two ways:

1) If memory cell transistor 450 is in an "off" state, then bit-line node 230 will remain unchanged (near Vdd potential) based on the fact that:

$$I_{store} > I_{446} + I_{448} + I_{450,asserted}$$

As a consequence, bit-line node 230 may be considered to be in a logic high state.

2) If memory cell transistor 450 is in an "on" state, then bit-line node 230 will be discharged to near ground potential based on the fact that:

$$I_{store} < I_{446} + I_{448} + I_{450,asserted}$$

As a consequence, bit-line node 230 can be considered to be in a logic low state.

Therefore, the "on" or "off" state of the memory cell transistor 450 can be readily determined by monitoring the voltage present on bit-line node 230. The read operation is terminated when memory cell transistor 450 is de-asserted by transitioning wl node 452 (not shown in Figure 4).

Referring to Figure 5, depicted is the flow diagram associated with the circuit which utilizes the self-biasing current reference, according to a specific example embodiment of this disclosure. In step 750 a first bit-line current is sensed when all memory cells coupled to the bit-line are de-asserted. In step 752 the sensed first bit-line current is converted to a voltage, and in step 754 the voltage is stored, *e.g.*, in the gate-source junction of transistor 214 acting as a voltage storage capacitor. In step 756 a reference current is provided based upon the stored voltage. In step 758 the reference current is compared to a second bit-line current when a single memory cell coupled thereto is asserted during a read operation. In step 760 a determination is made whether a logic state of the bit-line changes for determining a bit value charge state stored in the single memory cell.

According to the teachings of this disclosure, a "self-biased" current reference may be generated that effectively eliminates the limitations of existing solutions for properly reading data out of an EEPROM array. Use of pre-charge voltage less than the supply voltage reduces power consumption. The various embodiments of this disclosure may be used to reduce fabrication costs and enable more robust memory devices such as, for example but not limited to, serial EEPROM products.

While embodiments of this disclosure have been depicted, described, and are defined by reference to example embodiments of the disclosure, such references do not imply a limitation on the disclosure, and no such limitation is to be inferred. The subject matter disclosed is capable of considerable modification, alteration, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent art and having the benefit of this disclosure. The depicted and described embodiments of this disclosure are examples only, and are not exhaustive of the scope of the disclosure.

CLAIMS

What is claimed is:

1. A method for determining a charge state of a memory cell having a floating gate, said method comprising the steps of:

sensing a first current in a bit-line when all memory cells coupled to the bit-line are de-asserted;

converting the first current to a voltage;

storing the voltage;

providing a reference current based upon the stored voltage;

comparing the reference current with a second current in the bit-line when a single memory cell connected to the bit-line is asserted during a read operation thereof; and

determining a bit value charge state stored in the single memory cell from the comparison of the reference current with the second current.

2. The method according to claim 1, wherein the step of sensing the first current comprises the step of coupling a gate and drain of a first transistor to the bit-line when all memory cells coupled to the bit-line are de-asserted.

3. The method according to claim 2, wherein the step of converting the first current to the voltage comprises the step of generating the voltage across the gate and a source of the first transistor from the sensed first current.

4. The method according to claim 3, wherein the step of storing the voltage comprises the step of coupling the voltage across a gate and a connected together source-drain of a second transistor, wherein the voltage is stored between a capacitance formed between a gate and source-drain of the second transistor.

5. The method according to claim 3, wherein the step of storing the voltage comprises the step of coupling the voltage across a capacitor.

6. The method according to claim 4, wherein the step of providing the reference current comprises the step of generating the reference current with the first transistor based upon the voltage stored in the second transistor.

7. The method according to claim 5, wherein the step of providing the reference current comprises the step of generating the reference current with the first transistor base upon the voltage stored in the capacitor.

8. The method according to claim 1, wherein the step of comparing the reference current with the second current comprises the step of monitoring the voltage of the bit-line associated with the memory cell after said memory cell has been asserted.

9. The method according to claim 1, wherein the step of determining the bit value charge state stored in the single memory cell comprises step of detecting the change in logic state or lack thereof of the bit-line associated with the asserted memory cell.

10. The method according to claim 6, wherein the drain of the first transistor is coupled to the bit-line and the source of the first transistor is coupled to a power supply voltage, and the voltage stored in the second transistor biases the first transistor to provide the reference current.

11. The method according to claim 1, wherein during a read operation of the asserted memory cell the stored voltage in the second transistor is used in determining the reference current for sensing the bit value charge state of the asserted memory cell coupled to the bit-line.

12. The method according to claim 4, wherein the first and second transistors are p-type metal oxide semiconductor (PMOS) transistors.

13. The method according to claim 4, wherein the first and second transistors are n-type metal oxide semiconductor (NMOS) transistors.

14. An apparatus for determining a charge state of a memory cell having a floating gate, comprising:

a first transistor having a gate and drain coupled to a bit-line and a source coupled to a power supply voltage when all memory cells coupled to the bit-line are de-asserted, wherein a first current in the bit-line is sensed;

the first transistor converts the first current to a voltage;

a second transistor stores the voltage;

the first transistor provides a reference current based upon the stored voltage from the second transistor;

wherein the reference current is compared with a second current in the bit-line when a single memory cell connected to the bit-line is asserted during a read operation thereof; and

a bit value charge state stored in the single memory cell is determined from the comparison of the reference current with the second current.

15. The apparatus according to claim 14, wherein the first current through the first transistor generates the voltage between the gate and a source of the first transistor.

16. The apparatus according to claim 14, wherein the voltage is stored between a capacitance formed between a gate and source-drain of the second transistor.

17. The apparatus according to claim 14, wherein the voltage is stored on a capacitor.

18. The apparatus according to claim 14, wherein the reference current is compared with the second current by means of the bit-line associated with the asserted memory cell.

19. The apparatus according to claim 14, wherein the bit value charge state stored in the single memory cell is determined by detecting the change in logic state or lack thereof of the bit-line associated with the asserted memory cell.

20. The apparatus according to claim 14, wherein the first and second transistors are p-type metal oxide semiconductor (PMOS) transistors.

21. The apparatus according to claim 14, wherein the first and second transistors are n-type metal oxide semiconductor (NMOS) transistors.

22. An apparatus for determining a charge state of a memory cell having a floating gate, comprising:

a first transistor having a gate and drain coupled to a bit-line and a source coupled to a power supply voltage when all memory cells coupled to the bit-line are de-asserted, wherein a first current in the bit-line is sensed;

the first transistor converts the first current to a voltage;

a capacitor stores the voltage;

the first transistor provides a reference current based upon the stored voltage from the capacitor;

wherein the reference current is compared with a second current in the bit-line when a single memory cell connected to the bit-line is asserted during a read operation thereof; and

a bit value charge state stored in the single memory cell is determined from the comparison of the reference current with the second current.

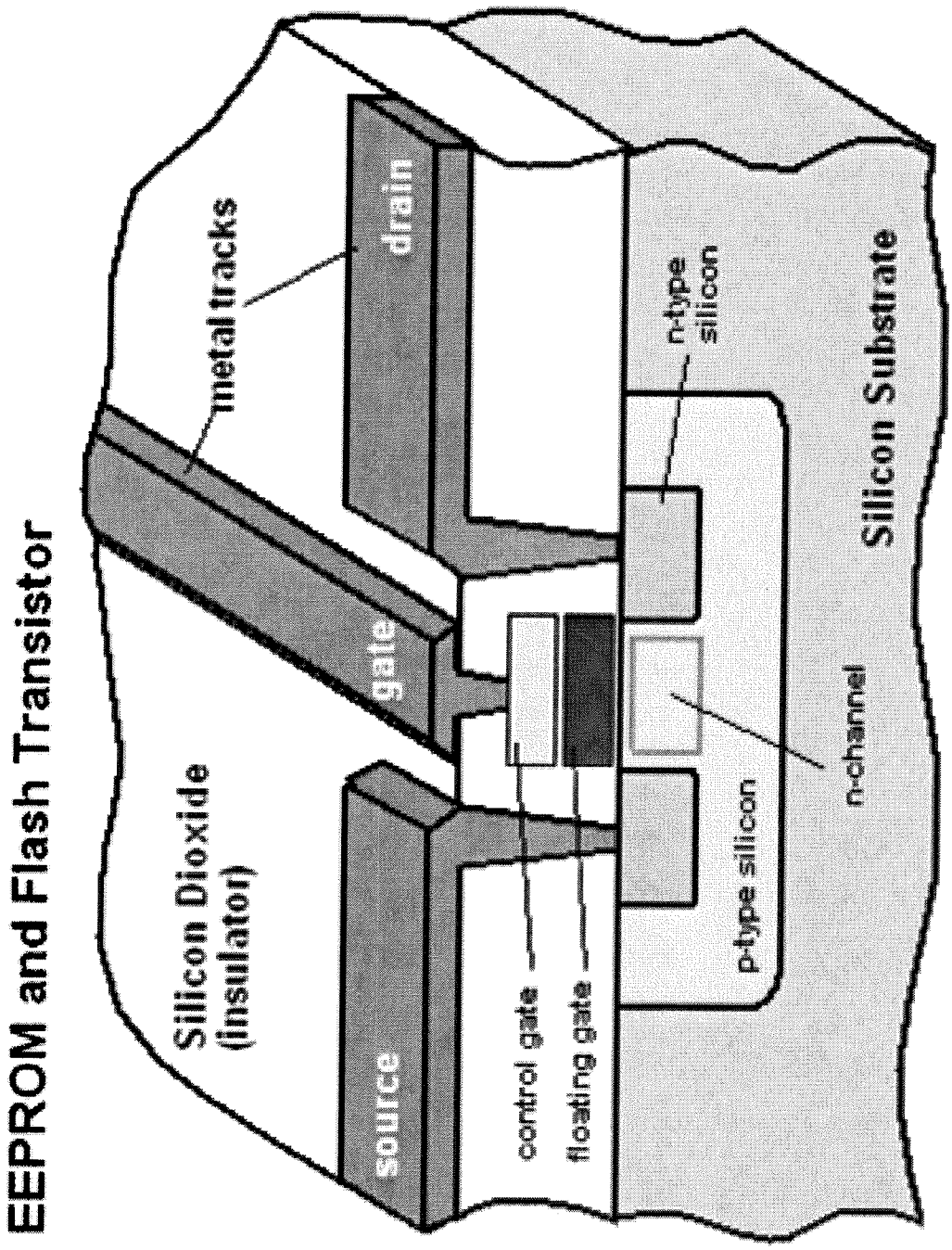
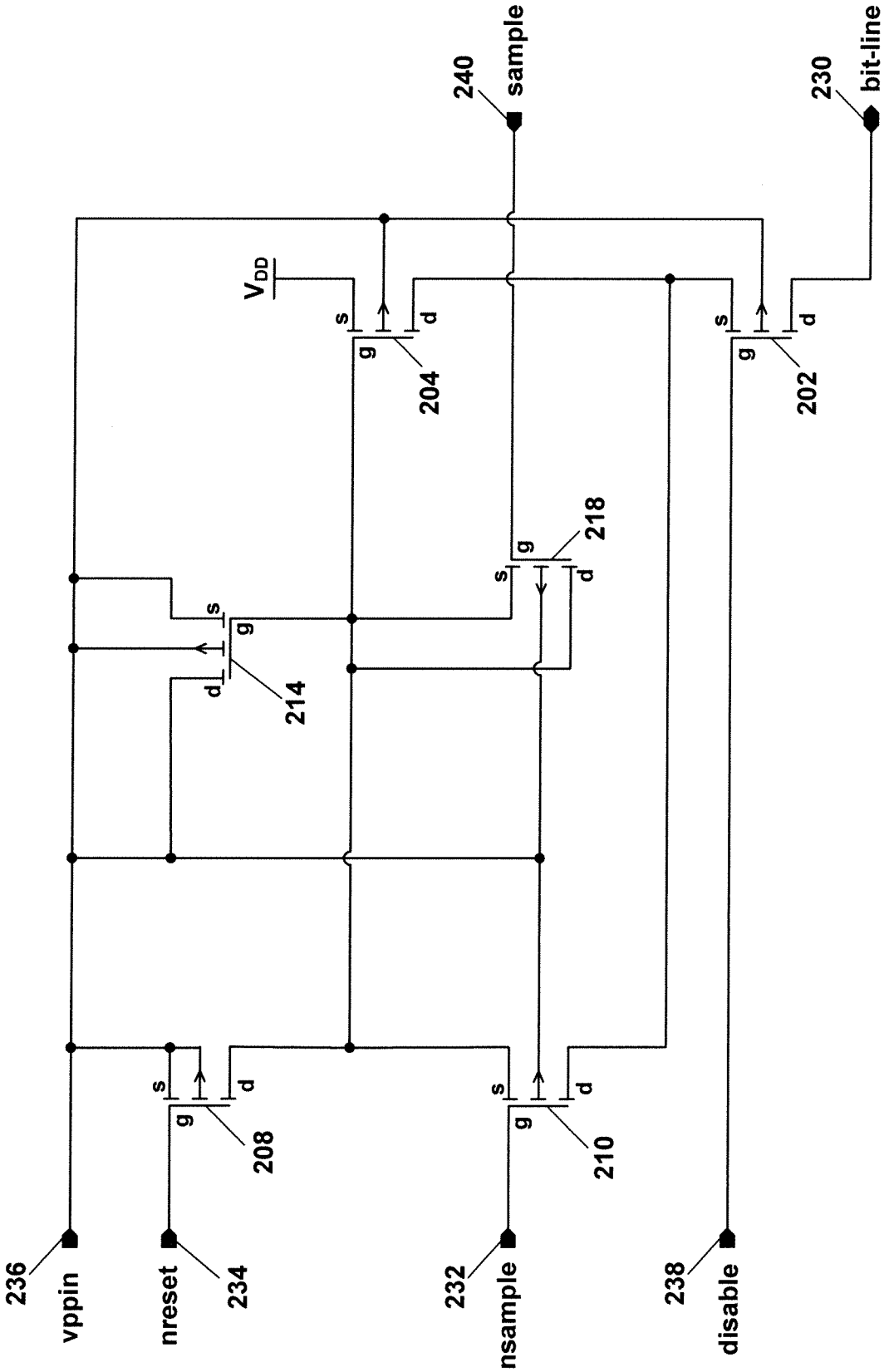

EEPROM and Flash Transistor
metal tracks
drain
gate
Silicon Dioxide
(insulator)
source
control gate
floating gate
n-type
silicon
p-type silicon
n-channel
Silicon Substrate

Figure 1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sample
230
bit-line
V_{DD}
s
d
g
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202
218
214
208
210
236
vppin
nreset
234
232
nsample
238
disable

Figure 2

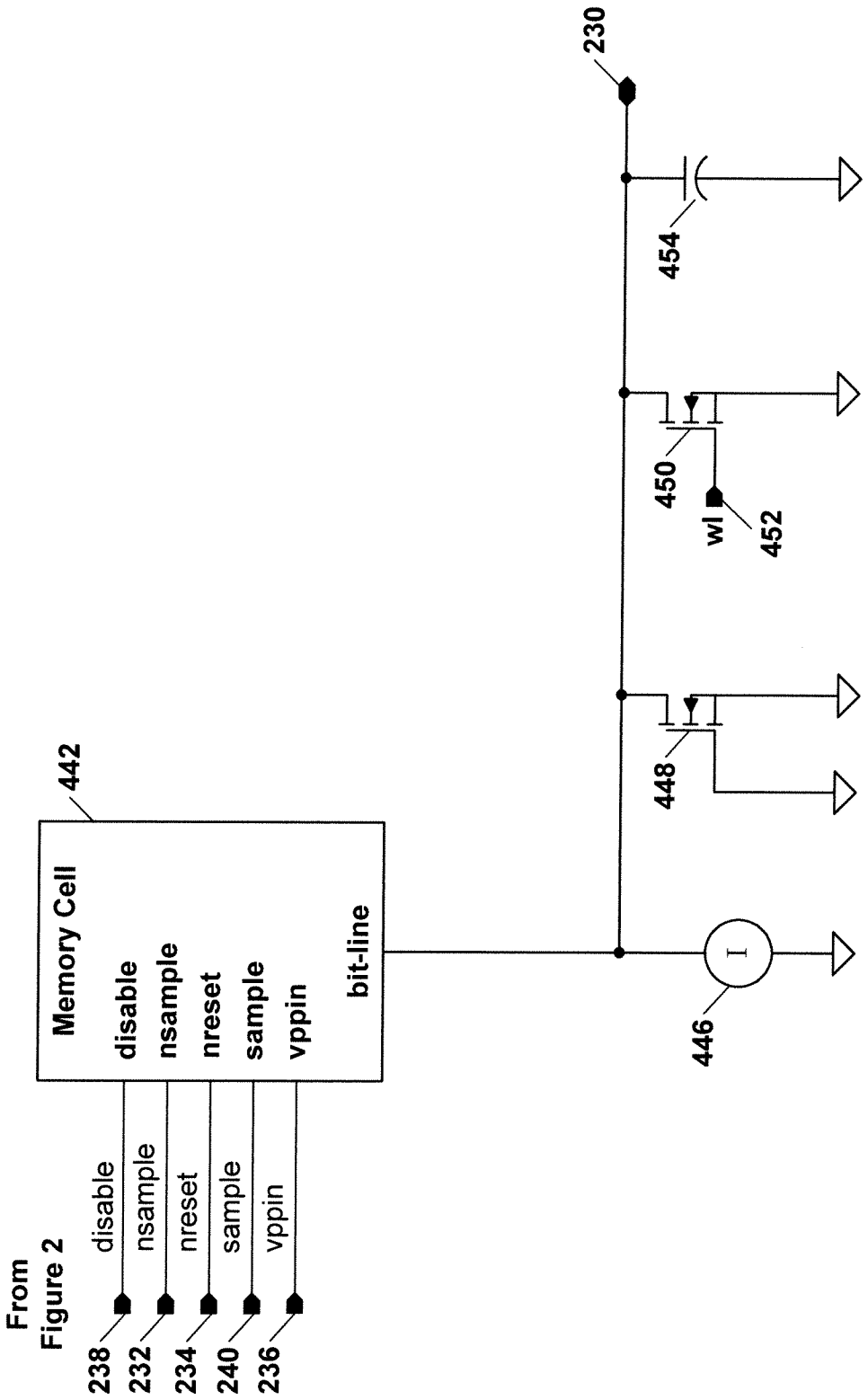
From Figure 2
disable
nsample
nreset
sample
vppin
238
232
234
240
236
Memory Cell
disable
nsample
nreset
sample
vppin
bit-line
442
230
454
450
wl
452
448
446

Figure 3

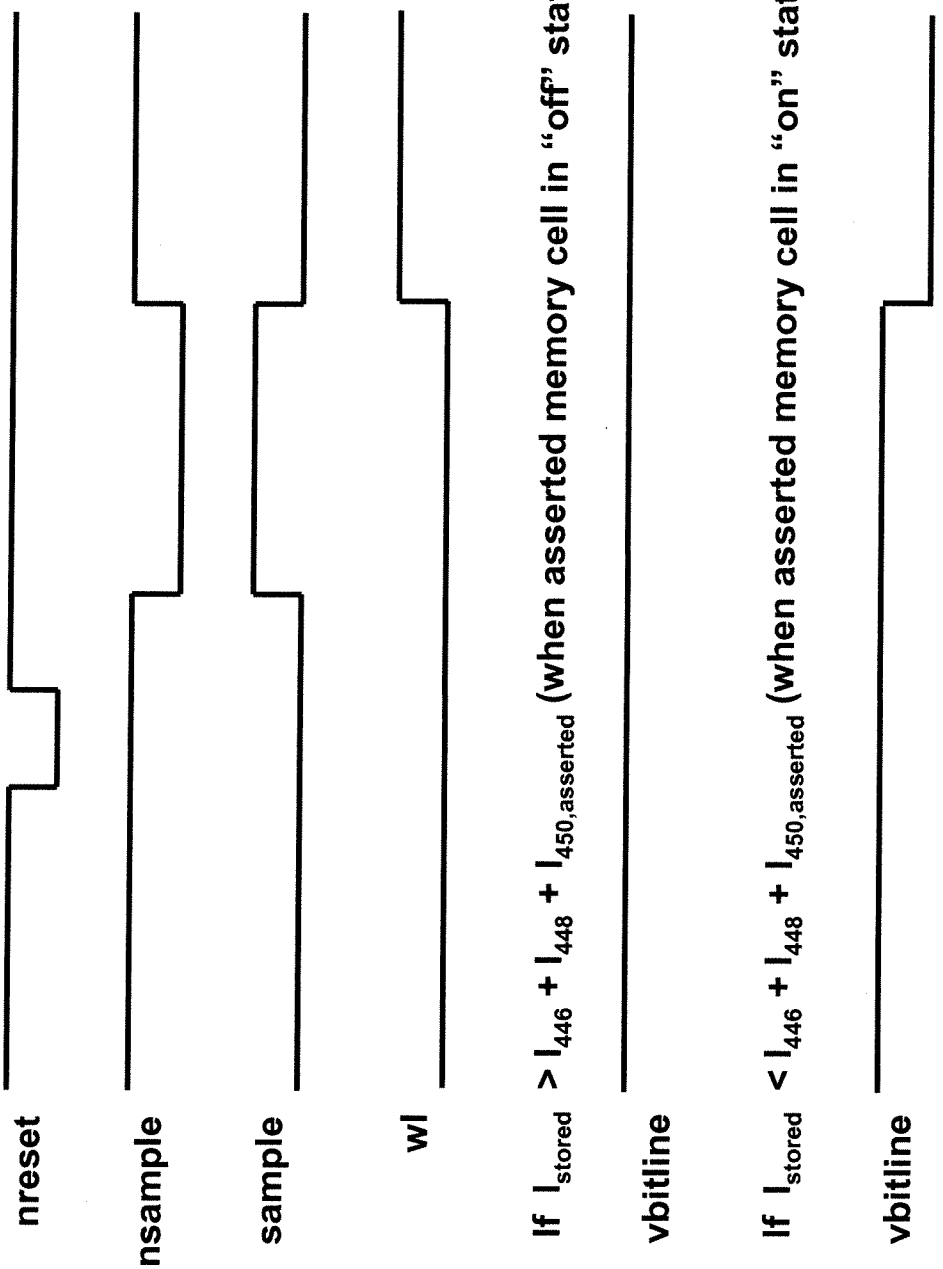
nreset
nsample
sample
wl
If $I_{stored} > I_{446} + I_{448} + I_{450,asserted}$ (when asserted memory cell in "off" state)
vbitline
If $I_{stored} < I_{446} + I_{448} + I_{450,asserted}$ (when asserted memory cell in "on" state)
vbitline

Figure 4

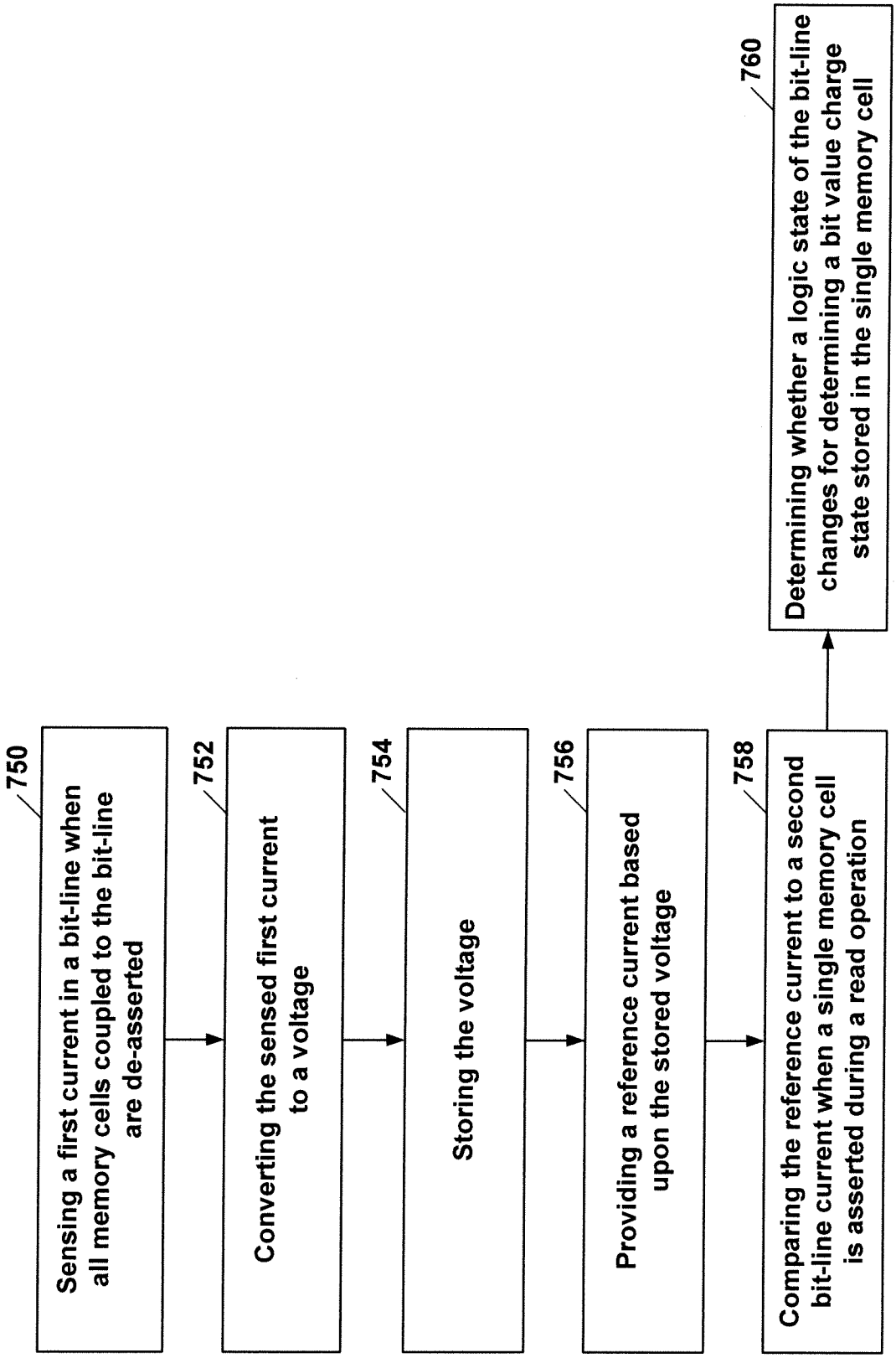
750
Sensing a first current in a bit-line when all memory cells coupled to the bit-line are de-asserted
752
Converting the sensed first current to a voltage
754
Storing the voltage
756
Providing a reference current based upon the stored voltage
758
Comparing the reference current to a second bit-line current when a single memory cell is asserted during a read operation
760
Determining whether a logic state of the bit-line changes for determining a bit value charge state stored in the single memory cell

Figure 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/060302

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C16/24 G11C16/28 G11C7/06 G11C7/14
ADD. G11C13/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2011/286259 A1 (PERNER FREDERICK [US]) 24 November 2011 (2011-11-24) paragraph [0030] - paragraphs [0051], [0055]; figures 2-4b,6	1-3,5, 7-9,22 4,6, 10-21
A	US 2008/106945 A1 (JO SUNG-KYU [KR] ET AL) 8 May 2008 (2008-05-08) paragraph [0026] - paragraph [0055]; figures 3-5	1,8,9, 14,22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2014	24/01/2014

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/060302

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011286259 A1	24-11-2011	NONE	
US 2008106945 A1	08-05-2008	CN 101174467 A	07-05-2008
		US 2008106945 A1	08-05-2008