United States Patent

[11] 3,618,133

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[45] Patented **Nov. 2, 1971**

[73] Assignee **International Standard Electric Corporaton**
New York, N.Y.

[32] Priority **June 7, 1968**
[33] **Great Britain**
[31] **27,161/68**

[54] **SYMMETRICAL POLYPHASE NETWORKS UTILIZING CONSTANT REACTANCES**
19 Claims, 44 Drawing Figs.

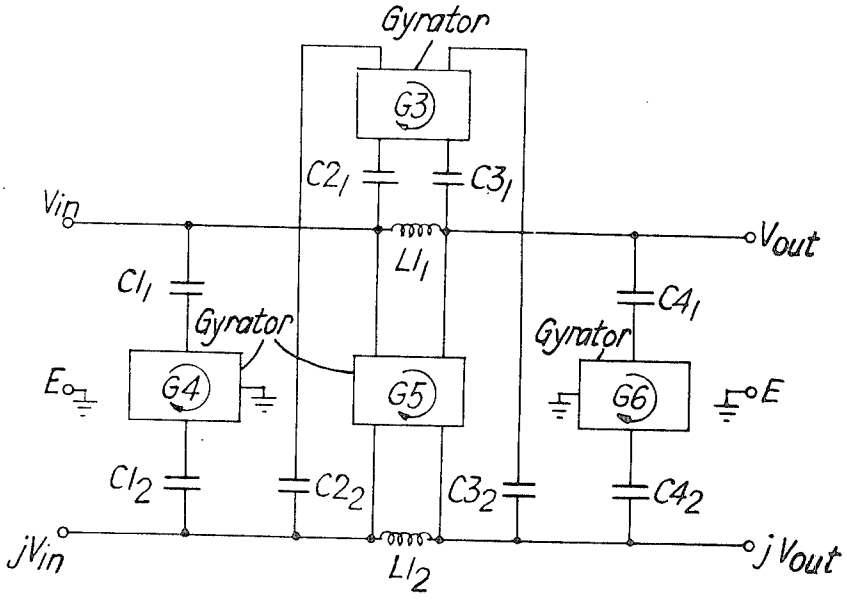
[52] **U.S. Cl.** **333/24,**
307/295, 333/70 R, 333/80 R, 332/45
[51] **Int. Cl.** **H03h 7/44**
[50] **Field of Search** ..... 333/1, 80, 80 T, 24, 70, 6; 307/295; 328/155; 324/107, 108; 336/5, 10, 12; 330/107, 109

[56] **References Cited**
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Primary Examiner—Eli Lieberman
Assistant Examiner—Paul L. Gensler
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ABSTRACT: Symmetrical polyphase networks are disclosed comprising N single-phase networks each including a constant reactance, i.e, a reactance whose value remains constant with changes in the frequency of the signal applied thereto. Due to the use of this constant reactance (controlled constant current source, such as properly connected and controlled transistors, or impedance transformers), the polyphase network responds differently to input signals of negative and positive frequencies (a positive frequency is a counterclockwise sequence of vectors representing polyphase input signals and a negative frequency is a clockwise sequence of vectors representing polyphase input signals). Also the polyphase network has a different insertion loss characteristic depending on the sequence of the polyphase input signals.



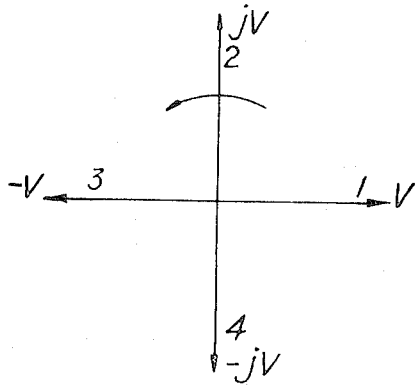


Fig. 1(A)

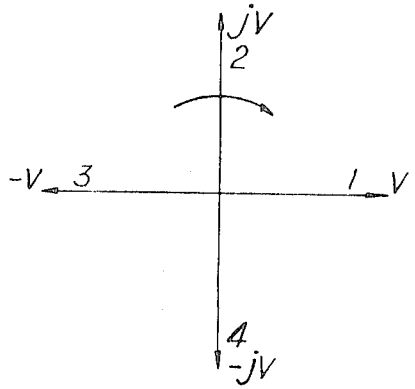


Fig. 1(B)

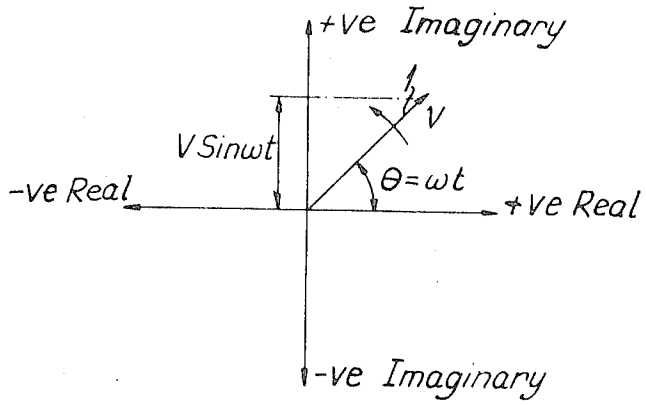


Fig. 2.

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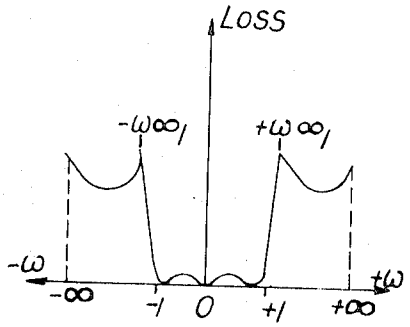


Fig. 3A.

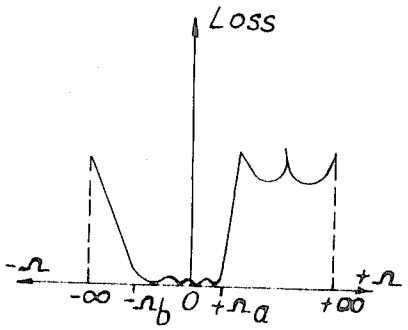


Fig. 3B.

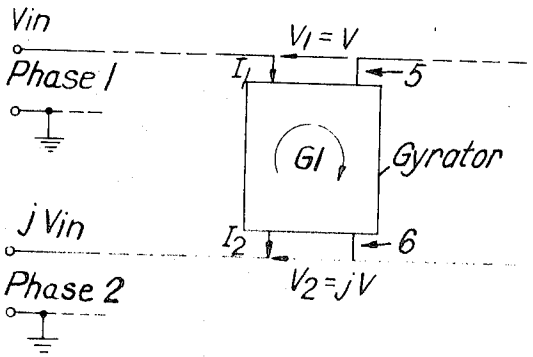


Fig. 4.

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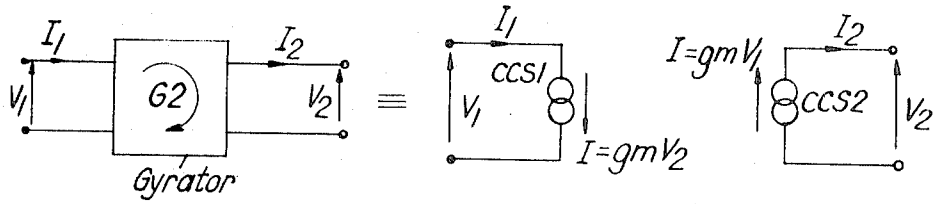


Fig. 5.

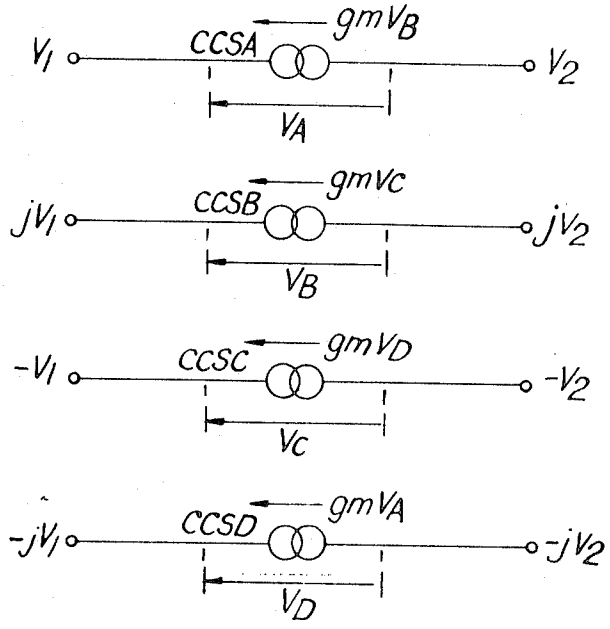


Fig. 6.

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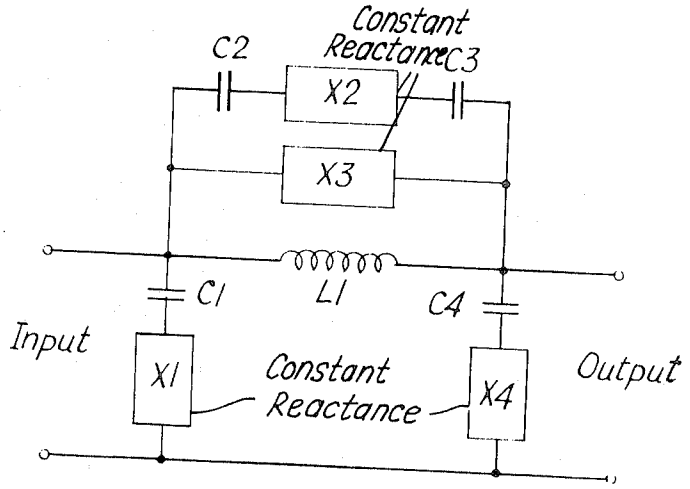


Fig. 7.

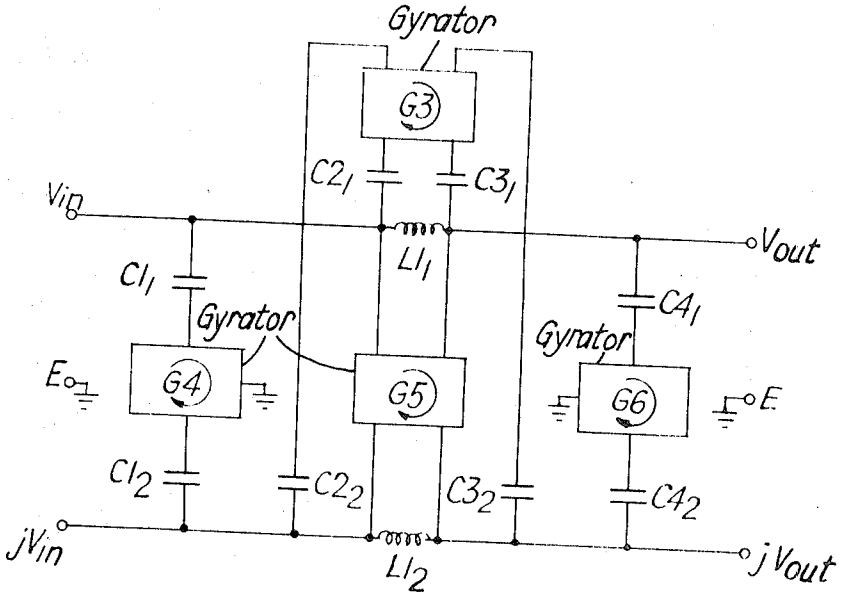


Fig. 8.

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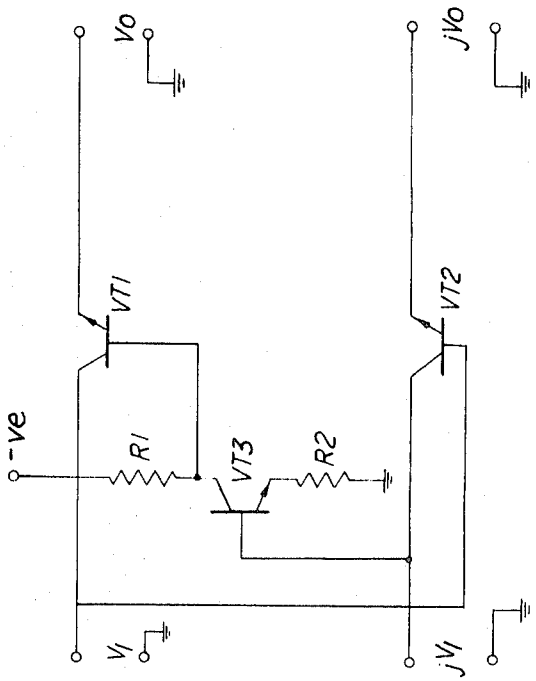


Fig. 9B.

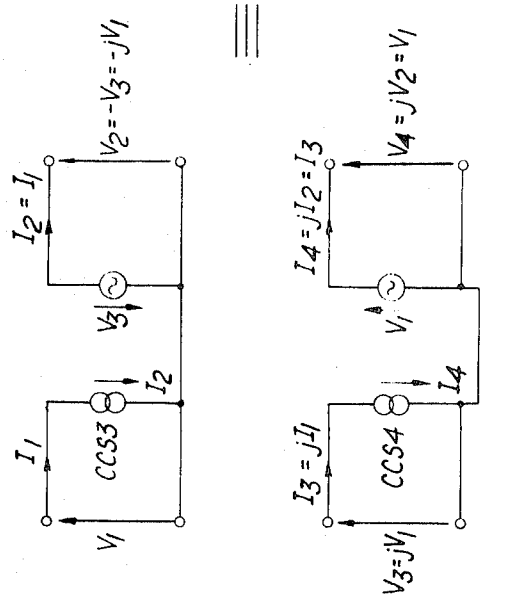


Fig. 9A.

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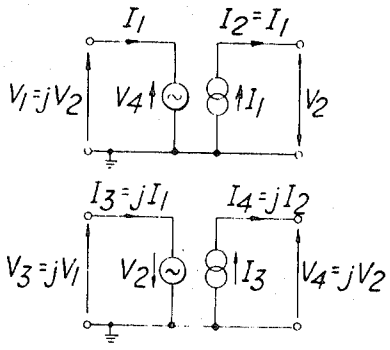


Fig. 10A.

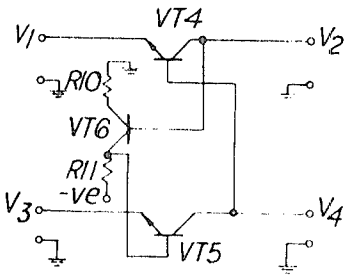


Fig. 10B

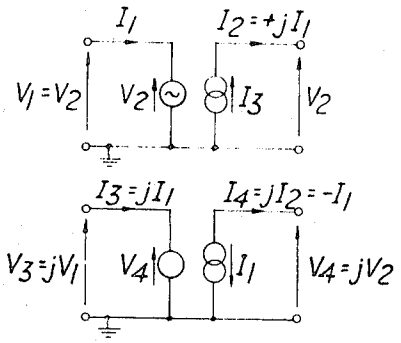


Fig. 11A.

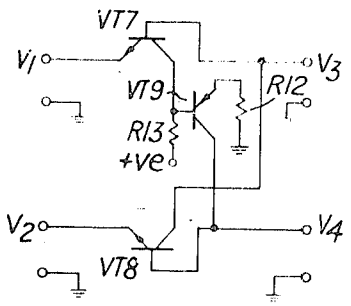


Fig. 11B.

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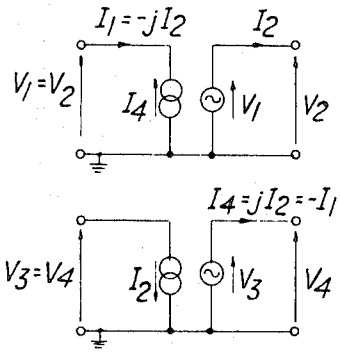


Fig. 12 (A)

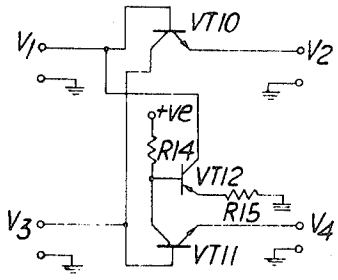


Fig. 12 (B)

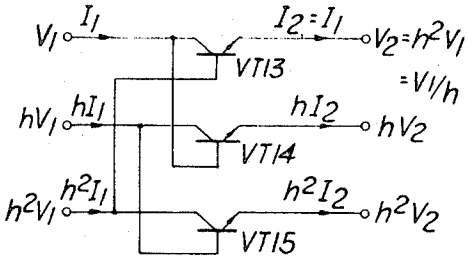


Fig. 16.

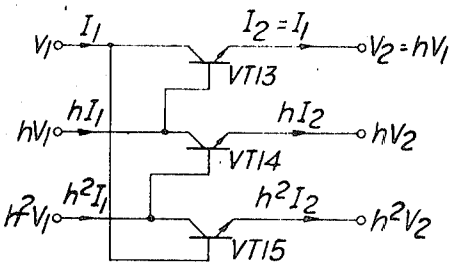


Fig. 17.

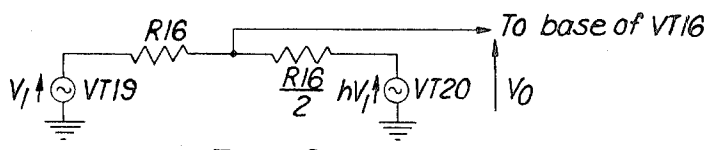


Fig. 19.

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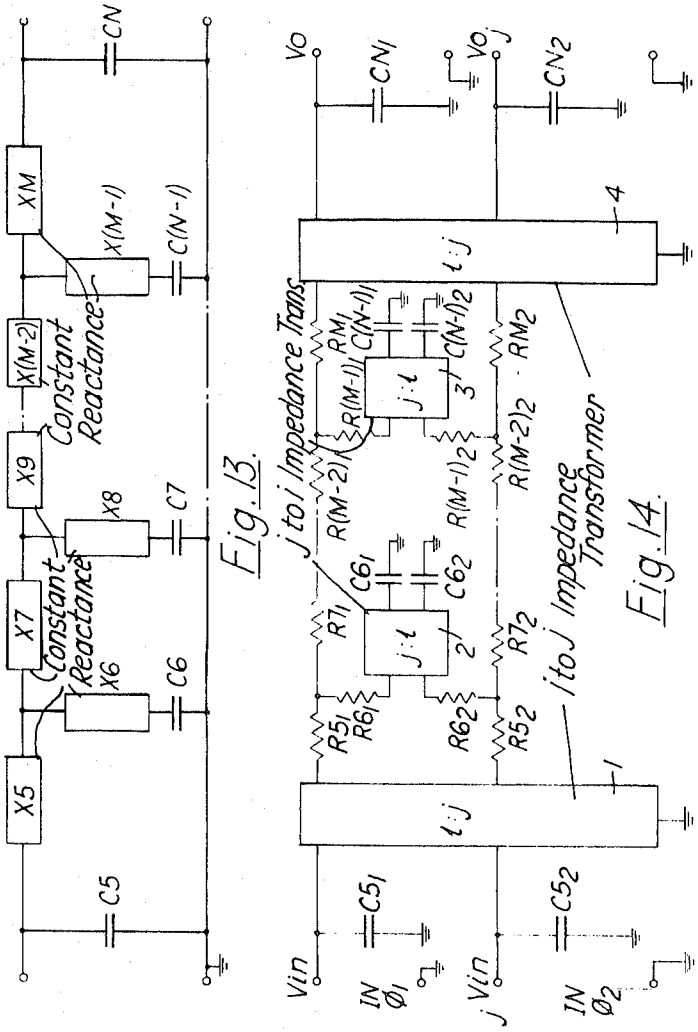


Fig. 13.

Fig. 14.

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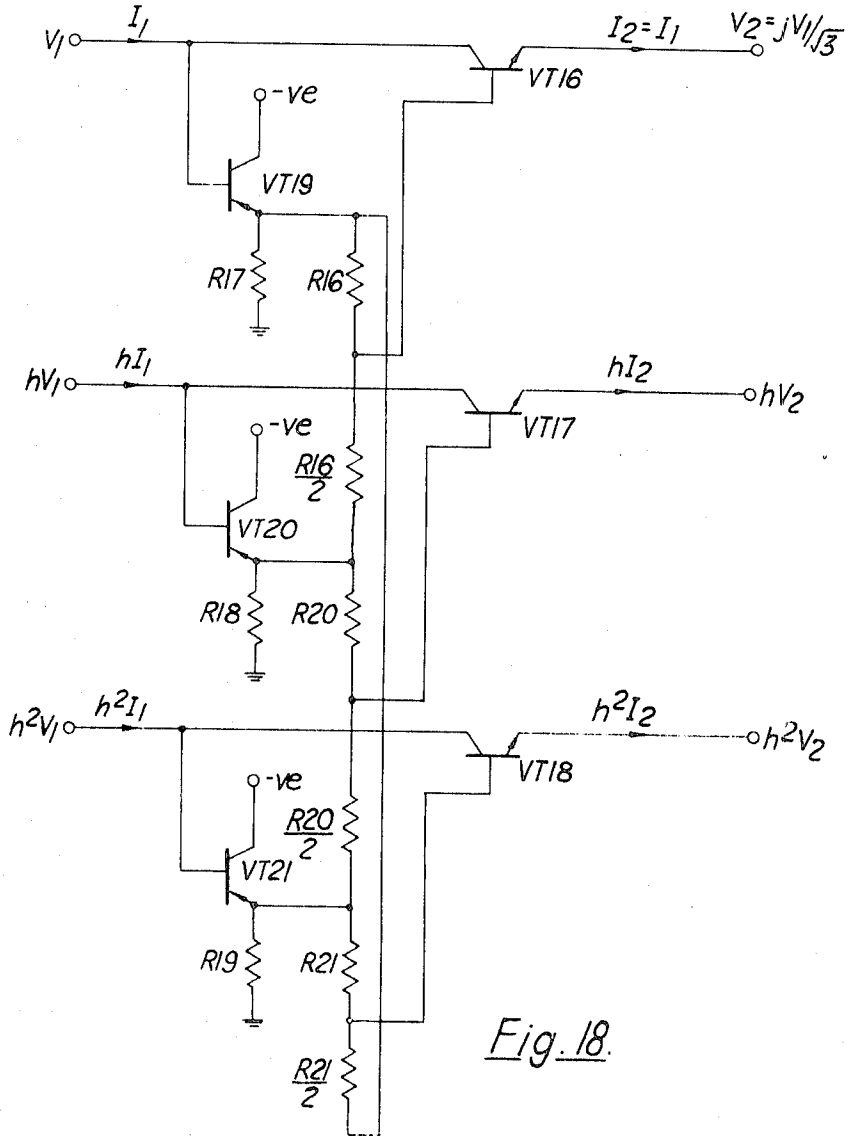


Fig. 18.

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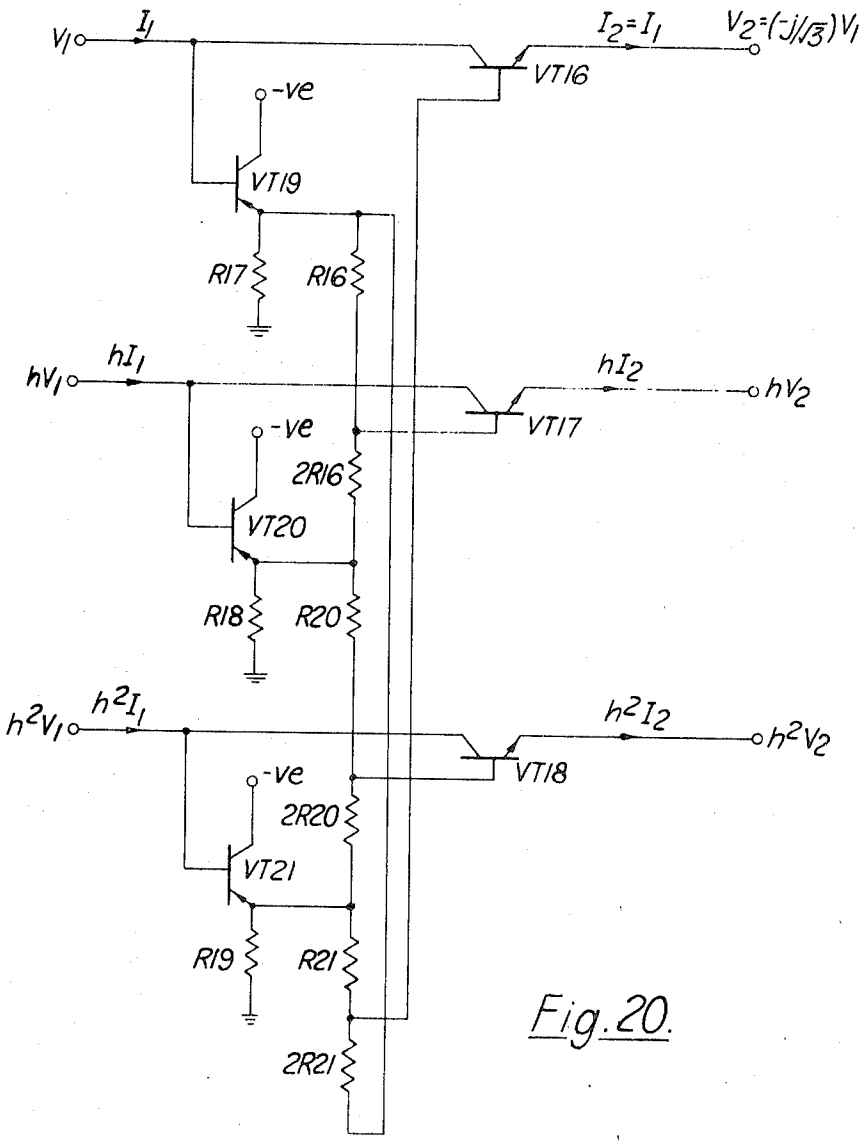


Fig. 20.

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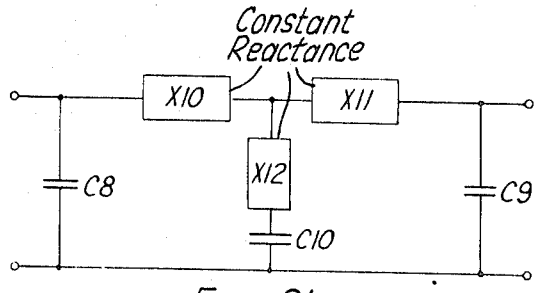


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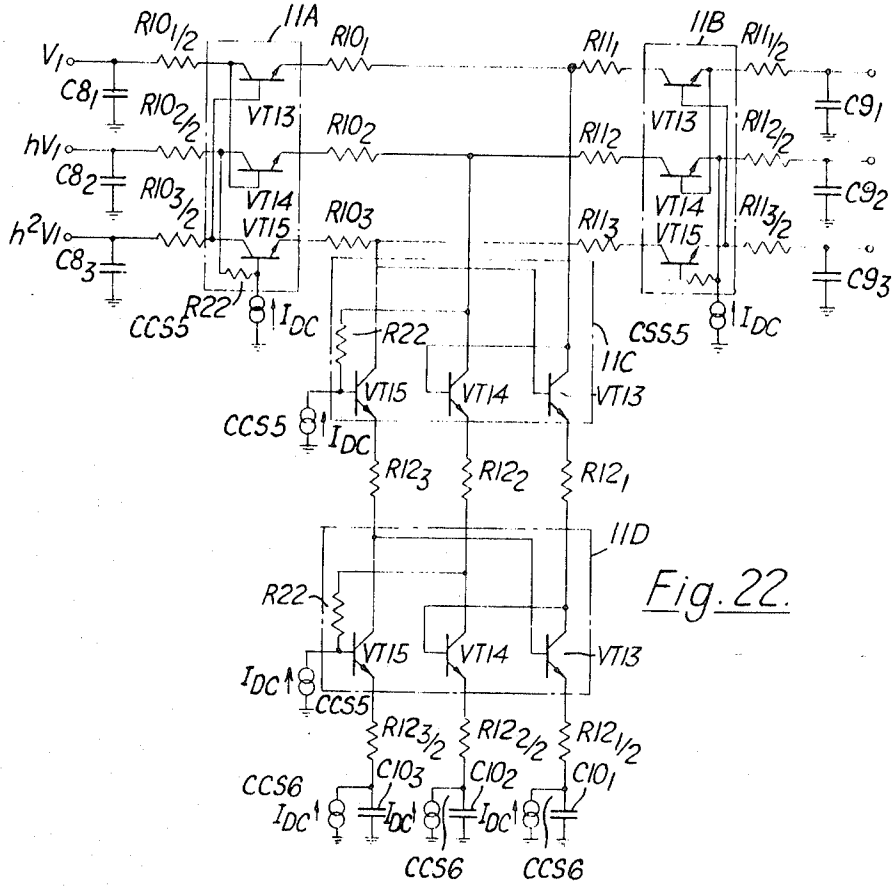


Fig. 22.

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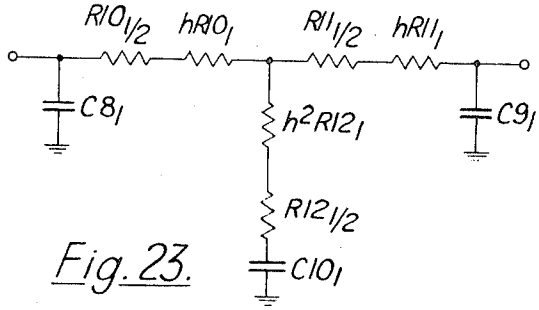


Fig. 23.

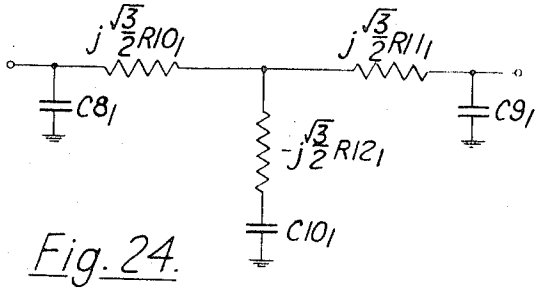


Fig. 24.

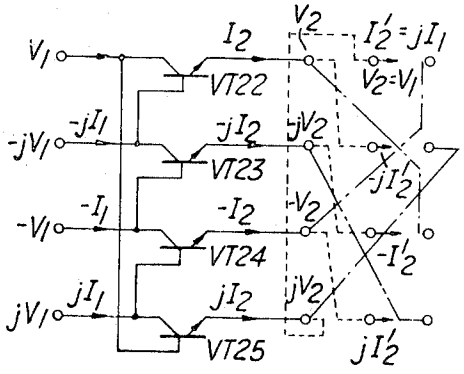


Fig. 25.

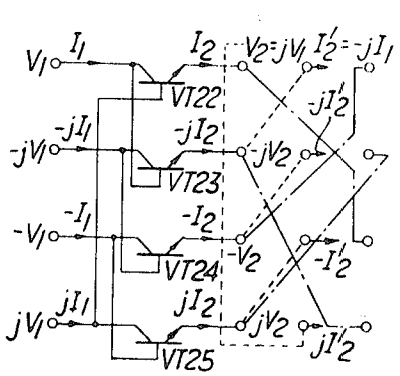


Fig. 26.

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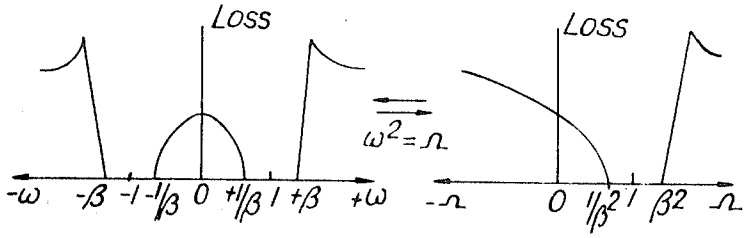


Fig. 27(A)

Fig. 27(B)

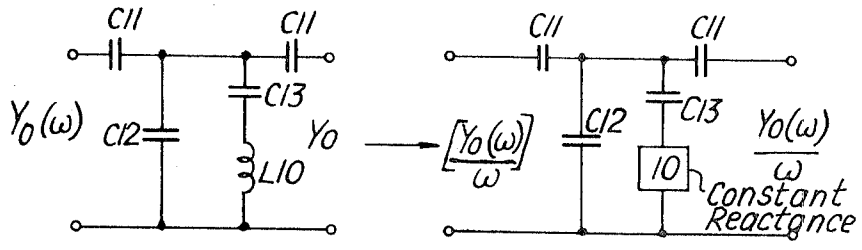
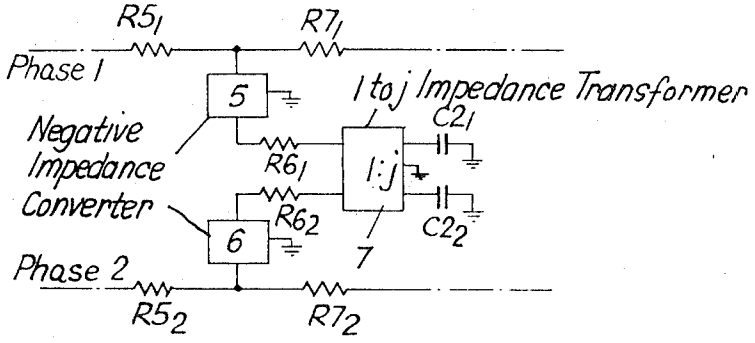


Fig. 28(A)

Fig. 28(B)

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Fig. 15



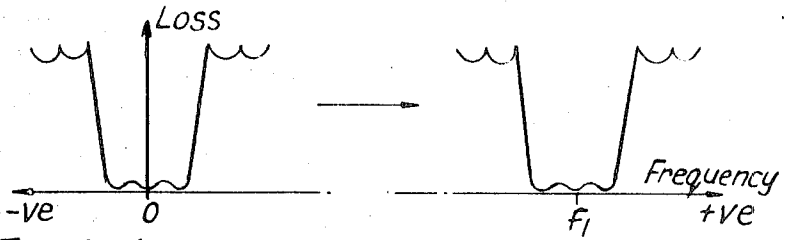


Fig. 29(A)

Fig. 29(B)

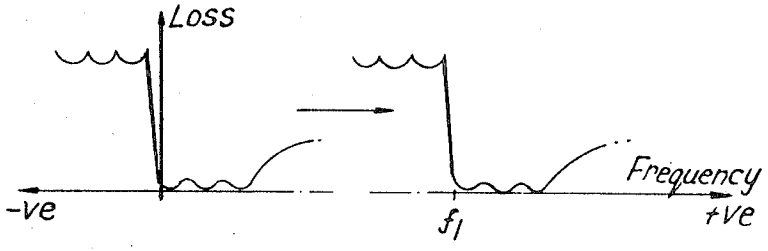


Fig. 30(A)

Fig. 30(B)

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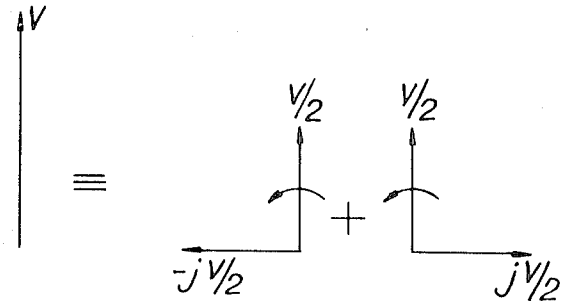


Fig. 31(A) Fig. 31(B) Fig. 31(C)

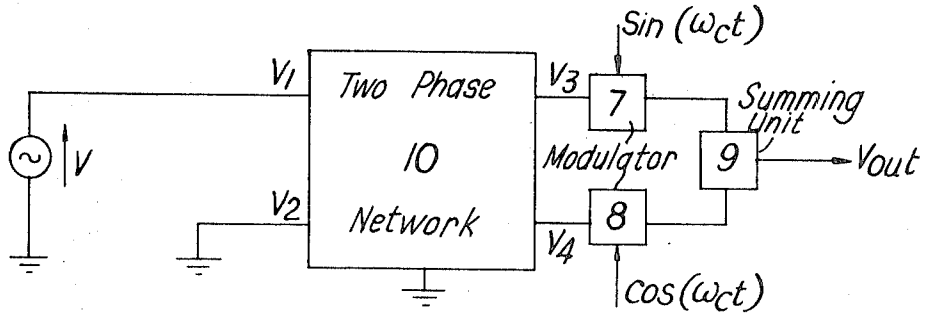


Fig. 32.

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SYMMETRICAL POLYPHASE NETWORKS UTILIZING CONSTANT REACTANCES

BACKGROUND OF THE INVENTION

The invention relates to polyphase networks and more particularly to symmetrical polyphase networks.

SUMMARY OF THE INVENTION

The term "constant reactance" as employed herein is defined as a reactance whose value remains constant with changes in the frequency of the signal applied thereto.

The term "positive frequency" as employed herein is defined as a counterclockwise sequence of vectors representing polyphase input signals.

The term "negative frequency" as employed herein is defined as a clockwise sequence of vectors representing polyphase input signals.

An object of the present invention is to provide a symmetrical polyphase network including constant reactances.

Another object of the present invention is to provide a symmetrical polyphase network including constant reactances such that the symmetrical polyphase network responds differently to input signals of negative and positive frequencies.

A feature of the present invention is the provision of a symmetrical polyphase network comprising N single-phase networks, one for each phase of an N-phase input signal, where N is an integer greater than one; each of said single-phase networks including at least one constant reactance so that the symmetrical polyphase network responds differently to input signals of negative and positive frequencies.

BRIEF DESCRIPTION OF THE DRAWING

The above-mentioned and other features and objects of this invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIGS. 1(A) and 1(B), respectively, illustrate positive and negative sequence four-phase vector diagrams;

FIG. 2 illustrates a positive sequence four-phase vector diagram;

FIG. 3(A) illustrates the frequency response curve of a simple third-order elliptic low-pass filter;

FIG. 3(B) illustrates the frequency response curve illustrated in the drawing according to FIG. 3(A) transformed into an asymmetric form;

FIG. 4 shows the gyrator realization of constant reactance;

FIG. 5 shows the controlled source representation of a gyrator;

FIG. 6 shows a method of realizing constant reactances in a four-phase system;

FIG. 7 shows the circuit diagram of a single-phase asymmetric-about-zero frequency filter;

FIG. 8 shows the circuit diagram of the polyphase realization of the circuit diagram of FIG. 7 for a two-phase system with quadrature inputs;

FIGS. 9(A) and 9(B), respectively, show circuit diagrams of the theoretical and practical realizations of a two-phase *1* to *j* impedance transformer of the voltage shift type;

FIGS. 10(A) and 10(B), respectively, show circuit diagrams of the theoretical and practical realizations of another two-phase voltage shift type *1* to *j* impedance transformer;

FIGS. 11(A) and 11(B), respectively, show circuit diagrams of the theoretical and practical realizations of a two-phase *1* to *j* impedance transformer of the current shift type;

FIGS. 12(A) and 12(B), respectively, show circuit diagrams of the theoretical and practical realizations of another two-phase current shift type *1* to *j* impedance transformer;

FIG. 13 shows the circuit diagram of a single-phase network which utilizes a plurality of constant reactances;

FIG. 14 shows the circuit diagram of the polyphase realization of the circuit diagram to FIG. 13 for a two-phase network with quadrature inputs;

FIG. 15 shows part of the circuit diagram of FIG. 14 together with negative impedance converters;

FIGS. 16, 17, 18 and 20, respectively, show the practical circuit diagrams of different forms of three-phase impedance transformers;

FIG. 19 shows the equivalent circuit diagram of one phase of the impedance transformer shown in FIG. 18;

FIG. 21 shows the circuit diagram of another single-phase network which utilizes a plurality of constant reactances;

FIG. 22 shows the circuit diagram of the polyphase realization of the circuit diagram of FIG. 21 for a three-phase network;

FIGS. 23 and 24 show equivalent circuit diagrams of one phase of the circuit diagram shown in FIG. 22;

FIGS. 25 and 26 show the circuit diagrams of different forms of four-phase impedance transformers;

FIGS. 27(A) and 27(B) show frequency response curves;

FIGS. 28(A) and 28(B) show circuit diagrams of a single-phase filter before and after transformation by image design techniques;

FIGS. 29(A) and (B) show frequency response curves for an N-path frequency translation system having low-pass filters connected in each of the N-paths thereof;

FIGS. 30(A) and (B) show frequency response curves for an N-path frequency translation system which utilizes the symmetrical polyphase networks according to the invention;

FIGS. 31(A) to (C) show vector diagrams; and quadrature inputs.

FIG. 32 shows the circuit diagram of a two-phase network with quadrature inputs.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In order to understand the operation of the symmetrical polyphase networks according to the present invention, the concept of negative frequency must be introduced. If a four-phase system is considered, which has as shown in FIG. 1(A) voltages of $V, -jV, -V, +jV$ applied to its four input terminals, then the input signal can be called symmetrical, since all voltages are equal in magnitude and spaced apart by steps of 90°, and of say positive sequence, since, conventionally, all vectors rotate anticlockwise and the voltage on path 1 leads the voltage on path 2 by 90°, and similarly, the voltage on path 2 leads the voltage on path 3 by 90°, etc. If now the vectors rotate the opposite way, i.e., as shown in FIG. 1(B), the system is still symmetrical, but is now of negative sequence (negative frequency), since the voltage on path 1 lags the voltage on path 2 by 90° instead of leading as before.

Considering the voltage on path 1 it can be seen from FIG. 2 that this voltage is $V \sin \omega t$, i.e., the projection of the vector 1 onto the imaginary axis when it is being rotated counterclockwise. When the sequence of vectors is reversed, $-V \sin \omega t$ will be observed. Since $-\sin \omega t = \sin(-\omega t)$, it can be said that, in a single-phase network, a positive sequence represents a positive ω and a negative sequence represents a negative ω. Thus, where positive and negative frequencies are hereinafter referred to with reference to the characteristics of a single-phase network, it means positive and negative sequence, respectively, in a polyphase network containing N single-phase networks.

In order to realize a polyphase network which has different magnitude responses to positive and negative sequence (positive and negative frequency) inputs, it is easiest to first consider a single-phase network having different magnitude responses to positive and negative frequencies. By its very nature such a single-phase network will not be physically realizable, since it is not possible to distinguish between positive and negative frequencies in a single-phase network containing real components. However, consideration of an asymmetric-about-zero frequency single-phase network can be used as a stepping stone to the synthesis of a polyphase network where positive and negative frequencies have a real significance and it will be seen that interconnections between the single-phase networks, so that each network "knows" what sequence of input has been applied, is necessary and sufficient for polyphase realization of the previously unrealizable single-phase network.

There are a variety of transforms that will change a symmetrical-about-zero frequency network to one that is asymmetric-about-zero.

By way of example, consider a simple third-order elliptic low-pass filter, the response of which is illustrated in FIG. 3(A). By making the transformation

$$\Omega=\frac{\omega}{1+\frac{\nu}{\omega_x}} \tag{1}$$

where ω is the frequency scale of the original filter, and

Ω is a new frequency scale,

the response is transformed into the asymmetric form illustrated in FIG. 3(B). As shown in FIG. 3(B) $\omega_x=\omega_\infty$ so that the peak that was at $-\omega_\infty$ (see FIG. 3(A)) is shifted to $\Omega=+\infty$ (see FIG. 3(B)). It is now possible to observe the effect of the above on realizability. The inverse transform of equation (1) is given by

$$\omega=\frac{\Omega}{1-\Omega/\omega_x} \tag{2}$$

Since the original network would have been constructed of coils and capacitors and resistively terminated, a coil which had an admittance of $1/j\omega L$ would, therefore, be transformed as below:

$$\frac{1}{j\omega L}=\frac{1-\Omega/\omega_x}{j\Omega L}=\frac{1}{j\Omega L}-\frac{1}{j\omega_x L} \tag{3}$$

The coil has, therefore, been transformed into a coil in parallel with a constant reactance. Similarly, a capacitor C would be transformed into a capacitor C in series with a constant reactance. However, since constant reactances are physically unrealizable in single-phase networks, the single-phase network is also unrealizable.

In the polyphase network according to the present invention, which contains N single-phase networks, it is possible to realize the constant reactance elements by means of, for example, gyrators, or sets of controlled sources, the latter being N-port gyrators.

Consider a two-phase system with quadrature inputs of V_{in} and jV_{in}. At any point in one of the two paths of the system there will be a voltage of V and a current of I. Since the two paths are physically identical, there will be at the corresponding point in the other of the two paths a voltage of jV and a current of jI.

Thus, if gyrator G1 is connected between the two phases, the two single-phase networks, in a symmetrical way as shown in FIG. 4, for example, it will have a voltage of V across port 5 and a voltage of jV across port 6. The gyrator must be symmetrical.

A symmetrical gyrator has the chain matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & \frac{+1}{gm} \\ gm & 0 \end{bmatrix} \cdot \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{4}$$

i.e., $$I_1=gmV_2, \quad \text{and} \quad I_2=+gmV_1 \tag{5}$$

Thus, the impedance seen looking into port 5 is

$$Z_1=\frac{V_1}{I_1}=\frac{V_1}{gmV_2}=\frac{V}{gm\cdot jV}=\frac{1}{jgm} \tag{6}$$

Similarly at port 6:

$$Z_2=\frac{V_2}{-I_2}=\frac{jV}{-gm\cdot V}=\frac{1}{jgm} \tag{7}$$

Therefore, it can be seen from equations (6) and (7) that looking into either port of gyrator G1 a reactance of $1/jgm$ is observed. Also, since the gyrator is a lossless element (theoretically), it is possible to construct lossless networks with their attendant low sensitivity (compared with active and passive R-C networks).

As shown in FIG. 5, gyrator G2 can be represented by two controlled sources, i.e., the constant current sources CCS1 and CCS2.

By using this representation, it is possible to envisage ways of extending the use of gyrators in systems having more than two phases. FIG. 6 shows a way of realizing constant reactances in a four-phase system with what is virtually a four-port gyrator.

For other than two or four phases, the arrangements are slightly more involved due to the complex relationship between voltages and currents of the single-phase circuits.

In practice the gyrator circuits are realized with transistors. As an example of the application of the above principles, consider the filter described hereinabove with reference to FIG. 3(B).

The single-phase version of this filter could take the form shown in FIG. 7 wherein coil L1 which is connected between one input and one output terminal is shunted by constant reactance X3 and capacitor C2, constant reactance X2 and capacitor C3 connected in series. The input terminals of the filter are shunted by capacitor C1 connected in series with constant reactance X1 and the output terminals are shunted by capacitor C4 connected in series with constant reactance X4.

The polyphase realization for a two-phase system with quadrature inputs is shown in FIG. 8 where it can be seen that four two-port gyrators G3 to G6 are utilized for the constant reactances of each one of the two phases.

One port of two-port gyrator G3 is used for one phase and is, therefore, connected in series between capacitors $C2_1$ and $C3_1$ across coil L1, while the other port of this gyrator is used for the other phase and is, therefore, connected in series between capacitors $C2_2$ and $C3_2$ across coil $L1_2$.

Similarly, the two-port gyrators G4 to G6 each have each one of the two ports thereof utilized for one of the two input phases, i.e., two ports of gyrator G4 are utilized with capacitors $C1_1$ and $C1_2$ to shunt the inputs of the two phases, the two ports of gyrator G5 are used to shunt coils $L1_1$ and $L1_2$, and the two ports of gyrator G6 is utilized with capacitors $C4_1$ and $C4_2$ to shunt the outputs of the two phases.

The gyrators and N-port gyrators used to realize constant reactances may be called polyphase-constrained networks, since the N terminals thereof are forced to carry voltages and currents which are always in N phases.

A further class of polyphase-constrained networks are those which include l to j impedance transformers to provide the constant reactances, where j is the conventionally employed mathematical symbol equal to $\sqrt{-1}$. (See page 479, "The International Dictionary of Physics and Electronics," 1956).

By way of example, consider the circuit diagram shown in FIG. 9(A) which shows a two-phase (quadrature) l to j impedance transformer of the voltage shift type having a constant current source (CCS3 or CCS4) in each phase thereof and the voltages and currents associated with each phase are as indicated. The phrase "l to j impedance transformer" means if impedances Z are placed on the output of each phase, in other words, looking into the inputs of the impedance transformer, impedances of jZ will be seen looking into either input from the output of the impedance transformer.

These networks which may be utilized as circuit elements to transform resistors into constant reactances are in practice realized with transistors as shown in FIG. 9(B). Each one of the two phases contains a transistor, i.e., transistors VT1 and VT2, having their collector-emitter circuits connected in series between the input and output terminals of the network.

The jV_1 voltage input to one of the two phases is also applied to the base of transistor VT1 in the other of the two phases by means of transistor VT3 having its base connected to the jV_1 voltage source, its collector connected to the base of transistor VT1 and to a negative electrical power supply via resistor R1 and its emitter connected to ground potential via resistor R2. The input voltage V_1 is applied directly to the base of transistor VT2.

Alternatively, the two-phase voltage shift type *1* to *j* impedance transformers may take the form shown in FIGS. 10(A) and 10(B). The equivalent circuit diagram of FIG. 10(A) shows the voltages and currents associated with each phase and the practical circuit diagram of FIG. 10(B) comprises a transistor in each one of the two phases, i.e., transistors VT4 and VT5 having their emitter-collector circuits connected in series between the input and output terminals of the network.

The jV_2 voltage output of one of the two phases is applied directly to the base of transistor VT4 and the output voltage V_2 of the other of the two phases is applied to the base of transistor VT5 in said one of the two phases by means of transistor VT6 having its base connected to the collector of transistor VT4, its collector connected to a negative electrical power supply via resistor R11 and to the base of transistor VT5 and its emitter connected to ground potential via resistor R10.

Examples of two-phase (quadrature) current shift types of *1* to *j* impedance transformers are shown in FIGS. 11(A) and 11(B) and FIGS. 12(A) and 12(B).

FIGS. 11(A) and 12(A) show the theoretical circuit diagrams and indicate the voltages and currents associated with each phase and do not require any further explanation.

FIG. 11(B) shows the practical circuit diagram for the theoretical circuit of FIG. 11(A) and comprises a transistor in each one of the two phases, i.e., transistors VT7 and VT8 having their emitter-base circuits connected in series between the input and output terminals of the network.

The base of the transistor VT7 is directly connected to the collector of transistor VT8 and the base of transistor VT8 is connected to the collector of transistor VT7 via transistor VT9 having its emitter connected to earth potential via resistor R12, its collector connected to the base of transistor VT8 and its base connected to the collector of transistor VT7 and to a positive electrical power supply via resistor R13.

FIG. 12(B) shows the practical circuit diagram for the theoretical circuit of FIG. 12(A) and comprises a transistor in each one of the two phases, i.e., transistors VT10 and VT11 having their base-emitter circuits connected in series between the input and output terminals of the network.

The base of transistor VT10 is connected to the collector of transistor VT11 via transistor VT12 having its emitter connected to ground potential via resistor R15, its base connected to a positive electrical power supply via resistor R14 and to the collector of transistor VT11, and its collector directly connected to the base of transistor VT10. The base of the transistor VT11 is directly connected to the collector of transistor VT10.

FIG. 13 shows the circuit diagram of a single-phase network which utilizes a large number of constant reactances X5, X6, X7, X8, X9...XM. The input to the network is shunted by capacitor C5, the output of the network is shunted by capacitor CN and constant reactances X6, X8...X(M−1) are respectively connected in series with capacitors C6, C7...C(N−1) between ground potential and the junction of the constant reactances X5 and X7, X7 and X9...X(M−2) and XM.

By utilizing any one of the *1* to *j* impedance transformers outlined in the preceding paragraphs, the polyphase version of the circuit diagram of FIG. 13 is shown in FIG. 14. This is a two-phase (quadrature) network having input phases Φ_1 and Φ_2 and input voltages V_{in} and jV_{in}.

The input to the single-phase circuits for Φ_1 and Φ_2 are, respectively, shunted by capacitors $C5_1$ and $C5_2$ while their outputs are respectively shunted by capacitors CN_1 and CN_2.

Since the 1 to *j* impedance transformers can be utilized as circuit elements to transform resistances into constant reactances, the T-networks of resistors $R5_1$, $R7_1$, and $R6_1$, and resistors $R5_2$, $R7_2$ and $R6_2$ are utilized in conjunction with the *j* to *1* impedance transformer 2 which is interposed between resistors $R6_1$, $R6_2$ and capacitors $C6_1$, $C6_2$ to provide the constant reactances X5, X6 and X7 of FIG. 13 in each phase of the two-phase network of FIG. 14.

Similarly, the *j* to *1* impedance transformer 3 is utilized in conjunction with the T-networks of resistors $R(M-2)_1$, RM_1 and $R(M-1)_1$ and resistors $R(M-2)_2$, RM_2 and $R(M-1)_2$ to provide the constant reactances X(M−2), XM and X(M−1) of FIG. 13 in each phase of the two-phase network of FIG. 14.

The *1* to *j* impedance transformer 1 interposed between the inputs to the network and resistors $R5_1$ and $R5_2$ is utilized to phase shift the inputs by *j* before they pass through the network and the *1* to *j* impedance transformer 4 interposed between resistors RM_1 and RM_2 and the outputs from the network corrects this phase shift before the signals are passed to the outputs of the network.

If, as is common, the reactances X6, X8, etc. are of opposite sign to the reactances X5, X7, X9, etc., it would be necessary to add negative impedance converters to the circuit diagram of FIG. 14 as shown in the circuit diagram of FIG. 15. Referring to FIG. 15, part of the circuit diagram of FIG. 14 is shown therein and includes negative impedance converters 5 and 6 which are, respectively, interposed between resistors $R6_1$ and the junction of resistors $R5_1$ and $R7_1$ and resistor $R6_2$ and the junction of resistors $R5_2$ and $R7_2$. Due to the use of the negative impedance converters which would be included in each of the resistance T-networks, it is necessary to change the *j* to *1* impedance transformers to *1* to *j* impedance transformers, e.g., transformer 7 (FIG. 15) for transformer 2 (FIG. 14).

The circuit diagram shown in FIG. 14 without the capacitors can be considered as an N-port gyrator which is lossless and passive although it may have to contain active devices to enable it to be realized.

FIGS. 16, 17, 18 and 20 show examples of practical circuit arrangements for three-phase constrained networks.

The three-phase constrained network according to FIG. 16 comprises a transistor in each of the three phases, each of the single-phase networks, i.e., transistors VT13 to VT15 having their collector-emitter circuits connected in series between the input and output terminals of the network. The base of transistor VT13 is connected to the collector of transistor VT15, the base of transistor VT14 is connected to the collector of transistor VT13 and the base of transistor VT15 is connected to the collector of transistor VT14.

This network which can be considered as a *1* to *h* impedance transformer has the chain matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} h & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{8}$$

$$\therefore Z_1 = \frac{V_1}{I_1} = hZ_2 \tag{9}$$

where Z_1 = input impedance
Z_2 = output impedance

$$h = \frac{1}{3}\sqrt{1} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} = e^{j2\pi/3} \tag{10}$$

Also,

$$h^2 = -\frac{1}{2} - j\frac{\sqrt{3}}{2} \tag{11}$$

$$h^3 = 1 \quad \text{or} \quad h = \sqrt[3]{1}$$

The three-phase constrained network of FIG. 17 is basically the same as the network of FIG. 16 except the bases of each of the transistors VT13 to VT15 are connected to the collector of the transistor in the subsequent instead of the preceding adjacent phase to provide a l to $1/h$ impedance transformer i.e., the base of transistor VT14 is connected to the collector of transistor VT15, the base of transistor VT15 is connected to the collector of transistor VT13 and the base of transistor VT13 is connected to the collector of transistor VT14.

This network has the chain matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1/h & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (13)$$

and

$$Z_1 = \frac{V_1}{I_1} = \frac{Z_2}{h} \quad (14)$$

FIG. 18 shows the practical circuit diagram of the three-phase constrained network which includes a transistor in each of the three phases, i.e., transistors VT16 to VT18 having their collector-emitter circuits connected in series between the input and output terminals of the network.

The interconnections between the three phases in order to provide a l to $-j\sqrt{3}$ impedance transformer is effected by three networks which each include a transistor, i.e., the transistors VT19 to VT21 having their collectors connected to a negative electrical supply and their emitters connected to ground potential, respectively, via bias resistors R17, R18 and R19.

The base of transistor VT19 is connected to the input voltage V_1 of one of the phases, i.e., to the collector of transistor VT16, the base of transistor VT20 is connected to the input voltage hV_1 of another one of the phases, i.e., to the collector of transistor VT17 and the base of transistor or VT21 is connected to the input voltage h^2V_1 of the other of the phases, i.e., to the collector of transistor VT18.

The emitter of transistor VT19 is also connected to the emitter of transistor VT20 via resistor R16 connected in series with resistor R16/2 and to the emitter of transistor VT21 via resistor R21/2 connected in series with a resistor R21. The junction of resistors R21 and R21/2 is connected to the base of transistor VT18 and the junction of resistors R16/2 and R16 is connected to the base of transistor VT16.

The emitter of transistor VT20 is also connected to the emitter of transistor VT21 via resistor R20 connected in series with resistor R20/2 and the junction of resistors R20 and R20/2 is connected to the base of transistor VT17.

The value of the resistances R16, R20 and R21 are arranged in conjunction with the transistors VT19 to VT21 such that a voltage of $jV_1/\sqrt{3}$ is applied to the base of transistor VT16, a voltage of hjV_1 is applied to the base of transistor VT17 and a voltage h^2jV_1 is applied to the base of transistor VT18.

This network has the chain matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} -j\sqrt{3} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (15)$$

and

$$Z_1 = \frac{V_1}{I_1} = -j\sqrt{3Z_2} \quad (16)$$

The equivalent circuit diagram of one phase of the circuit of FIG. 18 is shown in FIG. 19 from which, by way of example, the voltage applied to the base of the transistor which forms part of the first of the three phase will be established.

Consider transistors VT19 and VT20.

From FIG. 19 it can be seen that

$$I = \frac{(V_1 - hV_1)}{\frac{3}{2} \cdot R16} \quad (17)$$

and

$$V_0 = V_1 - IR16 \quad (18)$$

$$\therefore \frac{V_0}{V_1} = \frac{V_1 - IR}{V_1} = 1 - \frac{IR}{V_1} \quad (19)$$

From equations (17), (18) and (19)

$$\frac{V_0}{V_1} = 1 - \frac{(V_1 - hV_1)}{\frac{3}{2} \cdot R16 \cdot V_1}$$

$$= 1 - \tfrac{3}{2}(1-h)$$

$$\therefore \frac{V_0}{V_1} = \frac{1}{3} + \frac{2}{3}h. \quad (20)$$

From equations (10) and (20)

$$\frac{V_0}{V_1} = \frac{1}{3} + \frac{2}{3}\left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right)$$

$$V_0 = j\frac{V_1}{\sqrt{3}} \quad (21)$$

The three-phase constrained network of FIG. 20 is basically the same as the network of FIG. 18 except the three networks which each include one of the transistors VT19 to VT21 are arranged such that a l to $+j\sqrt{3}$ impedance transformer is provided, i.e., resistors R16/2, R20/2 and R21/2 are, respectively, replaced by resistors 2R16, 2R20 and 2R21, the junction of resistors R16 and 2R16 is connected to the base of transistor VT17, the junction of resistors R20 and 2R20 is connected to the base of transistor VT18 and the junction of resistors R21 and 2R21 is connected to the base of transistor VT16.

This network has the chain matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} j\sqrt{3} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (22)$$

and

$$Z_1 = \frac{V_1}{I_1} = +j\sqrt{3Z_2} \quad (23)$$

The electrical supply arrangements for each of the phases (single-phase networks) of the circuit diagrams of FIGS. 16, 17, 18 and 20 are not shown, but in practice would be arranged such that a predetermined potential difference exists between the collector and emitter, and the emitter and base of each of the transistors which form part of each of the phases. An example of how this may be achieved in practice will be outlined in a subsequent paragraph.

FIG. 21 shows the circuit diagram of a single-phase network which utilizes constant reactances X10 to X12. The input to the network is shunted by capacitor C8, the output is shunted by capacitor C9 and the constant reactance X12 is connected in series with capacitor C10 between ground potential and the junction of reactances X10 and X11. It is assumed that the constant reactance X12 is of opposite sign to the constant reactances X10 and X11.

By utilizing the l to h impedance transformers shown in FIG. 16, the three-phase version of the circuit of FIG. 21 is shown in FIG. 22.

Referring to FIG. 22, constant reactance X10 is provided in each phase by the l to h impedance transformer enclosed by the chain dotted line 11A and resistors $R10_{1/2}$ and $R10_1$ for

one of the three phases, resistors $R10_{2/2}$ and $R10_2$ for another of the three phases and resistors $R10_{3/2}$ and $R10_3$ for the other of the three phases. Constant reactance X11 is provided in each phase by the *l* to *h* impedance transformer enclosed by the chain dotted line 11B and resistors $R11_{1/2}$ and $R11_1$ for one of the three phases, resistors $R11_{2/2}$ and $R11_2$ for another of the three phases and resistors $R11_{3/2}$ and $R11_3$ for the other of the three phases.

Since constant reactance X12 is of opposite sign to constant reactances X10 and X11, it is necessary, as will be outlined in a subsequent paragraph with reference to FIGS. 23 and 24, to have two *l* to *h* impedance transformers, i.e., the transformers enclosed by the chain dotted lines 11C and 11D, associated with the three phases and resistors $R12_{1/2}$ and $R12_1$ for one of the three phases, resistors $R12_{2/2}$ and $R12_2$ for another of the three phases and resistors $R12_{3/2}$ and $R12_3$ for the other of the three phases.

The input to each phase is shunted by a capacitor, i.e., capacitor $C8_1$, $C8_2$ or $C8_3$, the output of each phase is shunted by a capacitor, i.e., capacitor $C9_1$, $C9_2$ or $C9_3$ and capacitor C10 of FIG. 21 is provided in each of the three phases by capacitors $C10_1$, $C10_2$ and $C10_3$.

The only difference between the *l* to *h* impedance transformers enclosed by the chain dotted lines 11A to D and the transformer shown in FIG. 16 is that resistor R22 is interposed between the base of transistor VT15 and the collector of transistor VT14, and constant current supply CCS5 is connected to the base of transistor VT15. These additional components together with constant current sources CCS6 which are connected between ground potential and the junction of resistors $R12_{1/2}$, $R12_{2/2}$ and $R12_{3/2}$ and capacitors $C10_1$ to 3 provide the necessary electrical supplies for the network.

Referring to FIG. 23, the equivalent circuit diagram of one phase of the network according to FIG. 22 is shown wherein it can be seen that resistors $R10_1$ and $R11_1$ are multiplied by *h*, respectively, by transformers 11A and 11B and resistor $R12_1$ is multiplied by h^2 by transformers 11C and 11D.

From equation (10), $h=-\frac{1}{2}+j\sqrt{3}/2$

From equation (10)

$$h=-\frac{1}{2}+j\frac{\sqrt{3}}{2}$$

$$\therefore \frac{R10_1}{2}+hR10_1=\frac{R10_1}{2}+\left[-\frac{1}{2}+j\frac{\sqrt{3}}{2}\right]R10_1 \quad (24)$$
$$=j\frac{\sqrt{3}}{2}R10_1$$

Similarly

$$\frac{R11_1}{2}+hR11_1=j\frac{\sqrt{3}}{2}R11_1 \quad (25)$$

From equation (11)

$$h^2=-\frac{1}{2}-j\frac{\sqrt{3}}{2}$$

$$\therefore \frac{R12_1}{2}+h^2R12_1=\frac{R12_1}{2}+\left[-\frac{1}{2}-j\frac{\sqrt{3}}{2}\right]R12_1 \quad (26)$$
$$=-j\frac{\sqrt{3}}{2}R12_1$$

The equivalent circuit diagram of FIG. 23 can, therefore, from equations (24), (25) and (26) be reduced to the equivalent circuit diagram shown in FIG. 24.

FIGS. 25 and 26 show examples of practical circuit arrangements for four-phase constrained networks. The electrical supply arrangements are not shown, but they may be provided in a similar manner to three-phase networks.

The four-phase constrained network of FIG. 25 comprises a transistor in each phase, i.e., transistors VT22 to VT25 having their collector-emitter circuits connected in series between the input and output terminals of the network. The bases of transistors VT22 to VT25 are, respectively, connected to the collectors of transistor VT23, VT24, VT25 and VT22.

The network without the dotted connections or the chain dotted connections is of the voltage shift type having the chain matrix.

$$\begin{bmatrix}V_1\\I_1\end{bmatrix}=\begin{bmatrix}j & 0\\0 & 1\end{bmatrix}\begin{bmatrix}V_2\\I_2\end{bmatrix} \quad (27)$$

$$\therefore Z_1=\frac{V_1}{I_1}=jZ_2 \quad (28)$$

When the dotted connections are added to the original network it will be of the current shift type and the chain matrix becomes

$$\begin{bmatrix}V_1\\I_1\end{bmatrix}=\begin{bmatrix}1 & 0\\0 & -j\end{bmatrix}\begin{bmatrix}V_2'\\I_2'\end{bmatrix} \quad (29)$$

and

$$Z_1=jZ_2 \quad (30)$$

When the chain dotted connections are added to the original network, i.e., crossing over the output leads of phases 1 and 3 and phases 2 and 4, the matrices of equations (27) and (29) are multiplied by −1.

The four-phase constrained network according to FIG. 26 is basically the same as the network according to FIG. 25 except the bases of transistors VT22 to VT25 are, respectively, connected to the collectors of transistors VT25, VT22, VT23 and VT24 to provide a *l* to $-j$ impedance transformer, therefore, the network without the dotted connections or the chain dotted connections is of the voltage shift type having the chain matrix

$$\begin{bmatrix}V_1\\I_1\end{bmatrix}=\begin{bmatrix}-j & 0\\0 & 1\end{bmatrix}\begin{bmatrix}V_2\\I_2\end{bmatrix} \quad (31)$$

and a chain matrix

$$\begin{bmatrix}V_1\\I_1\end{bmatrix}=\begin{bmatrix}1 & 0\\0 & j\end{bmatrix}\begin{bmatrix}V_2'\\I_2'\end{bmatrix} \quad (32)$$

when the dotted connections are added to the original network thereby providing a network of the current shift type.

As before, the chain dotted connections of FIG. 26 caused the matrices of equations (31) and (32) to be multiplied by −1.

It should be noted that the design of the single-phase network may be accomplished by the transformation of existing image network sections to asymmetric polyphase sections which may be accomplished by using known image design techniques, if the constant reactance is included as an extra circuit element.

Considering the symmetrical-about-zero frequency response shown in FIG. 27(A) where it can be seen that

$\omega=\pm\beta$ (33)

or $\omega=\pm 1/\beta$ (34)

or $\omega=0$ (35)

By making the transformation $\omega^2=\Omega$, the frequency response shown in FIG. 27(A) is transformed to the frequency response shown in FIG. 27(B) where it can be seen that.

$\Omega=\beta^2$ (36)

or $\Omega=1/\beta^2$ (37)

or $\Omega=0$ (38)

If all the admittances (Y) are multiplied by ω before frequency transformation then

$j\omega C\rightarrow j\omega^2 C\rightarrow j\Omega C$ (39)

and $1/j\omega L\rightarrow 1/jL\uparrow$ Y constant (40)

By way of example, consider the single-phase filter shown in FIG. 28(A) wherein the image impedance at the input and output are, respectively, represented by $Y_o(\omega)$ and Y_0. Then by this transform technique the circuit diagram is transformed to the circuit diagram shown in FIG. 28(B) where it can be seen that the capacitances C11 to C13 remain the same but the inductance L10 is transformed to a constant reactance represented by the block 10

i.e. $Y=1/j\omega L10 \rightarrow 1/jL10$

$jY=1/L10.$ (41)

If, however, all the admittances (Y) are divided by ω before frequency transformation then

$j\omega C \rightarrow jC \rightarrow Y$ constant (42)

and $1/j\omega L \rightarrow 1/j\omega^2 L \rightarrow 1/j\Omega L$ (43)

The insertion loss design of the single-phase network may also be accomplished by using the Z-transform method providing it is modified such that the transform takes account of both negative and positive frequencies.

The symmetrical polyphase networks outlined in the preceding paragraphs have a particular, but not necessarily an exclusive, application in the N-path frequency translation system outlined in British Pat. No. 1,098,250 and also in single sideband generation in a manner similar, but superior to conventional quadrature modulation.

The transfer function of the N-path frequency translation system is defined by

$V_0(p)=K\cdot H(p-p_1)\cdot V_1(p-p_1+p_2)$

where K is a constant.

$H(p)$ is the transfer function of the network(s) in the N paths

$P_1=j2\pi f_1$

$P_2=j2\pi f_2$

f_1 is the input switching rate

f_2 is the output switching rate

It can be seen that the transfer function $H(p)$ is shifted along the real frequency axis by an amount f_1. Normally, in the N-path filter system, where $p_1=p_2$, this would result in a band pass characteristic symmetrical about the frequency f_1. If low-pass filters are connected in the N paths, the resultant characteristic will be that of a shifted low-pass filter (including that at negative frequencies which is the mirror image of the positive frequency response). This is shown in the drawing according to FIGS. 29(A) and (B). Symmetrical characteristics are often very wasteful when modulation processes are involved. In such cases much more attenuation is needed on one side of the passband than the other. By using the symmetrical polyphase networks according to the invention, the characteristic can be made to fit the requirement more efficiently. Also, it is no longer necessary for the switching or carrier frequency to be at midband. FIGS. 30(A) and (B) illustrate this by way of example.

The symmetrical polyphase networks according to the invention may also be used for splitting a single-phase signal into N phases.

According to the theory of symmetrical components any unbalanced system of N vectors can be represented as the sum of N-symmetrical vector systems. If, for example, a two-phase (quadrature) system is considered with an input of V on one phase only, then this is equivalent to applying two opposite sequence two-phase signals simultaneously as shown in the drawings according to FIGS. 31(A) to (C). If the transfer function of the system is $H(p)$ to the vector system of FIG. 31(B) then it will be $H(-p)$ to the vector system of FIG. 31(C). FIG. 32 shows a two-phase system with an input on one phase only which includes a two-phase network 10 having the input V_1 for one phase thereof, i.e., phase 1 connected to voltage source V and the input V_2 for the other phase thereof, i.e., phase 2 connected to ground potential, i.e., $V_2=O$. The voltage output V_3 of phase 1 is connected via modulator 7 and summing unit 9 to the output and the voltage output V_4 of phase 2 is connected via modulator 8 and summing unit 9 to the output. A modulation signal $\sin(\omega_c t)$ is applied to modulator 7 and a modulation signal $\cos(\omega_c t)$ is applied to modulator 8.

At the output of phase 1, therefore,

$V_3=V/2(H(p)+H(-p))$

and on phase 2

$V_4=jV/2(H(p)-H(-p))$

If quadrature modulation is then applied to V_3 and V_4 as shown in FIG. 32 the resultant output is

$$V_0(p)=\frac{V(p\pm p_c)}{2}[H(p)+H(-p)\pm j(jH(p)-jH(-p))]$$

$$=H(p)V(p-p_c)+H(-p)V(p+p_c)$$

The effect is as if the modulation was done first, followed by a normal type of filter with the response $H(p+p_c)$. For this purpose the characteristic of the polyphase network would be as shown in FIG. 30. The lower sideband would then be suppressed while the upper sideband $V(p+p_c)$ would be passed. This basic method can be used for any number of phases.

It should be noted that it is possible to use the network of FIG. 32 without modulators and, thus, simply as a circuit to provide a two-phase output from a single-phase input. This is provided the network offers sufficient attenuation to negative sequence inputs and passes positive sequence inputs. FIG. 31 shows a suitable characteristic. In a similar manner, it is possible to generate an N-phase output from a single-phase input.

While I have described above the principles of my invention in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation to the scope of my invention as set forth in the objects thereof and in the accompanying claims.

1. A symmetrical polyphase network comprising:
N single-phase networks, a different one coupled to each phase of an N-phase input signal, where N is an integer greater than one;
each of said single-phase networks including
at least one constant reactance so that said polyphase network responds differently to input signals of negative and positive frequencies, the reactance value of said constant reactance being different than zero.

2. A polyphase network according to claim 1, wherein
each of said constant reactances includes
an N-port symmetrical gyrator, each of said N ports being coupled to a different one of said single-phase networks.

3. A polyphase network according to claim 1, wherein
each of said constant reactances includes
an N-phase l to j impedance transformer, where j is equal to $\sqrt{-1}$.

4. A polyphase network according to claim 3, wherein
said impedance transformer includes
N circuits each having
a transistor with its collector-emitter circuit connected in series between the input and output terminals of its associated one of said circuits, and its base coupled to the collector of said transistor in another one of said circuits.

5. A polyphase network according to claim 4, wherein
N is equal to four; and
the base of said transistor in one of said circuits is directly connected to the collector of said transistor in another of said circuits receiving as an input signal a signal lagging in phase with respect to the phase of the input signal coupled to said one of said circuits.

6. A polyphase network according to claim 4, wherein
N is equal to two;
said transistor of one of said circuits includes
a first transistor; and
said transistor of the other of said circuits includes
a second transistor, the base of said second transistor being directly connected to the collector of said first transistor; and further including
a third transistor network coupling the base of said first transistor to the collector of said second transistor.

7. A polyphase network according to claim 6, wherein
said third transistor network includes

a third transistor,
an electrical power supply,
a first resistor coupling the emitter of said third transistor to one terminal of said power supply providing a given potential,
means directly connecting the collector of said third transistor to the base of said first transistor,
a second resistor coupling the collector of said third transistor to the other terminal of said power supply providing a potential lower than said given potential, and
means directly connecting the base of said third transistor to the collect or of said second transistor.

8 A polyphase network according to claim 4, wherein
N is equal to three; and further including
a fourth transistor network coupling the collector of said transistor of each of said circuits to the base of said transistor of an adjacent one of said circuits.

9. A polyphase network according to claim 8, wherein
said fourth transistor network coupled to two adjacent ones of said circuits includes
an electrical power supply,
a fourth transistor having its base directly connected to the collector of said transistor in one of said two adjacent ones of said circuits and its collector directly connected to one terminal of said power supply providing a given potential,
a first resistor coupled between the emitter of said fourth transistor and the other terminal of said power supply providing a potential greater than said given potential, and
a potentiometer coupled between the emitter of said fourth transistor and the base of said transistor in the other of said two adjacent ones of said circuits,
said potentiometer including
a second resistor having a first terminal connected to the emitter of said fourth transistor and a second terminal, and
a third resistor having a first terminal directly connected to said second terminal of said second resistor and a second terminal connected to the emitter of a transistor included in said fourth transistor network coupled to another two adjacent ones of said circuits,
said second resistor having a value one-half of the value of said third resistor,
the base of said transistor in said other of said two adjacent ones of said circuits being directly connected to said second terminal of said second resistor and said first terminal of said third resistor.

10. A polyphase network according to claim 3, wherein
N is equal to two; and
said impedance transformer includes
two circuits each having
a transistor with its emitter-base circuit connected in series between the input and output terminals of its associated one of said circuits;
the base of said transistor in one of said circuits being directly connected to the collector of said transistor in the other of said circuits; and
a third transistor network coupling the base of said transistor in said other of said circuits to the collector of said transistor in said one of said circuits.

11. A polyphase network according to claim 10, wherein
said third transistor network includes
a third transistor;
an electrical power supply,
a first resistor coupling the emitter of said third transistor to one terminal of said power supply providing a given potential,
means directly connecting the base of said third transistor to the collector of said transistor of said one of said circuits,
a second resistor coupling the base of said third transistor to the other terminal of said power supply providing a potential higher than said given potential
means directly connecting the collector of said third transistor to the base of said transistor in said other of said circuits.

12. A polyphase according to claim 1, wherein
each of said constant reactances includes
an N phase l to $-j$ impedance transformer, where j is equal to $\sqrt{-1}$.

13. A polyphase network according to claim 12, wherein
N is equal to four; and
said impedance transformer includes
four circuits each having
a transistor with its collector-emitter circuit coupled in series between the input and output terminals of its associated one of said circuits and its base connected to the collector of said transistor in an adjacent one of said circuits receiving as an input signal a signal leading in phase with respect to the phase of the input signal coupled to said associated one of said circuits.

14. A polyphase network according to claim 12, wherein
N is equal to three; and
said impedance transformer includes
three circuits each having
a transistor with its collector-emitter circuit coupled in series between the input and output terminals of its associated one of said circuits, and a fourth transistor network coupling the base of said transistor of said associated one of said circuits to the collector of said transistor of said associated one of said circuits.

15. A polyphase network according to claim 14, wherein
said fourth transistor network includes
an electrical power supply,
a fourth transistor,
means directly connecting the base of said fourth transistor to the collector of said transistor of said associated one of said circuits,
means directly connected to one terminal of said power supply providing a given potential,
a first resistor coupling the emitter of said fourth transistor to the other terminal of said power supply providing a potential higher than said given potential,
a second resistor coupling the emitter of said fourth transistor to the base of said transistor of said associated one of said circuits, and
a third resistor coupling the junction of said second resistor and the base of said transistor of said associated one of said circuits to the emitter of a transistor included in said fourth transistor network of an adjacent one of said circuits,
the value of said third resistor being one-half the value of said second resistor.

16. A polyphase network according to claim 1, wherein
N is equal to three; and
said constant reactance includes
a three-phase impedance transformer of one of a three-phase l to h impedance transformer and a three-phase l to $1/h$ impedance transformer, where h is equal to $e^{j2\pi/3}$.

17. A polyphase network according to claim 16, wherein
both of said l to h and l to $1/h$ impedance transformers include
three circuits each having
a transistor with its collector-emitter circuit coupled in series between the input and output terminals of its associated one of said circuits and its base directly connected to the collector of said transistor of an adjacent one of said circuits;
a source of voltage V coupled to the first of said circuits;
a source of voltage Vh coupled to the second of said circuits;
and
a source of voltage Vh^2 coupled to the third of said circuits.

in each of said circuits the base of said transistor in said associated one of said circuits being directly connected to the collector of said transistor in an adjacent one of said circuits receiving as an input signal a signal leading in phase with respect to the phase of the input signal coupled to said associated one of said circuits.

19. A polyphase network according to claim 17, wherein said *l* to *1/h* impedance transformer includes

in each of said circuits the base of said transistor in said associated one of said circuits being directly connected to the collector of said transistor in an adjacent one of said circuits receiving as an input signal a signal lagging in phase with respect to the phase of the input signal coupled to said associated one of said circuits.

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