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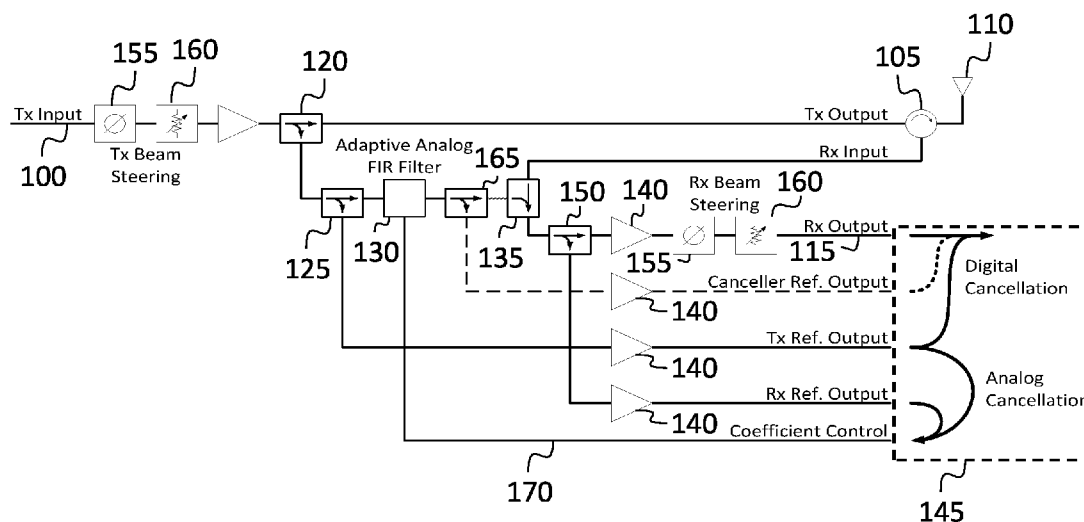


FIG. 1

(57) Abstract: A system for transmitting and receiving electromagnetic waves simultaneously. A portion of a signal to be transmitted through a transmitting antenna element is diverted from a transmit signal path, processed by an adjustable filter, and coupled into receive signal path. The adjustable filter is adjusted to approximate the channel that the leakage signals go through to get from the transmitter to the receiver so that the signal coupled into the receiving path through the filter partially cancels the parasitic leakage from the transmit signal path to the receive signal path.

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MICROWAVE ANALOG CANCELLATION FOR IN-APERTURE SIMULTANEOUS TRANSMIT AND RECEIVE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application is related to and incorporates by reference in its entirety, as if set forth in full, U.S. Patent Application Ser. No. 15/295,084, entitled "SYSTEM AND METHOD FOR ADAPTIVE SIMULTANEOUS TRANSMIT AND RECEIVE LEAKAGE CANCELLATION", filed on October 17, 2016 ("the '084 Application").

BACKGROUND

1. Field

[0002] One or more aspects of embodiments according to the present invention relate to a system for transmitting and receiving electromagnetic waves, and more particularly to a system and method for transmitting and receiving simultaneously.

2. Description of Related Art

[0003] In various commercial or military systems that transmit and receive electromagnetic waves, such as communications systems or radar systems, it may be useful to transmit and receive simultaneously. Coupling of the transmitted signal, which may be strong, into the receiver, which may otherwise receive only a relatively weak signal, may however interfere with simultaneous receiver operation and pose an obstacle to this mode of operation.

[0004] Thus, there is a need for a system and method for simultaneously transmitting and receiving electromagnetic waves.

SUMMARY

[0005] Aspects of embodiments of the present disclosure are directed toward a system for transmitting and receiving electromagnetic waves simultaneously. A portion of a signal to be transmitted through a transmitting antenna element is diverted from a transmit signal path, processed by an adjustable filter, and coupled into a receive signal path. The adjustable filter is adjusted to approximate the channel that the leakage signals go through to get from the transmitter to the receiver so that the signal coupled into the receiving path through the filter partially cancels the parasitic leakage from the transmit signal path to the receive signal path.

[0006] According to an embodiment of the present invention there is provided a transmit-receive phased array system for simultaneously transmitting and receiving, including: a transmit input for receiving a signal to be transmitted; a transmit output, operatively coupled to the transmit input, for producing a signal for an antenna

1 element; a receive input, for receiving a signal from the antenna element; a receive
output, for producing an analog corrected receive signal, the receive output
operatively coupled to the receive input through a receive signal path, an adjustable
filter having: an input operatively coupled to the transmit input and an output
5 operatively coupled to the receive signal path; a digitizer operatively coupled to, and
configured to digitize signals from: the receive output, the input of the filter; the
output of the filter; and the receive signal path, to form corresponding digitized
signals, and a processing circuit, configured to: control the adjustable filter so as to
10 partially cancel parasitic leakage from the transmit input to the receive output;
estimate an added noise and distortion component of the digitized receive output
signal to form a digital noise and distortion correction signal, the noise and distortion
component being due to effects from the adjustable filter; and subtract the digital
noise and distortion correction signal from the digitized receive output signal.

[0007] In one embodiment, the processing circuit is further configured to: digitally
15 filter the digitized signal from the output of the adjustable filter to form a digital
parasitic leakage correction signal; and subtract the digital parasitic leakage
correction signal from the digital receive output signal.

[0008] In one embodiment, the adjustable filter is an analog finite impulse
response filter.

20 **[0009]** In one embodiment, the analog finite impulse response filter is
implemented as a tapped delay line.

[0010] In one embodiment, the tapped delay line includes: a plurality of power
dividers, each having: an input; a first output; and a second output; a plurality of
delay elements, each connected to a respective power divider of the plurality of
25 power dividers; and a plurality of multipliers for respective tap weights, each
connected to a respective power divider of the plurality of power dividers; a second
delay element of the plurality of delay elements providing a delay twice as great as a
delay provided by a first delay element of the plurality of delay elements, and the
second delay element providing a delay twice as great as a delay provided by a third
30 delay element of the plurality of delay elements.

[0011] In one embodiment, the input of a second power divider of the plurality of
power dividers is connected to the first output of a first power divider of the plurality
of power dividers through a first attenuator, the first output of the second power
divider is connected to a multiplier for a first tap weight, of the plurality of multipliers
35 for respective tap weights, through a second attenuator, and the first output of a third
power divider is connected to a multiplier for a second tap weight, of the plurality of
multipliers for respective tap weights, through a third attenuator.

1 **[0012]** In one embodiment, each of: the multiplier for the first tap weight; and the multiplier for the second tap weight; is a vector modulator configured to receive two analog voltages representing the respective tap weight.

5 **[0013]** In one embodiment, the system includes a digital to analog converter connected to the processing circuit and to an analog input of each of the vector modulators.

10 **[0014]** In one embodiment, the system includes: a first directional coupler having: an input port connected to the transmit input, a coupled port, and a through port, and a second directional coupler having: an input port connected to the coupled port of the first directional coupler, a coupled port, and a through port, wherein the input of the adjustable filter is connected to the through port of the second directional coupler, and the input of the adjustable filter is operatively coupled to the transmit input through the first directional coupler and through the second directional coupler.

15 **[0015]** In one embodiment, the system includes a third directional coupler having: an input port connected to the output of the filter, a coupled port, and a through port, the coupled port being connected to the digitizer, and configured to provide, to the digitizer, the signal from the output of the filter.

20 **[0016]** In one embodiment, the adjustable filter includes a plurality of control inputs for setting a corresponding plurality of adjustable parameters, and the processing circuit is configured to calculate a plurality of parameter values and provide a plurality of corresponding signals to the control inputs.

25 **[0017]** In one embodiment, the processing circuit is configured to calculate the plurality of parameter values using a least mean squares method.

30 **[0018]** In one embodiment, the processing circuit is configured to calculate the plurality of parameter values using a recursive least squares filter.

35 **[0019]** According to an embodiment of the present invention there is provided a transmit-receive array, including a plurality of transmit-receive modules, each of the transmit-receive modules including: a transmit input for receiving a signal to be transmitted; a transmit output, operatively coupled to the transmit input, for producing a signal for an antenna element; a receive input, for receiving a signal from the antenna element; a receive output, for producing an analog corrected receive signal, the receive output operatively coupled to the receive input through a receive signal path, an adjustable analog filter having: an input operatively coupled to the transmit input and an output operatively coupled to the receive signal path; a digitizer operatively coupled to, and configured to digitize signals from: the receive output, the input of the filter; the output of the filter; and the receive signal path, to form corresponding digitized signals, and a processing circuit, configured to: control the adjustable filter so as to partially cancel parasitic leakage from the transmit input to

1 the receive output; estimate an added noise and distortion component of the
digitized receive output signal to form a digital noise and distortion correction signal,
the noise and distortion component being due to effects from the adjustable filter;
and subtract the digital noise and distortion correction signal from the digitized
5 receive output signal.

[0020] In one embodiment, the processing circuit of each of the transmit-receive
modules is further configured to: digitally filter the digitized signal from the output of
the adjustable filter of the transmit-receive module to form a digital parasitic leakage
correction signal; and subtract the digital parasitic leakage correction signal from the
10 digital receive output signal of the transmit-receive module.

[0021] In one embodiment, the adjustable filter of each of the transmit-receive
modules is an analog finite impulse response filter.

[0022] In one embodiment, the analog finite impulse response filter of each of the
transmit-receive modules is a tapped delay line.

15 BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Features, aspects, and embodiments are described in conjunction with the
attached drawings, in which:

[0024] FIG. 1 is a block diagram of a transmit-receive system, according to an
20 embodiment of the present invention;

[0025] FIG. 2 is a block diagram of a control and correction circuit, according to
an embodiment of the present invention;

[0026] FIG. 3A is a block diagram of a tapped delay line, according to an
embodiment of the present invention;

25 [0027] FIG. 3B is a block diagram of a tapped delay line, according to an
embodiment of the present invention;

[0028] FIG. 4A is a block diagram of a tapped delay line, according to an
embodiment of the present invention;

[0029] FIG. 4B is a block diagram of a tapped delay line, according to an
30 embodiment of the present invention; and

[0030] FIG. 5 is a block diagram of a linear array, according to an embodiment of
the present invention.

DETAILED DESCRIPTION

35 [0031] The detailed description set forth below in connection with the appended
drawings is intended as a description of exemplary embodiments of a system and
method for microwave analog cancellation for in-aperture simultaneous transmit and
receive for phased array RF systems provided in accordance with the present

1 invention and is not intended to represent the only forms in which the present
invention may be constructed or utilized. The description sets forth the features of
the present invention in connection with the illustrated embodiments. It is to be
understood, however, that the same or equivalent functions and structures may be
5 accomplished by different embodiments that are also intended to be encompassed
within the spirit and scope of the invention. As denoted elsewhere herein, like
element numbers are intended to indicate like elements or features.

[0032] Referring to FIG. 1, in some embodiments, a transmit-receive system
includes a transmit input 100, connected through a circulator 105 to an antenna
10 element 110. The antenna element 110 may transmit and receive simultaneously. A
received signal may travel from the antenna element 110 through the circulator 105
and along a receive signal path to a receive output 115.

[0033] Power may leak from the transmit input 100 to the receive output 115
through various mechanisms, such as by reflection from the antenna element or
15 through imperfect isolation of the circulator. Such leakage, referred to herein as
“parasitic” leakage (and which results in a signal, in the receive signal path, referred
to herein as a “parasitic” signal), may degrade the performance of the receiver, for
example by adding noise to the received signal, or causing distortion of the received
signal through nonlinear mechanisms.

[0034] Accordingly, a portion of the transmitted signal may be diverted (e.g., by a
20 first directional coupler 120), transmitted through a second directional coupler 125,
and filtered (e.g., by an adjustable filter 130) to form a correction signal, and the
correction signal may be coupled to the receive signal path, e.g., through a third
directional coupler 135. Each such directional coupler may have an input port, a
25 coupled port (to which a relatively small fraction of the input power is diverted) and a
transmitted or “through” port (to which most of the input power is transmitted). The
correction signal coupled into the receive signal path may be adjusted (e.g., in the
adjustable filter 130) to be substantially equal in amplitude and time to the parasitic
signal and substantially opposite in phase across some bandwidth of interest, so that
30 it partially (or substantially) cancels the parasitic leakage across some bandwidth of
interest. As used herein, the term “partially” when used to refer to a degree of
cancellation or subtraction includes any degree of cancellation or subtraction,
including perfect cancellation or perfect subtraction.

[0035] A further portion of the transmitted signal may be diverted, by the second
35 directional coupler 125 (from the portion of the transmitted signal diverted by the first
directional coupler 120), amplified by an amplifier 140 to form a transmit reference
signal, and fed into a control and correction circuit 145. Other signals fed to the
control and correction circuit 145 (discussed in further detail below) may also be

1 amplified by similar amplifiers 140. Similarly, a portion of the received signal may be
diverted from the receive signal path by a fourth directional coupler 150, and similarly
amplified to form a receive reference signal and fed into the control and correction
circuit 145. The control and correction circuit 145 may infer, e.g., by correlating the
5 receive reference signal and the transmit reference signal, the extent to which un-
canceled or “residual” parasitic signal remains in the receive reference signal, and it
may adjust the adjustable filter 130 (through a coefficient control connection 170) to
endeavor to further reduce the residual parasitic signal. This adjustment or
“adaptation” of the adjustable filter 130 may be performed continuously and in real
10 time by the control and correction circuit 145 during operation.

[0036] The adjustable filter 130 may have a plurality of adjustable parameters
(e.g., “tap weights”, and “tap spacing”, discussed in further detail below) that
determine the amplitude, time, and phase changes imparted by the adjustable filter
130 to the signal propagating through it. To determine the direction in which to adjust
15 the adjustable parameters of the adjustable filter 130, and the extent to which to
adjust them, the control and correction circuit 145 may employ a canonical
calculation or utilize adaptive algorithms, such as a least mean squares (LMS)
algorithm or a recursive least squares (RLS) algorithm. In this manner the system
may continually adapt the adjustable parameters of the adjustable filter 130, in real
20 time.

[0037] The through port of the fourth directional coupler 150 may be amplified by
an amplifier 140 and its amplitude and phase may be further adjusted by a beam
steering circuit (which may include an adjustable phase shifter 155 and an adjustable
attenuator 160) to form the signal at the receive output 115 which may be fed into
25 the control and correction circuit 145 or into the receiver of the RF system. In the
signal at the receive output 115, the effects of parasitic leakage may be largely
suppressed by the analog cancellation provided through the cancellation path
including the first directional coupler 120, the adjustable filter 130, and the third
directional coupler 135. The signal at the receive output 115 may be digitized, and
30 further cancellation may be performed digitally by the control and correction circuit
145, which may correlate the transmit reference signal with the signal at the receive
output 115, and then subtract a digital parasitic leakage correction signal (which may
be a digitally filtered version of the digitized transmit reference signal) from the
digitized signal at the receive output 115. The parameters of the digital filter used to
35 filter the digitized transmit reference signal may similarly be computed directly or
adjusted adaptively, e.g., using a least mean squares (LMS) algorithm, or “least
mean squares method” or a recursive least squares (RLS) algorithm.

1 **[0038]** The transmit-receive system of FIG. 1 may be part of an array of like
systems, (the antenna elements of which form, for example, an array antenna). The
transmitted signals may originate from a common source, and the relative amplitude
and phase of the signal transmitted by each element may be controlled by a beam
5 steering circuit (which, like the receive beam steering circuit, may include an
adjustable phase shifter 155 and an adjustable attenuator 160). The adaptation of
the adjustable parameters of the adjustable filter 130, and of the digital filter, may
also serve to cancel parasitic cross-coupling between elements of the array, e.g.,
coupling of a parasitic signal from the transmit input of a first transmit-receive system
10 of the array into the receive signal path of a second transmit-receive system of the
array, because this cross-coupled parasitic signal will also be correlated with the
transmit reference signal in the second transmit-receive system, and accordingly, the
control and correction circuit 145 of the second transmit-receive system will
endeavor to cancel it. In such a system, when the transmitter beam steering circuit is
15 adjusted, the adaptive algorithms of the control and correction circuit 145 may
automatically account for the change in amplitude or phase and dispersion of cross-
coupled parasitic signals that results by adjusting the adjustable parameters of the
adjustable filter 130, and of the digital filter, accordingly.

20 **[0039]** The adjustable filter 130 may include active elements, e.g., amplifiers, or
multipliers, and, in addition to imparting time, amplitude, and phase changes to the
signal propagating through it, the adjustable filter 130 may add unwanted noise or
distortion in or out of the bandwidth of the desired cancellation (referred to herein as
“filter noise”) to the signal, which may degrade the performance of the receiver.
Accordingly, the control and correction circuit 145 may estimate the additive noise
25 and distortion added from the analog canceller filter 130 to adjust the analog
cancellation coefficients 170 and the digital cancellation coefficients to perform a
noise canceling function. A fifth directional coupler 165 may be used to divert a
portion of the signal at the output of the adjustable filter 130, amplified to form a
canceler reference output signal, and fed into the control and correction circuit 145.
30 From the canceler reference output signal and the transmit reference signal, the
control and correction circuit 145 may form a digital noise correction signal (as an
estimate of the filter noise component in the signal at the receive output 115) and
subtract this digital noise correction signal from the signal at the receive output 115.
The control and correction circuit 145 may also estimate the filter noise and distortion
35 component by, for example, calculating, from the transmit reference signal and the
values of the adjustable parameters of the adjustable filter 130, what the signal at the
output of the adjustable filter 130 would be if the adjustable filter 130 were free of
noise and distortion, and subtracting this hypothetical signal from the signal

1 measured at the output of the adjustable filter 130, to estimate the noise and distortion at the output of the adjustable filter 130. In another embodiment, an adaptive algorithm (such as a least mean squares (LMS) algorithm or a recursive least squares (RLS) algorithm) is used to adjust the signal at the output of the
5 adjustable filter 130 (as measured by the canceler reference output signal) to match the computed ideal signal.

[0040] FIG. 2 shows the internal structure of the control and correction circuit 145, in one embodiment. Input signals 200, such as the receive reference signal and the canceler reference output signal, are digitized by a digitizer 202 (e.g., an analog to
10 digital converter), and the digital signals are processed (e.g., as described above) by a processing circuit 205 (discussed in further detail below). The processing circuit 205 may have a digital received signal output 210 for sending the corrected received signal (in which parasitic leakage is partially canceled and filter noise is partially subtracted) to a subsequent circuit, such as a portion of a communications system, a
15 client of a communications system, or a radar system. A digital to analog converter 215 may convert digital control signals from the processing circuit 205 to analog control signals 220 (i.e., parameter control signals or coefficient control signals) for the adjustable filter 130. In some embodiments the adjustable filter 130 is digitally controlled (e.g., it contains one or more analog to digital converters) and the control
20 outputs for it, from the control and correction circuit 145, are digital outputs. In such an embodiment the digital to analog converter 215 may be absent from the control and correction circuit 145.

[0041] Referring to FIG. 3A, in some embodiments, the adjustable filter 130 is an analog finite impulse response filter implemented as a 4-tap tapped delay line. In this
25 circuit power dividers 310a-c alternate with delay elements 315a-c. Each power divider 310a-c has a tap output that is connected to a multiplier 320a-c for a respective tap weight (i.e., a multiplier multiplying the signal transmitted through it by a respective tap weight). The final delay element 315c also has a tap output that is connected to a multiplier 320d for a respective tap weight. The products of the tap
30 output signals and the respective tap weights (i.e., the outputs of the multipliers 320a-d) may be combined by a combiner (not shown) to form the filter output. The tap weights may be the adjustable parameters, or “coefficients” of the adjustable filter 130.

[0042] FIG. 3B also shows a 4-tap tapped delay line embodiment of the
35 adjustable filter 130, according to another embodiment in which the delay line has a parallel topology. As in the case of the linear tapped delay line of FIG. 3A, the signal at the output of the second multiplier 320b, for example, propagates through one delay element 315b providing one unit (τ) of delay; the signal at the output of the

fourth multiplier 320d propagates through two delay elements 315a and 315c providing, (like the three delay units 315a-c between the input and the output of the fourth multiplier 320d of the linear tapped delay line of FIG. 3A) a total of three units (i.e., 3τ) of delay. The configuration of FIG. 3B may exhibit less loss than the configuration of FIG. 3A (with, for example, the splitter loss at the output of the fourth multiplier 320d being $2L_s$ in FIG. 3B and $3L_s$ in FIG. 3A), the splitter phase contributions may be the same at all taps (being $2\phi_s$ for each tap in the configuration of FIG. 3B, but ranging from ϕ_s to $4\phi_s$ in the configuration of FIG. 3A), and the amplitude variation across the taps may be lower in the configuration of FIG. 3B (the total loss being lower, for example, at the output of the fourth multiplier 320d) than in the configuration of FIG. 3A. The configuration of FIG. 3B may also make it possible to insert gain stages within the delay line without affecting the relative phases at the taps (as illustrated for example in FIGs. 4A and 4B, and discussed in further detail below).

[0043] Referring to FIG. 4A, the circuit of FIG. 3B may be generalized to an 8-tap tapped delay line that includes two 4-tap tapped delay lines 400 each similar to the one of FIG. 3B, fed by the two taps of a 2-tap tapped delay line 405 having a delay difference of four units (4τ) of delay between them. Each of the tap weights may be implemented using a respective vector modulator 410a-h; the outputs of the vector modulators may be combined in a combiner 415 (e.g., an 8-way combiner 415 constructed from two four-way combiners 420 and a two-way combiner 425).

[0044] Amplifiers 140 may be included at various stages in the tapped delay line to compensate for losses in the other components and avoid an unacceptable loss of signal to noise ratio. An attenuator 430 may be included at each output of each power divider 310a-g at which a delay element 315a-g is not present, to balance the loss of the delay element 315a-g at the other output. For example, an attenuator 430 may be coupled to a first output of power divider 310b and a delay element 315b may be coupled to a second output of power divider 310b. Attenuators 430 may also be used (e.g., at the input) to reduce the gain of an amplifier stage (e.g., if a commercial amplifier with a suitable gain is not readily available) and to improve reverse isolation.

[0045] Referring to FIG. 4B, in another embodiment, an 8-tap tapped delay line includes an 8-way power divider 435 feeding a set of 8 taps with tap weights implemented using vector modulators 410a-h, at the input of the parallel delay line. The parallel delay line of FIG. 4B has delay stages that are increasingly coarse in the direction from the input to the output, unlike the parallel delay line of FIG. 4A, which has delay stages that are increasingly fine in the direction from the input to the output. The circuit of FIG. 4A may be better suited for applications in which

1 preserving signal to noise ratio is important, whereas the circuit of FIG. 4B may be better suited for applications in which preserving dynamic range is important.

5 **[0046]** In one embodiment, each of the vector modulators may include two mixers, the radio frequency (RF) input of one of which may be fed with the signal at the RF input of the vector modulator and the other of which may be fed with the input RF signal phase-shifted by 90 degrees. The two respective intermediate frequency (IF) inputs of the two mixers may then be fed with two respective analog voltages corresponding to the in-phase and quadrature components of one of the tap weights 320a-h, so that the two analog voltages represent the complex tap weight. Each 10 vector modulator may for example be an HMC631LP3 vector modulator available from Analog Devices (www.analog.com). As used herein, the terms radio frequency and RF refer to any frequency suitable for being transmitted for received with an antenna element and an electronic circuit, and include without limitation microwave and millimeter wave frequencies, for example.

15 **[0047]** Referring to FIG. 5, in some embodiments a plurality of antenna elements 110 may be connected to a plurality of transmit-receive (TR) modules 605 (each including a circulator connected to the corresponding antenna element as shown in FIG. 1 in addition to analog cancellation circuitry) to form, for example, a five-element linear array. In such an array, embodiments of the present invention may be 20 employed to partially cancel parasitic leakage and parasitic cross-coupling, as discussed in further detail above.

[0048] The term “processing circuit” is used herein to include any combination of hardware, firmware, and software, employed to process data or digital signals. Processing circuit hardware may include, for example, application specific integrated 25 circuits (ASICs), general purpose or special purpose central processing units (CPUs), digital signal processors (DSPs), graphics processing units (GPUs), and programmable logic devices such as field programmable gate arrays (FPGAs). In a processing circuit, as used herein, each function is performed either by hardware configured, i.e., hard-wired, to perform that function, or by more general purpose 30 hardware, such as a CPU, configured to execute instructions stored in a non-transitory storage medium. A processing circuit may be fabricated on a single printed wiring board (PWB) or distributed over several interconnected PWBs. A processing circuit may contain other processing circuits; for example a processing circuit may include two processing circuits, an FPGA and a CPU, interconnected on a PWB.

35 **[0049]** It will be understood that when an element is referred to as being “connected to”, or “coupled to” another element, it may be directly connected to or coupled to the other element, or one or more intervening elements may be present. In contrast, when an element is referred to as being “directly connected to” or

1 “directly coupled to” another element or layer, there are no intervening elements present.

5 **[0050]** Although limited embodiments of a system and method for microwave analog cancellation for in-aperture simultaneous transmit and receive have been specifically described and illustrated herein, many modifications and variations will be apparent to those skilled in the art. Accordingly, it is to be understood that the system and method for microwave analog cancellation for in-aperture simultaneous transmit and receive employed according to principles of this invention may be embodied other than as specifically described herein. The invention is also defined in 10 the following claims, and equivalents thereof.

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WHAT IS CLAIMED IS:

1. A transmit-receive phased array system for simultaneously transmitting and receiving, comprising:
a transmit input for receiving a signal to be transmitted;
a transmit output, operatively coupled to the transmit input, for producing a signal for an antenna element;
a receive input, for receiving a signal from the antenna element;
a receive output, for producing an analog corrected receive signal, the receive output operatively coupled to the receive input through a receive signal path,
an adjustable filter having:
an input operatively coupled to the transmit input and
an output operatively coupled to the receive signal path;
a digitizer operatively coupled to, and configured to digitize signals from:
the receive output,
the input of the filter;
the output of the filter; and
the receive signal path,
to form corresponding digitized signals, and
a processing circuit, configured to:
control the adjustable filter so as to partially cancel parasitic leakage from the transmit input to the receive output;
estimate an added noise and distortion component of the digitized receive output signal to form a digital noise and distortion correction signal, the noise and distortion component being due to effects from the adjustable filter; and
subtract the digital noise and distortion correction signal from the digitized receive output signal.

2. The system of claim 1, wherein the processing circuit is further configured to:

digitally filter the digitized signal from the output of the adjustable filter to form a digital parasitic leakage correction signal; and
subtract the digital parasitic leakage correction signal from the digital receive output signal.

3. The system of claim 1, wherein the adjustable filter is an analog finite impulse response filter.

1 4. The system of claim 3, wherein the analog finite impulse response filter is implemented as a tapped delay line.

5 5. The system of claim 4, wherein the tapped delay line comprises:
a plurality of power dividers, each having:
 an input;
 a first output; and
 a second output;
a plurality of delay elements, each connected to a respective power divider of
10 the plurality of power dividers; and
a plurality of multipliers for respective tap weights, each connected to a
respective power divider of the plurality of power dividers;
a second delay element of the plurality of delay elements providing a delay
twice as great as a delay provided by a first delay element of the plurality of delay
15 elements, and
the second delay element providing a delay twice as great as a delay
provided by a third delay element of the plurality of delay elements.

20 6. The system of claim 5, wherein
the input of a second power divider of the plurality of power dividers is
connected to the first output of a first power divider of the plurality of power dividers
through a first attenuator,
the first output of the second power divider is connected to a multiplier for a
first tap weight, of the plurality of multipliers for respective tap weights, through a
25 second attenuator, and
the first output of a third power divider is connected to a multiplier for a
second tap weight, of the plurality of multipliers for respective tap weights, through a
third attenuator.

30 7. The system of claim 6, wherein each of:
the multiplier for the first tap weight; and
the multiplier for the second tap weight;
is a vector modulator configured to receive two analog voltages representing
the respective tap weight.

35 8. The system of claim 7, further comprising a digital to analog converter
connected to the processing circuit and to an analog input of each of the vector
modulators.

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9. The system of claim 1, further comprising:
a first directional coupler having:
an input port connected to the transmit input,
5 a coupled port, and
a through port, and
a second directional coupler having:
an input port connected to the coupled port of the first directional
coupler,
10 a coupled port, and
a through port,
wherein the input of the adjustable filter is connected to the through port of the
second directional coupler, and the input of the adjustable filter is operatively
coupled to the transmit input through the first directional coupler and through the
15 second directional coupler.

10. The system of claim 9, further comprising
a third directional coupler having:
an input port connected to the output of the filter,
20 a coupled port, and
a through port,
the coupled port being connected to the digitizer, and configured to provide, to
the digitizer, the signal from the output of the filter.

25 11. The system of claim 1, wherein:
the adjustable filter comprises a plurality of control inputs for setting a
corresponding plurality of adjustable parameters, and
the processing circuit is configured to calculate a plurality of parameter values
and provide a plurality of corresponding signals to the control inputs.

30 12. The system of claim 11, wherein the processing circuit is configured to
calculate the plurality of parameter values using a least mean squares method.

35 13. The system of claim 11, wherein the processing circuit is configured to
calculate the plurality of parameter values using a recursive least squares filter.

14. A transmit-receive array, comprising a plurality of transmit-receive
modules, each of the transmit-receive modules comprising:

1 a transmit input for receiving a signal to be transmitted;
a transmit output, operatively coupled to the transmit input, for producing a
signal for an antenna element;
a receive input, for receiving a signal from the antenna element;
5 a receive output, for producing an analog corrected receive signal, the receive
output operatively coupled to the receive input through a receive signal path,
an adjustable analog filter having:
an input operatively coupled to the transmit input and
an output operatively coupled to the receive signal path;
10 a digitizer operatively coupled to, and configured to digitize signals from:
the receive output,
the input of the filter;
the output of the filter; and
the receive signal path,
15 to form corresponding digitized signals, and
a processing circuit, configured to:
control the adjustable filter so as to partially cancel parasitic leakage
from the transmit input to the receive output;
estimate an added noise and distortion component of the digitized
20 receive output signal to form a digital noise and distortion correction signal, the noise
and distortion component being due to effects from the adjustable filter; and
subtract the digital noise and distortion correction signal from the
digitized receive output signal.

25 15. The array of claim 14, wherein the processing circuit of each of the
transmit-receive modules is further configured to:
digitally filter the digitized signal from the output of the adjustable filter of the
transmit-receive module to form a digital parasitic leakage correction signal; and
subtract the digital parasitic leakage correction signal from the digital receive
30 output signal of the transmit-receive module.

16. The array of claim 14, wherein the adjustable filter of each of the
transmit-receive modules is an analog finite impulse response filter.

35 17. The array of claim 16, wherein the analog finite impulse response filter
of each of the transmit-receive modules is a tapped delay line.

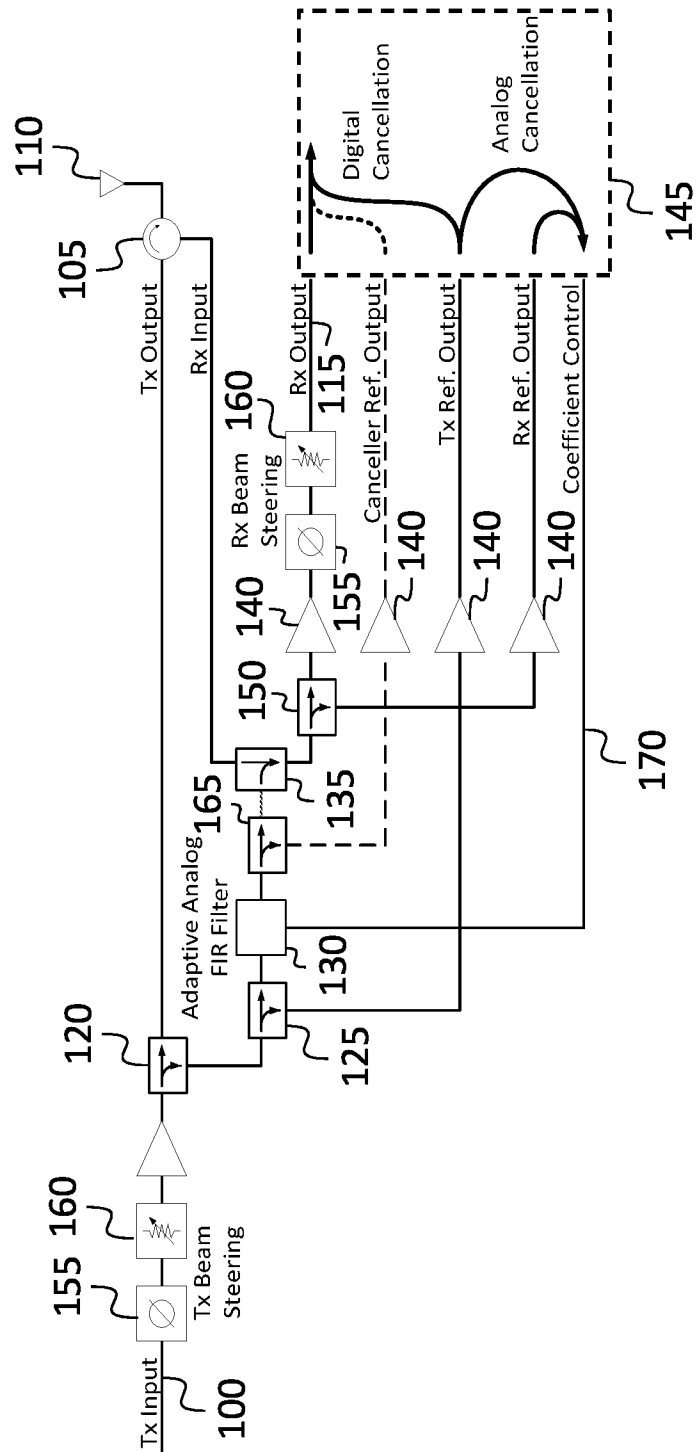


FIG. 1

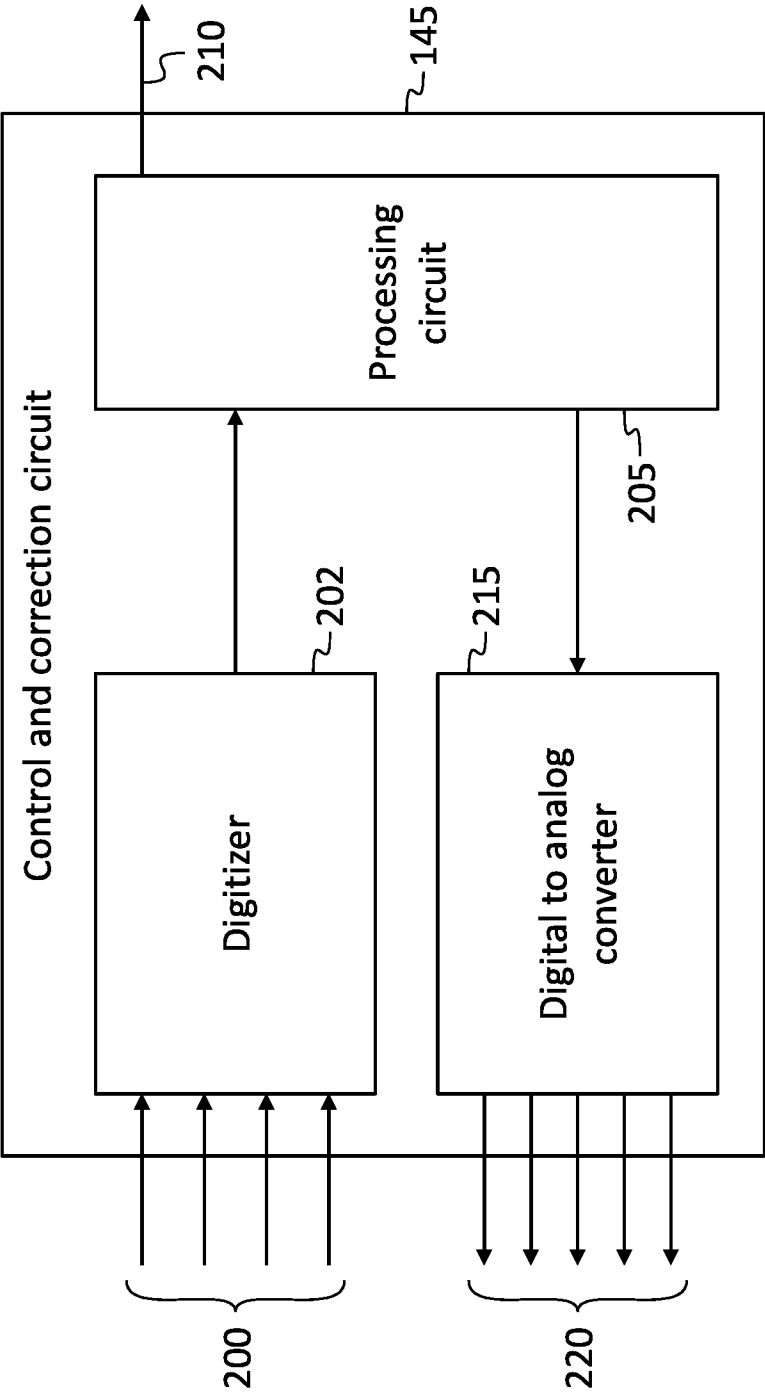


FIG. 2

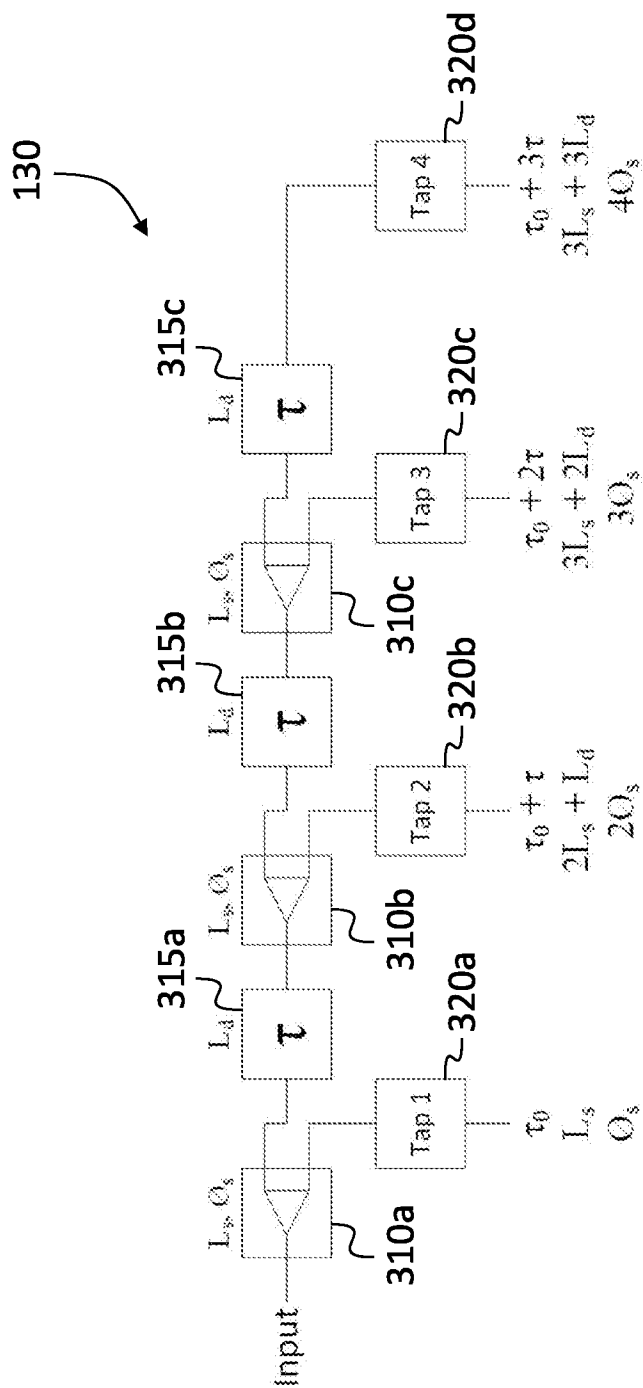


FIG. 3A

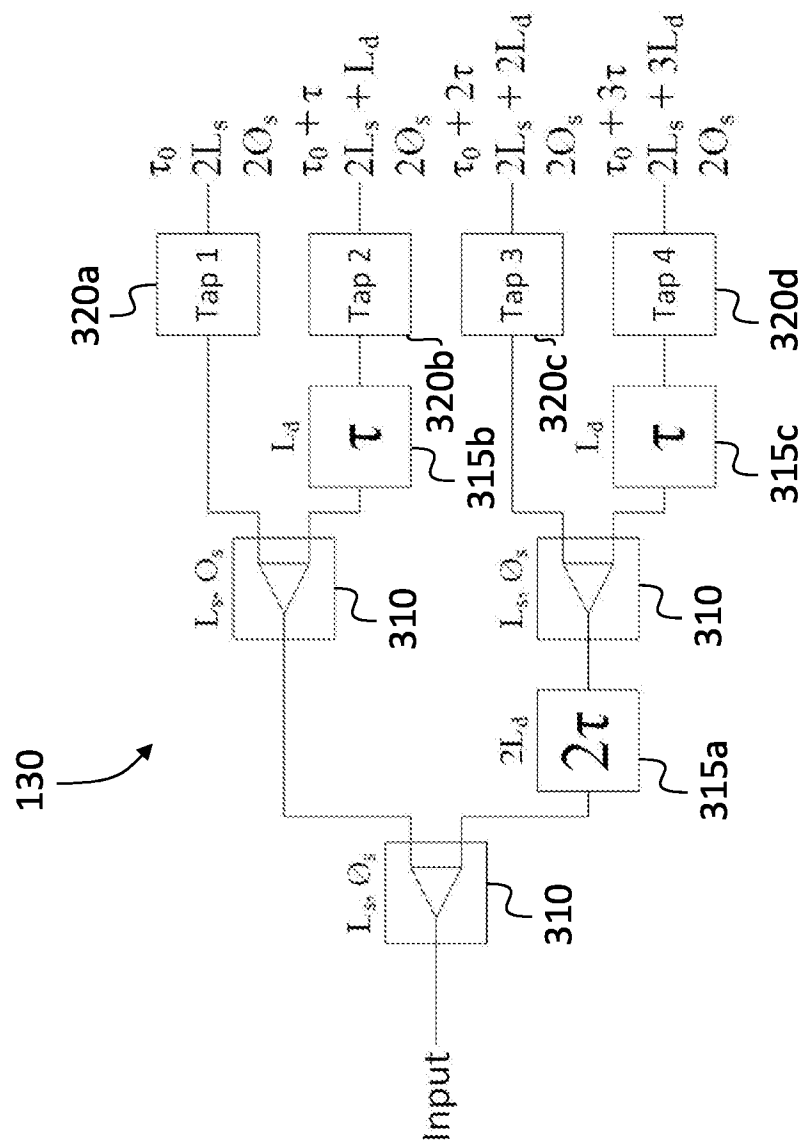
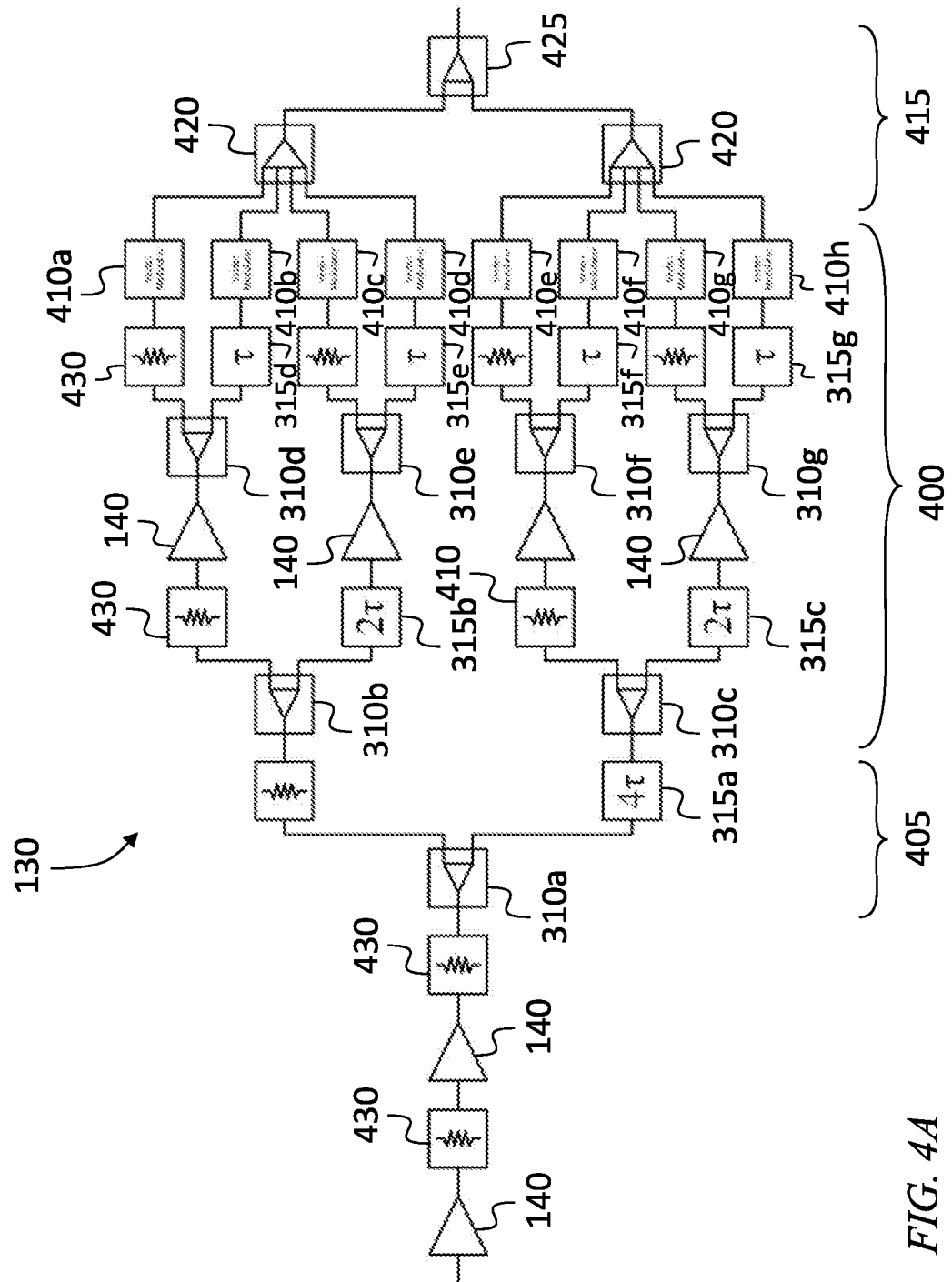


FIG. 3B



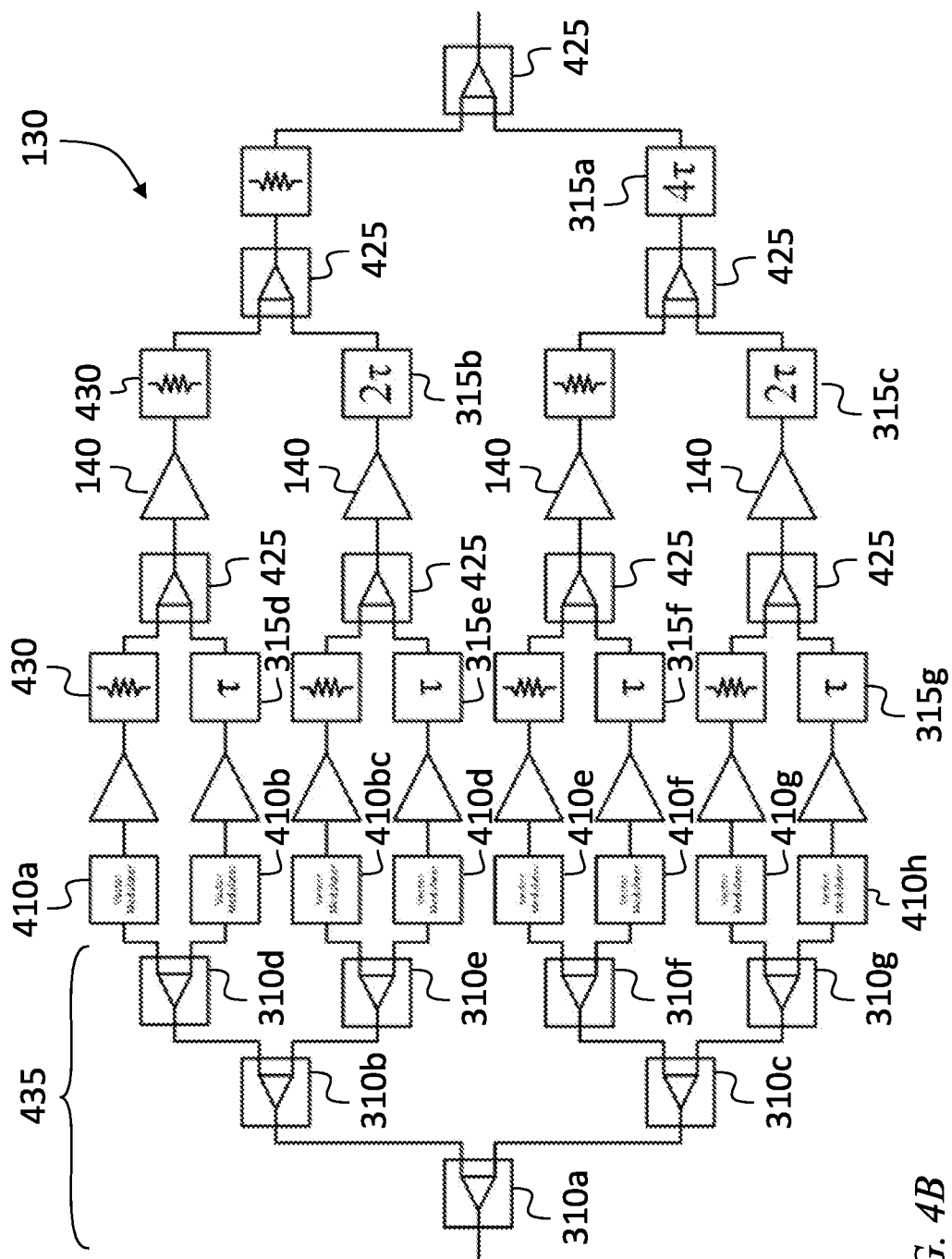


FIG. 4B

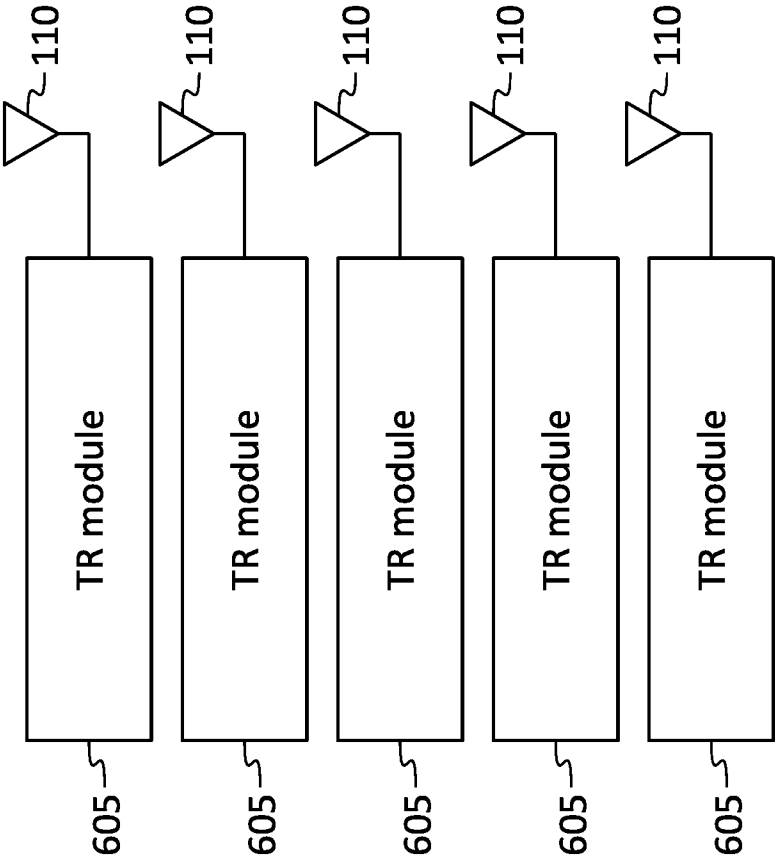


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/067853

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04B1/525
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2015/130257 A1 (INTEL CORP [US]; CHOI YANG-SEOK [US]; TALWAR SHILPA [US]) 3 September 2015 (2015-09-03) abstract paragraphs [0004] - [0006], [0023], [0034], [0045] - [0060]; figures 1-3 -----	1-17
X	WO 2015/021481 A2 (UNIV LELAND STANFORD JUNIOR [US]) 12 February 2015 (2015-02-12) abstract; figures 1,4-6 paragraphs [0084] - [0089]; claims 1-3 -----	1-17
A	US 6 812 824 B1 (GOLDINGER JAMES [US] ET AL) 2 November 2004 (2004-11-02) abstract; figures 17,18 columns 24-26 ----- -/--	1-17



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

5 April 2018

Date of mailing of the international search report

12/04/2018

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Authorized officer

Almenar Muñoz, M

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2017/067853

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/273952 A1 (KRIKORIAN KAPRIEL V [US] ET AL) 7 December 2006 (2006-12-07) abstract; figure 2 paragraphs [0016] - [0026] -----	1-17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2017/067853

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