(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 May 2014 (08.05.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/070779 A1

(51) International Patent Classification:
G06F 15/16 (2006.01) *H04B 17/02* (2006.01)
H04L 12/40 (2006.01)

(21) International Application Number:
PCT/US2013/067318

(22) International Filing Date:
29 October 2013 (29.10.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/720,306 30 October 2012 (30.10.2012) US
61/720,311 30 October 2012 (30.10.2012) US
61/720,321 30 October 2012 (30.10.2012) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) **Title**: ADDRESS BASED SERIAL COMMUNICATION INTERFACE FOR CONTROL AND MONITORING OF SYSTEM-ON-CHIP IMPLEMENTATIONS

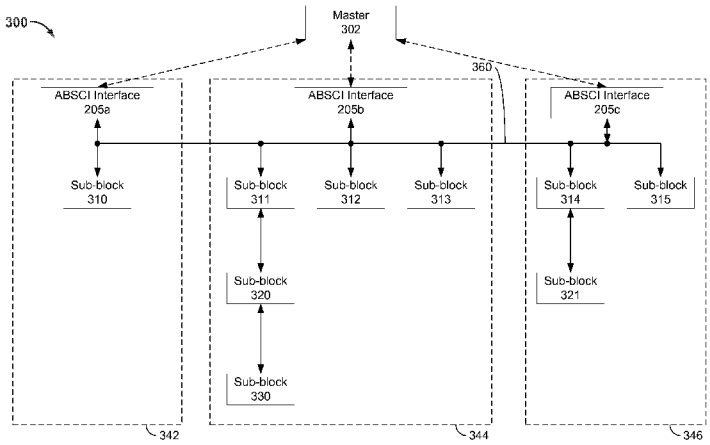

FIG. 3

(57) **Abstract**: A wireless data transceiver comprises a data bus, a first slave device and a second slave device. The first slave device and the second slave device are coupled to the data bus such that both devices can detect transmitted data packets. The transceiver further comprises an interface device coupled to the data bus. The interface device is configured to convert data formatted according to a first protocol to a second protocol, and vice-versa. The transceiver further comprises a first master controller and a second master controller coupled to the interface device. The first master controller receives first data formatted according to the second protocol and outputs data packets having a first slave address corresponding to the first slave device. The second master controller receives second data formatted according to the second protocol and outputs data packets having a second slave address corresponding to the second slave device.

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ADDRESS BASED SERIAL COMMUNICATION INTERFACE FOR CONTROL AND MONITORING OF SYSTEM-ON-CHIP IMPLEMENTATIONS

BACKGROUND

[0001] Transceivers receive and transmit signals using a variety of analog and/or digital components. The characteristics and performance of the analog and/or digital components can vary over time. For example, the internal temperature of the transceiver can affect the characteristic or performance of the analog and/or digital components.

[0002] Typically, transceivers can be designed to account for variations in the characteristics or performance of the analog and/or digital components. However, if a transceiver is built on silicon or a similar substrate, the design constraints can be very narrow. Such constraints can be even more restrictive when designing transceivers for low-power, high frequency applications.

[0003] Transceivers receive and transmit signals using a variety of analog and/or digital components. Often, the analog and/or digital components are monitored to ensure that they are working properly. To monitor the analog and/or digital components, circuits, such as biasing circuits, can be used to sample a signal passing through or outputted by the analog and/or digital components.

[0004] However, biasing circuits can affect the signal passing through the various analog and/or digital components. For example, biasing circuits can cause signal loss and/or introduce noise into the signal. In addition, conventional biasing circuits are fairly large. For example, some biasing circuits include between fifteen and twenty transistors. If a hundred or more points along the signal path are each being monitored by a biasing circuit, such overhead can significantly increase the size of a transceiver.

SUMMARY

[0005] It may be desirable to introduce digital controls around the analog and/or digital components to control the characteristic or performance of transceiver components. The digital controls can be used to both test components of the transceiver and adjust the characteristic or performance of one or more components during operation. The digital controls can be configured such that the characteristic

or performance of the one or more components are adjusted without interfering with the operation of the transceiver.

[0006] In some embodiments, the digital controls are implemented using an address based serial communication interface (ABSCI) protocol that interfaces with a serial peripheral interface (SPI) protocol or an inter-integrated circuit (I2C) protocol. The digital controls can include one or more master controllers. Master controllers may use the SPI or I2C protocol to transmit messages to an interface device, which then uses the ABSCI protocol to forward the messages to the various components to control the operation of the components that receive the messages. For example, one master controller can be configured to communicate with an interface device, which is configured to forward messages to a plurality of components using a single data bus. The master controller can construct messages that target a single component, two or more components, or all of the components. The components themselves may also act as master controllers, transmitting control messages to other components. The digital controls can include multiple master controllers, each master controller controlling the operation of a different part of the transceiver.

[0007] A biasing circuit is disclosed herein that reduces signal loss and minimizes noise introduced into the signal. Typical biasing circuits are constructed using solely passive elements (e.g., resistors, capacitors, etc.) or solely active elements (e.g., transistors). However, the biasing circuit disclosed herein includes both passive elements and active elements. Furthermore, the biasing circuit disclosed herein includes a compact design such that hundreds of points along the signal path can be monitored without significantly increasing the size of the transceiver.

[0008] One aspect of the disclosure provides a wireless data transceiver. The transceiver comprises a data bus. The transceiver further comprises a first layer comprising a first slave device. The first slave device may be coupled to the data bus such that the first slave device detects transmissions on the data bus. The transceiver further comprises a second layer comprising a second slave device, the second slave device coupled to the data bus. The transceiver further comprises an interface device coupled to the data bus. The interface device may be configured to convert first data packets formatted according to a first protocol to a second protocol

and to convert second data packets formatted according to the first protocol to the second protocol. The transceiver further comprises a first master controller coupled to the interface device. The first master controller may be configured to receive first data packets formatted according to the second protocol and to output third data packets having a first slave address corresponding to the first slave device. The transceiver further comprises a second master controller coupled to the interface device. The second master controller may be configured to receive second data packets formatted according to the second protocol and to output fourth data packets having a second slave address corresponding to the second slave device.

[0009] The wireless data transceiver of the preceding paragraph can have any sub-combination of the following features: where the first layer further comprises a third slave device, and where the first slave device is configured to output fifth data packets having a third slave address corresponding to the third slave device for reception by the third slave device; where the first slave device is configured to adjust a performance characteristic of the first slave device based on instructions included in the third data packets having the first slave address; where the first slave device is configured to transmit the first data formatted according to the first protocol to the interface device, and where the instructions included in the data packets having the first slave address are based on the first data; where the first slave device comprises: a slave controller configured to execute instructions included in the third data packets having the first slave address, an analog device coupled to the slave controller, where a characteristic of the analog device is controlled based on the instructions executed by the slave controller, a sensor coupled to the slave controller, where the sensor is configured to monitor the characteristic of the analog device and transmit measurements corresponding to the characteristic to the slave controller, and a bias circuit coupled between the analog device and the sensor, where the bias circuit is configured to reduce an amount of noise injected into the analog device by the sensor; where the bias circuit comprises a first transistor, and where a gate of the first transistor is coupled to the analog device; where the bias circuit further comprises a second transistor and a third transistor, where a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and where a source of the second transistor and a source of the third transistor are coupled to a supply voltage; where the bias circuit further comprises a fourth transistor and a low pass filter, where a drain of the third transistor and a drain

and a gate of the fourth transistor are coupled to the low pass filter, and where an output of the low pass filter is coupled to the sensor; where a signal at the output of the low pass filter is a representation of a signal at the gate of the first transistor; or where the first chip is an application layer chip, and where the second chip is a radio frequency (RF) analog front-end chip.

[0010] Another aspect of the disclosure provides a method for adjusting a characteristic of a wireless data transceiver. The method comprises transmitting, by a first slave device, first data formatted according to a first protocol to a master controller. The method further comprises receiving, by the first slave device from the master controller, a first instruction in a packet from a data bus. The first instruction may be generated based on the first data. The packet may have a destination address of a first slave address corresponding to the first slave device. The method further comprises adjusting, by the first slave device, a characteristic of the first slave device based on the first instruction. The method further comprises generating, by the first slave device, a second instruction based on the first instruction. The method further comprises transmitting, by the first slave device, the second instruction to a second slave device that adjusts a characteristic of the second slave device based on the second instruction.

[0011] The method of the preceding paragraph can have any sub-combination of the following features: receiving, by the first slave device from the master controller, a second packet from the data bus, where the second packet has a destination address of a second slave address corresponding to a third slave device, and discarding the second packet; receiving, by the first slave device from the master controller, a second packet from the data bus, where the second packet has a destination address of a broadcast address, and adjusting the characteristic of the first slave device based on instructions included in the second packet; where transmitting first data formatted according to a first protocol to a master controller comprises: obtaining a measurement of an analog device comprised within the first slave device using a bias circuit and a sensor, where the bias circuit is coupled between the analog device and the sensor, and where the bias circuit is configured to reduce an amount of noise injected into the analog device by the sensor, and generating the first data, where the first data comprises the measurement; where the bias circuit comprises a first transistor, and wherein a gate of the first transistor is coupled to the analog device; where the bias circuit further comprises a second

transistor and a third transistor, where a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and where a source of the second transistor and a source of the third transistor are coupled to a supply voltage; where the bias circuit further comprises a fourth transistor and a low pass filter, where a drain of the third transistor and a drain and a gate of the fourth transistor are coupled to the low pass filter, and where an output of the low pass filter is coupled to the sensor; where a signal at the output of the low pass filter is a representation of a signal at the gate of the first transistor; or where the first slave device is comprised within at least one of an application layer chip, a baseband chip, or a radio frequency (RF) analog front-end chip.

[0012] Another aspect of the disclosure provides a wireless data transceiver. The transceiver comprises a data bus. The transceiver further comprises a first slave device coupled to the data bus. The first slave device may be configured to read a first data packet comprising a first slave address and to transmit a second data packet. The transceiver further comprises an interface device coupled to the data bus. The interface device may be configured to convert the first data packet formatted according to the second protocol to the first protocol. The transceiver further comprises a master controller configured to transmit the first data packet to the interface device based on the second data packet received from the first slave device. The first data packet may comprise a first instruction. The first data packet may comprise a destination address of the first slave address. The interface device may be further configured to transmit the first data packet over the data bus. The transceiver further comprises a second slave device configured to receive a third data packet from the first slave device. The third data packet may comprise a second instruction. The first slave device may be configured to execute the first instruction. The second instruction may be based on the first instruction.

[0013] The wireless data transceiver of the preceding paragraph can have any sub-combination of the following features: where the first slave device is configured to adjust a performance characteristic of the first slave device based on the first instruction; where the first slave device comprises: a slave controller configured to execute the first instruction included in the first data packet having the first slave address, an analog device coupled to the slave controller, where a characteristic of the analog device is controlled based on the first instruction executed by the slave controller, a sensor coupled to the slave controller, where the

sensor is configured to monitor the characteristic of the analog device and transmit measurements corresponding to the characteristic to the slave controller, a bias circuit coupled between the analog device and the sensor, where the bias circuit is configured to reduce an amount of noise injected into the analog device by the sensor; where the bias circuit comprises a first transistor, and where a gate of the first transistor is coupled to the analog device; where the bias circuit comprises a second transistor and a third transistor, where a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and where a source of the second transistor and a source of the third transistor are coupled to a supply voltage; where the bias circuit comprises a fourth transistor and a low pass filter, where a drain of the third transistor and a drain and a gate of the fourth transistor are coupled to the low pass filter, and where an output of the low pass filter is coupled to the sensor; or where a signal at the output of the low pass filter is a representation of a signal at the gate of the first transistor.

[0014] Another aspect of the disclosure provides a bias circuit of a wireless data transceiver. The bias circuit comprises a first transistor. A gate of the first transistor may be configured to receive an input signal. The bias circuit further comprises a second transistor. The bias circuit further comprises a third transistor. A gate of the second transistor may be coupled to a gate of the third transistor and a drain of the first transistor. A source of the second transistor and a source of the third transistor may be coupled to a supply voltage. The bias circuit further comprises a fourth transistor. The bias circuit further comprises a low pass filter. A drain of the third transistor and a drain and a gate of the fourth transistor may be coupled to the low pass filter. An output of the low pass filter may be an output signal. The bias circuit may be configured to reduce an amount of noise injected into an analog or digital device when measuring a characteristic of the analog or digital device.

[0015] The bias circuit of the preceding paragraph can have any sub-combination of the following features: where the output signal is a representation of the input signal; where the input signal has a first frequency and the output signal has a second frequency, where the first frequency is greater than the second frequency; where the input signal is a signal in a radio frequency (RF) path of the analog or digital device; where the output signal is used to adjust the signal in the RF path of the analog or digital device; where a controller is coupled to the output of the

low pass filter to measure at least one of amplitude, gain, noise, phase, or variation of the signal in the RF path; where the input signal is isolated from the supply voltage; where the low pass filter comprises a resistor coupled between the drain of the fourth transistor and the output of the low pass filter, and where the low pass filter comprises a capacitor coupled between the output of the low pass filter and ground; or where a source of the first transistor and a source of the fourth transistor are coupled to ground.

[0016] Another aspect of the disclosure provides a bias circuit of a wireless data transceiver. The bias circuit comprises an active circuit configured to receive an input signal. The active circuit may comprise a decoupling circuit configured to decouple the input signal from a supply voltage. The bias circuit further comprises a passive circuit coupled to the active circuit. The passive circuit may be configured to filter the input signal and generate an output signal based on the filtered input signal. The bias circuit may be configured to reduce an amount of noise injected into an analog or digital device when measuring characteristics of the analog or digital device.

[0017] The bias circuit of the preceding paragraph can have any sub-combination of the following features: where the active circuit comprises a first transistor, a second transistor, a third transistor, and a fourth transistor, wherein a gate of the first transistor receives the input signal, where a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and where a source of the second transistor and a source of the third transistor are coupled to the supply voltage; where the passive circuit comprises a low pass filter, wherein a drain of the third transistor and a drain and a gate of the fourth transistor are coupled to the low pass filter, and where an output of the low pass filter is the output signal; where the low pass filter comprises a resistor coupled between the drain of the fourth transistor and the output of the low pass filter, and where the low pass filter comprises a capacitor coupled between the output of the low pass filter and ground; where a source of the first transistor and a source of the fourth transistor are coupled to ground; where the output signal is a representation of the input signal; where the input signal has a first frequency and the output signal has a second frequency, where the first frequency is greater than the second frequency; where the input signal is a signal in a radio frequency (RF) path of the analog or digital device; where the output signal is used to adjust the signal in the RF path of the analog or

digital device; or where a controller is coupled to an output of the passive circuit to measure at least one of amplitude, gain, noise, phase, or variation of the signal in the RF path.

[0018] Certain aspects, advantages and novel features of the inventions are described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment of the inventions disclosed herein. Thus, the inventions disclosed herein may be embodied or carried out in a manner that achieves or selects one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Throughout the drawings, reference numbers can be re-used to indicate correspondence between referenced elements. The drawings are provided to illustrate embodiments of the inventions described herein and not to limit the scope thereof.

[0020] Figure 1 illustrates a block diagram of an example MMW transceiver.

[0021] Figure 2 illustrates a block diagram of an example address based serial communication interface (ABSCI) control and monitoring system that includes an ABSCI interface device and one or more sub-blocks in communication with each other via an ABSCI data bus.

[0022] Figure 3 illustrates a block diagram of a layout of an example master device, ABSCI interfaces, and sub-blocks in a system on a chip (SoC).

[0023] Figure 4 illustrates a block diagram of a layout of example master devices, ABSCI interfaces, and sub-blocks in an SoC.

[0024] Figure 5 illustrates a block diagram of an example ABSCI sub-block.

[0025] Figure 6 illustrates an example bias-T circuit.

[0026] Figure 7 illustrates a chip diagram of an example sub-block.

[0027] Figure 8 illustrates an example packet generated by an ABSCI interface device.

[0028] Figure 9 illustrates an example ABSCI read path for one or more of the sub-blocks of Figure 2.

[0029] Figure 10 illustrates a schematic diagram of an example bus junction.

[0030] Figures 11-13 illustrate example automated start-up procedures for a phase lock loop (PLL).

[0031] Figure 14 illustrates a block diagram of an example switch controller.

[0032] Figure 15 illustrates a flowchart of an embodiment of a method for adjusting a characteristic of a wireless data transceiver.

[0033] Figure 16 illustrates an example docking system.

DETAILED DESCRIPTION

Introduction

[0034] Consumer electronics may be equipped with communication devices that permit the wireless transfer of data. For example, consumer electronics can include Wi-Fi chips to communicate via the IEEE 802.11 standard, Bluetooth chips to communicate via the Bluetooth communication protocols, or other such chips. As wireless communication technology has improved, more and more data is being transferred using wireless means.

[0035] Traditionally, large data files (e.g., audio files, video files, uncompressed image files, such as in the RAW format, etc.) have been transferred using conventional wired protocols even as wireless communication technology has improved due to the power consumption and delay associated with transferring such large data files. However, the ability to transfer large data files wirelessly from one electronic device to another may benefit both users and the manufacturers of electronic devices that manage these large data files if power consumption and delay can be reduced. Users may see a reduction in incompatibility issues between devices and less clutter. As for manufacturers, the connection ports and cables often dictate the shape and size of the electronic device. In fact, because cables and connectors should be large enough so that they can be handled by adult humans, electronic devices are often designed to be larger than they otherwise need

to be. Thus, the ability to transfer large data files wirelessly could significantly reduce the form factor of electronic devices that manage large data files.

[0036] Transceivers that communicate in the millimeter wave (MMW) frequencies may be able to handle the wireless transfer of large data files at high data rates and low power consumption. Accordingly, described herein are transceivers and components thereof that can achieve the goals described above. While aspects of the disclosure are described herein with respect to MMW frequencies, this is not meant to be limiting. As an example, MMW frequencies may be centered at 60 GHz, although higher and lower frequencies may also be considered MMW frequencies. However, the features described herein apply to any device that communicates at high frequencies (e.g., 2.4GHz, 5GHz, 20-120GHz, higher frequencies than 120GHz, frequencies less than 20GHz, and the like).

[0037] For instance, a MMW transceiver as described herein may include a control unit that uses a high-speed serial communication interface to control and monitor highly integrated system-on-chip (SoC) implementations that include one or more slave devices. Each slave device (or slave) may have a unique address and be connected to a bus. SoC's, like ultra-high speed radio transceivers (such as the MMW transceiver), may include a strong communication setup for different blocks within the chip to interact with each other. In certain embodiments, an address-based serial communication interface is described herein that may enable this intra-chip communication setup. When compared to two currently-available serial communication protocols available today (namely, serial peripheral interface (SPI) and the inter-integrated circuit (I2C) protocol), embodiments of this interface can offer significant advantages in terms of data rate, scalability, timing constraint flexibility, and/or ease of use in SoC applications. This interface may be especially beneficial for MMW applications, in which the time frame during which adjustments can be made is often very short. For example, under certain conditions, in an embodiment of the interface, a chip select line for some or all slaves is eliminated so that the number of slaves allowable is not limited (or is at least increased). For realizing speeds in excess of 250Mbps, some of the existing handshaking signals, such as an acknowledge signal, can be eliminated. Instead, the MMW transceiver can use system monitoring to ensure or attempt to ensure correct data transmission. The reduction in overhead may reduce power consumption and may be beneficial for low-power MMW applications.

[0038] In certain embodiments, the serial interface described herein can be used for systems (e.g., MMW transceivers) with a single master device (or master) and a scalable number of slave devices. Each of these slaves (or a subset thereof) can provide a robust interface for control and monitoring of any sub-system in the SoC with the underlying communication fabric. The system described herein may also support multiple masters, using (for example) an I2C (or SPI) interface block. Special broadcast modes are also described that, in certain embodiments, enable simultaneous configuration of some or all the slaves within a specified time. A software reset feature can also be implemented to reduce the number of IOs.

[0039] The I2C and SPI protocols were not designed for SoC applications (internal communication) and hence have significant overheads (e.g., contention-detection, acknowledge cycle, individual slave select line per slave, etc.) when used in intra-chip communication. This overhead leads to slower speeds, less flexibility, and higher overall cost in terms of power consumption and area.

[0040] The standard I2C serial communication protocol may include a two-wire interface. The protocol may use two open-drain wired-AND lines with external pull-up resistors. Each of the two wires has a driver circuit with sensing logic to identify contention issues. Data transmission occurs in bytes with some or all bytes followed up with an Acknowledge (ACK) cycle. I2C is half-duplex, and the maximum realizable throughput in some implementations is 3.4Mbps. Typical applications for I2C are memory and computer peripherals, which are mostly digital blocks. However, the standard I2C protocol is modified at least in part to become a modified I2C protocol for purposes of this disclosure.

[0041] The standard SPI protocol is a 4-wire, full-duplex serial communication interface. Multiple slaves are supported with individual Slave Select (SS) lines. Since a master initiates the communication with the slaves, there is no overhead in SPI due to arbitration logic. As a result, SPI can have throughputs of up to 70Mbps. However, this scheme typically uses one SS line for each slave SPI module and therefore tends to be less scalable. The SPI bus can be configured in a wired-OR configuration or can be daisy-chained. Typical applications for SPI include analog and mixed-signal blocks, such as analog-to-digital converters (ADCs), real time clock (RTC) generators, and brown-out detectors. However, the standard SPI

protocol is modified at least in part to become a modified SPI protocol for purposes of this disclosure.

[0042] As described above, typical biasing circuits include solely passive elements (e.g., resistors, capacitors, etc.) or solely active elements (e.g., transistors). However, limiting the biasing circuit to only passive elements or only active elements can cause problems. For example, using only passive elements can limit the range of the frequency band that the biasing circuit can handle. To compensate, the size of the biasing circuit may need to be increased. As another example, using only active elements can cause noise to be injected into the signal path.

[0043] Accordingly, a hybrid biasing circuit is disclosed herein, which includes both passive and active elements. The hybrid biasing circuit disclosed herein includes a compact design such that hundreds of points along the signal path can be monitored without significantly increasing the size of the transceiver. In fact, the hybrid biasing circuit disclosed herein exhibits characteristics that reduce or eliminate signal loss and/or the injection of noise in the radio frequency (RF) signal path of a MMW transceiver.

[0044] For ease of illustration, various features are described herein with respect to MMW transceivers. However, some or all of these features may also be implemented in other transceivers, receivers, or transmitters designed for wavelengths other than millimeter waves. Furthermore, for ease of illustration, this specification refers generally to systems implemented in SoCs. However, the features described herein may be more generally implemented in any integrated circuit (IC).

[0045] Further, the systems and methods described herein can be implemented in any of a variety of electronic devices, including, for example, cell phones, smart phones, personal digital assistants (PDAs), tablets, mini-tablets, laptops, desktops, televisions, digital video recorders (DVRs), set-top boxes, media servers, audio/visual (A/V) receivers, video game systems, high-definition disc players (such as Blu-ray® players), computer peripherals (such as mice, keyboards, scanners, printers, copiers, and displays), universal serial bus (USB) keys, cameras, routers, switches, other network hardware, radios, stereo systems, loudspeakers, sound bars, appliances, vehicles, digital picture frames, and medical devices, to name a few.

[0046] For purposes of summarizing this disclosure, certain aspects, advantages and novel features of several embodiments have been described herein. It is to be understood that not necessarily all such advantages can be achieved in accordance with any particular embodiment of the embodiments disclosed herein. Thus, the embodiments disclosed herein can be embodied or carried out in a manner that achieves one advantage or group of advantages as taught herein without necessarily achieving other advantages as taught or suggested herein.

MMW Transceiver Overview

[0047] Figure 1 illustrates a block diagram of an example MMW transceiver 100. As described above, the MMW transceiver 100 includes various input ports, output ports, analog components, and/or digital components. For example, as illustrated in Figure 1, the MMW transceiver 100 includes an RF_in port and an RF_out port. The RF_in port is configured to receive MMW signals transmitted by another device within a set frequency range (e.g., a MMW frequency range, such as 57-66GHz, etc.). The RF_out port is configured to transmit MMW signals to one or more devices within a set frequency range (e.g., a MMW frequency range, such as 57-66GHz, etc.).

[0048] The MMW transceiver 100 further includes components to process signals received via the RF_in port and/or generate signals to be transmitted via the RF_out port. For example, the MMW transceiver 100 includes PLL 102, LO 104, signal distribution block (e.g., splitter) 106, gain blocks 108 and 110, up-conversion frequency mixer 112, down-conversion frequency mixer 114, amplifiers 116, 118, 120, and 122, baseband (BB) blocks 124 and 126, mixed-signal modem 130, digital enhancement and control unit 140, and voltage regulator 150. In an embodiment, PLL 102 and LO 104 generate a LO signal that is passed to the signal distribution block 106 and the gain blocks 108 and 110. The signal distribution block 106 can be configured to distribute the LO signal to multiple components. Gain blocks 108 and 110 amplify the LO signal so that the LO signal can properly drive the frequency mixers 112 and/or 114. However, in other embodiments, as described herein, one of more of the gain blocks 108 and/or 110 can be removed.

[0049] In some embodiments, the MMW signal received via the RF_in port is passed to amplifier 118. As an example, amplifier 118 may be a low noise

amplifier (LNA). The amplifier 118 can adjust the amplitude of the received MMW signal and pass it to the down-conversion frequency mixer 114. The down-conversion frequency mixer 114 can down-convert the MMW signal from a MMW frequency to an intermediate frequency (IF) or a BB frequency using the LO signal. The down-converted signal then passes through amplifier 114 before being processed by the BB blocks 124.

[0050] Likewise, the MMW signal transmitted via the RF_out port is generated based on a signal generated by the BB blocks 126 that passes through amplifier 122 and the LO signal. In an embodiment, the signal generated by the BB blocks 126 is a BB or IF signal. The up-conversion frequency mixer 112 upconverts the BB or IF signal to a MMW signal using the LO signal. The MMW signal may pass through amplifier 116 before transmission occurs.

[0051] In some embodiments, the mixed-signal modem 130 is a digital component that transmits data to and receives data from other components of an electronic device (e.g., memory, a processor, etc.). For example, the data can be communicated via a 32-bit data bus. Data received by the mixed-signal modem 130 via the data bus can be transferred to the BB blocks 126. Likewise, data received by the mixed-signal modem 130 from the BB blocks 124 can be transferred to other components of the electronic device via the data bus.

[0052] Digital enhancement and control unit 140 provides digital means for controlling the various analog and/or digital components of the MMW transceiver 100. For example, digital enhancement and control unit 140 can adjust the characteristic or performance of the amplifier 118, the down-conversion frequency mixer 114, and so on.

[0053] In an embodiment, voltage regulator 150 generates an approximately constant voltage (e.g., 1.2V) that is supplied to one or more components of the MMW transceiver 100. The voltage regulator 150 may generate the approximately constant voltage based on an unregulated voltage (e.g., 3.3V) received via a port of the MMW transceiver 100.

Address-Based Serial Communication Interface for SoC Applications

[0054] Figure 2 illustrates a block diagram of an address based serial communication interface (ABSCI) control and monitoring system 200 that includes

an ABSCI interface device 205 and one or more sub-blocks 210a-N in communication with each other via an ABSCI data bus 220. In an embodiment, the ABSCI interface device 205 is a hardware processor or controller embedded in the digital enhancement and control unit 140. The sub-blocks 210a-N can be slave devices because they are controlled by a master device (not shown) that communicates with the ABSCI interface device 205. Each of the sub-blocks 210a-N can include an analog and/or digital component of the MMW transceiver 100, a hardware processor or controller, and/or other similar circuitry. The sub-blocks 210a-N are described in greater detail below with respect to Figure 5.

[0055] In a highly integrated SoC, like a wireless communication transceiver SoC (e.g., MMW transceiver 100), numerous sub-blocks 210a-N, spread across the entire chip (or a portion thereof), may be monitored and controlled for improved performance. Because the total number of read and write bits in many chips can be in the hundreds or thousands, it can be extremely inefficient to use one I2C/SPI block to route all the lines individually across the chip to each sub-block 210a-N. Thus, as described herein, one I2C/SPI block can interface with an ABSCI control and monitoring system that can provide efficient access to one or more of the sub-blocks 210a-N.

[0056] The ABSCI described herein can be a scalable control and monitoring solution for highly-integrated SoC systems that include transceivers like the MMW transceiver 100. As illustrated in Figure 2, the ABSCI interface device 205 is an example device used in the ABSCI control and monitoring system 200 to control N sub-systems (e.g., sub-blocks 210a-N) in the MMW transceiver 100 (where N is an integer). In an embodiment, each of the N sub-blocks 210 has a unique address (e.g., an m-bit address, where m is an integer and N is less than or equal to 2^m) that may be transmitted as part of the control data sequence.

[0057] The ABSCI control and monitoring system 200 may appear as a single SPI or I2C slave to an external controller (e.g., a controller operated by the digital enhancement and control unit 140, a controller located outside the MMW transceiver 100 in the SoC, etc.) that interacts with the SoC. For example, the ABSCI interface device 205 can be a block that interacts with the external controller via the standard SPI or I2C interface and that interacts with the sub-blocks 210a-N using the ABSCI data bus 220 and the ABSCI protocol described below.

[0058] In certain embodiments, the ABSCI interface device 205 is a three-way SPI, I2C, and ABSCI interfacing block configured to interface the high speed ABSCI data bus 220 described herein with the SPI and I2C protocols. The master device 205 can advantageously handle the exchange of data between three different clock domains in certain embodiments. For example, the SPI, I2C, and ABSCI protocols may each run on different clock domains. A data rate adaptation logic block, not shown, can also be provided.

ABSCI Control and Monitoring System Layout

[0059] Figure 3 illustrates a block diagram of a layout of a master device 302, ABSCI interfaces 205a-c, and sub-blocks 310-315, 320-321, and 330 in SoC 300. As illustrated in Figure 3, master device 302 communicates with ABSCI interfaces 205a, 205b, and/or 205c. In an embodiment, master device 302 is an external controller (e.g., a processor) located outside an ABSCI control and monitoring system that uses the standard SPI or I2C protocol. Each ABSCI interface device 205a-c communicates with one or more sub-blocks 310-315 via ABSCI data bus 360 in the depicted embodiment. Furthermore, sub-block 311 may communicate with sub-block 320, sub-block 320 may communicate with sub-block 330, and sub-block 314 may communicate with sub-block 321. In some embodiments, one of more of sub-blocks 311, 320, 330, 314, and/or 321 communicate with other sub-blocks using the ABSCI data bus 360. In other embodiments, one or more of sub-blocks 311, 320, 330, 314, and/or 321 communicate with other sub-blocks using an ABSCI data bus other than the ABSCI data bus 360. Thus, sub-blocks like sub-blocks 311, 320, 314 can act both as a slave device (e.g., by receiving instructions from master device 302) and as a master device (e.g., by providing instructions to other sub-blocks 320, 321, and 330). A given sub-block may act as both a slave and a master at the same time or at different times.

[0060] In an embodiment, the ABSCI control and monitoring system controls and monitors sub-blocks spread over multiple chips 342, 344, and 346. For example, chips 342, 344, and 346 may be separate portions of the MMW transceiver 100. Chip 342 could be the application layer of the MMW transceiver 100. Chip 344 could be the BB (e.g., physical layer and data link layer) of the MMW transceiver

100. Chip 346 could be the RF analog front end of the MMW transceiver 100. In order to support standard serial interfaces, an ABSCI interface device 205a-c is provided in one or more of chips 342, 344, and 346. For example, the master device 302 communicates with one of ABSCI interfaces 205a-c, which serves as an interface to the sub-blocks 310-315. As another example, the master device 302 communicates with some or all of the ABSCI interfaces 205a-c, which each serve as an interface for the sub-blocks 310-315 in the same chip 342, 344, or 346. In some embodiments, one or more of the ABSCI interfaces 205a-c can transfer fully duplex data (or half-duplex data) and control signals from external SPI/I2C master devices, such as master 302, to the sub-blocks 310-315, 320-321, and/or 330 and hence serve as terminal blocks for the on-chip ABSCI data bus 360.

[0061] In some embodiments, the SoC allows the ABSCI control and monitoring system to function in a multi-master environment. Figure 4 illustrates a block diagram of a layout of master devices 402, 404, and 406, ABSCI interfaces 405a-c, and sub-blocks 310-315, 320-321, and 330 in SoC 400. As illustrated in the example embodiment of Figure 4, master device 402 communicates with ABSCI interfaces 205a, master device 404 communicates with ABSCI interface device 205b, and master device 406 communicates with ABSCI interface device 205c. Master devices 402, 404, and 406 may be similar to master device 302 of Figure 3. In other embodiments, not shown, master devices 402, 404, and 406 each communicate with the same ABSCI interface device 205a-c.

[0062] In some embodiments, ABSCI interface device 205a communicates with sub-blocks 310 and 311 via ABSCI data bus 460, ABSCI interface device 205b communicates with sub-blocks 312 and 313 via ABSCI data bus 470, and ABSCI interface device 205c communicates with sub-blocks 314 and 315 via ABSCI data bus 480. Furthermore, the sub-blocks 310-315, 320-321, and 330 may communicate with each other as described above with respect to Figure 3. In other embodiments, not shown, each ABSCI interface device 205a-c communicates with the respective sub-blocks 310-315, 320-321, and/or 330 using the same ABSCI data bus 460, 470, or 480.

[0063] In an embodiment, at least some master devices are associated with a chip 342, 344, or 346 of the MMW transceiver 100 and provide instructions or otherwise communicate only with the sub-blocks of that chip. For example, master

device 406 is associated with chip 346 and communicates indirectly only with sub-blocks 314, 315, and/or 321. In further or alternative embodiments, at least some master devices are associated with a portion of a chip 342, 344, or 346 of the MMW transceiver 100 and provide instructions or otherwise communicate at least with one sub-block of that chip. For example, master device 404 is associated with chip 344 and communicates indirectly with sub-blocks 312 and 313, but not with sub-blocks 311, 320, or 330. In further or alternative embodiments, at least some master devices are associated with a plurality of chips 342, 344, or 346 of the MMW transceiver 100 and provide instructions or otherwise communicate at least with one sub-block of the plurality of chips. For example, master device 402 is associated with chips 342 and 344 and communicates indirectly with sub-blocks 310, 311, 320, and/or 330.

[0064] Having multiple master devices in a SoC may provide several benefits. For example, multiple master devices allow for the simultaneous or nearly simultaneous control and adjustment of different portions of the SoC. One master device can control a first portion of the SoC, such as the application layer, and another master device can control simultaneously or nearly simultaneously a second portion of the SoC, such as the baseband layer. As another example, by associating sub-blocks with different master devices, one or more sub-blocks can receive instructions more quickly because the master devices have fewer sub-blocks to communicate with. Thus, the performance of the SoC can be improved more quickly. As another example, the presence of multiple master devices can reduce the number of lines placed throughout the SoC. With master devices interspersed throughout the SoC, each master device can be placed physically closer to the sub-blocks, thereby reducing the number of lines.

ABSCI Sub-Blocks

[0065] Figure 5 illustrates a block diagram of an ABSCI sub-block, which is a more detailed example embodiment of the sub-block 210 of Figure 2. As illustrated in Figure 5, the sub-block 210 includes a controller 504, an analog and/or digital component 506, a bias-T circuit 508, and a sensor 510. The sub-block 210 communicates with the ABSCI interface device 205 via the ABSCI data bus 220.

[0066] In an embodiment, the controller 504 (e.g., a hardware processor) receives instructions from the ABSCI interface device 205 over the ABSCI data bus 220 and sends messages back to the ABSCI interface device 205 (which may be forwarded to the external controller or master device). Messages transmitted between the ABSCI interface device 205 and the controller 504 may be communicated with the ABSCI protocol, described in greater detail below.

[0067] The analog and/or digital component 506 can be any component of the MMW transceiver 100 (e.g., an amplifier, a frequency mixer, a frequency divider, a digital-to-analog converter, etc.). The controller 504 can adjust the behavior of the analog and/or digital component 506 via signal 522 based on instructions received from an external controller via the ABSCI interface device 205.

[0068] In an embodiment, the sensor 510 monitors a characteristic or performance of at least a portion of the analog and/or digital component 506. For example, the sensor 510 can measure the power level of a signal generated by the analog and/or digital component 506. As another example, the sensor 510 can monitor the current level in a portion of the analog and/or digital component 506.

[0069] In order to reduce noise injected into the signal path of the MMW transceiver 100 and/or in order to reduce signal loss, a bias-T circuit 508 may serve as an interface between the analog and/or digital component 506 and the sensor 510. The bias-T circuit 508 may sample a signal 524, which represents the signal or portion of the analog and/or digital component 506 that the sensor 510 is monitoring, and provides a representation of signal 524 (as signal 526) to the sensor 510. The bias-T circuit 508 is described in greater detail below with respect to Figure 6. The bias-T circuit 508 is optional and may be omitted in some embodiments.

[0070] Once the sensor processes the signal 526 to extract the relevant data, such data can be transmitted to the controller 504 as signal 528. The controller 504 then provides the data embedded in signal 528 to the external controller via the ABSCI interface device 205. Based on the data received from the controller 504, the external controller may instruct the controller 504 to adjust the behavior of the analog and/or digital component 506 to meet desired performance levels.

Bias-T Circuit

[0071] Figure 6 illustrates an example bias-T circuit, which is a more detailed embodiment of the bias-T circuit 508 of Figure 5. As illustrated in Figure 6, the bias-T circuit 508 includes transistors 602, 604, 606, and 608, a resistor 612, and a capacitor 614. In an embodiment, the transistors 602, 604, 606, and 608 form an active portion of the bias-T circuit 508, and resistor 612 and capacitor 614 form a passive portion of the bias-T circuit 508.

[0072] In an embodiment, an input signal is coupled to the gate of the transistor 602. For example, the signal in the analog and/or digital component 506, e.g., the signal 524, is coupled to the gate of the transistor 602. Thus, the bias-T circuit 508 may appear to have a high impedance when looking into the bias-T circuit 508 from the signal path of the analog and/or digital component 506. Furthermore, transistors 606 and 608 are flipped so that the source of each transistor 606 and 608 is coupled to supply 610. This flipped coupling of the transistors 606 and 608 can result in the bias-T circuit 508 exhibiting signal separation. The signal 524 can be decoupled or (in certain embodiments) isolated from supply 610, which decoupling can reduce noise injected into the signal 524 and the signal path of the analog and/or digital component 506. In some embodiments, the decoupling or isolation of the signal 524 from the supply 610 also reduces or eliminates the likelihood of signal loss. While aspects of the disclosure refer herein to the “drain” or “source” of a transistor, “drain” and “source” may be interchangeable depending on the type of transistor used to implement the features described herein.

[0073] The resistor 612 is coupled to the capacitor 614 to form a low pass filter. The output of the low pass filter, signal 526, is also the output of the bias-T circuit 508. In an embodiment, the signal 526 is a low frequency representation of the signal 524 (e.g., between 20MHz-100MHz). For example, the low pass filter of the bias-T circuit 508 can preserve the relative magnitude and phase of the signal 524 in generating the signal 526. One or more components of the MMW transceiver 100 may monitor the relative magnitude and/or phase of a signal in the signal path to determine whether the MMW transceiver 100 is operating as desired. If the MMW transceiver 100 is not operating as desired, one or more components of the MMW transceiver 100 can use the relative magnitude and/or phase to make the appropriate adjustments. For instance, the sensor 510 can monitor the relative

magnitude and/or phase of the signal 524 to determine whether the analog and/or digital component 506 is operating as desired and/or whether the operation of the analog and/or digital component 506 should be adjusted. Although a first-order low-pass filter is shown, higher order filters may be implemented in other embodiments, including filters with additional resistors and capacitors.

[0074] In some embodiments, the bias-T circuit 508 can serve as an interface between any of the components or subsystems of the MMW transceiver 100 and devices that monitor such components or subsystems. The bias-T circuit 602 can provide information about the operation of such components or subsystems to the monitoring devices. For example, such information can include the magnitude, gain, noise, phase, and/or variation of signals generated by or passing through the components or subsystems. Based on the information provided by the bias-T circuit 602, such monitoring devices then can adjust operation of the components or subsystems to improve the performance of the MMW transceiver 100.

[0075] In some embodiments, because the bias-T circuit 508 includes just four transistors rather than the fifteen to twenty transistors typically seen in biasing circuits, the bias-T circuit 508 can handle a larger range of frequencies, has a more compact design, and consumes less power than traditional biasing circuits.

Example Chip Representation of ABSCI Sub-Blocks

[0076] Figure 7 illustrates an example chip diagram of a sub-block, such as the sub-block 210 of Figure 2. As illustrated in Figure 7, the sub-block 210 includes several input and output ports. For example, the sub-block 210 includes input ports aClk 702, aDataIn 704, aResetn 706, aCSn 708, aAddr<a:0> 710, and aReadData<r:0> 712, and the sub-block 210 includes output ports aDataOut 714, aReadEnable 716, aResetnOut 718, and aWriteData<w:0> 720.

[0077] In an embodiment, the ABSCI data bus 220 of Figure 2 includes one or more wires (e.g., 5 wires, including aspects of a 4-wire SPI system with an additional contention avoidance signal referred to herein as ABSCI Read Enable Output or “aReadEnable”). A first signal on a first wire is ABSCI Data In (referred to herein as “aDataIn”) and is sent to input port aDataIn 704. aDataIn can include data serially pushed into a slave device (e.g., a sub-block). A second signal on a second

wire is ABSCI Data Out (referred to herein as "aDataOut") and is received from output port aDataOut 714. aDataOut can include data serially read out of the slave device. A third signal on a third wire is ABSCI clock pin (referred to herein as "aClk") and is sent to input port aClk 702. aClk can be a clock signal sent from a master device to a slave device. Internal registers of the sub-block 210 can be triggered on the rising or falling edge of the clock signal. A fourth signal on a fourth wire is ABSCI Common Slave Select (referred to herein as "aCSn") and is sent to input port aCSn 708. aCSn may behave as a global slave select signal common to some or all slave devices. The master device may pull aCSn low during data transmission. A fifth signal on a fifth wire is aReadEnable and can be received from output port aReadEnable 716. aReadEnable can be used for read path arbitration, as described below with respect to Figures 9 and 10. aReadEnable can stay high for the duration for which data is serially shifted out of the slave device.

[0078] In an embodiment, setting the ABSCI data bus 220 width to 5 wires enables easier full-chip routing, although fewer or more wires than 5 may be used in other embodiments. The ABSCI control and monitoring system can be easily scalable, and adding newer slave devices may include a two-step process of (i) assigning a unique slave address to the new slave device and (ii) connecting the new slave device to the ABSCI data bus 220 using a junction block, for example, as described below with respect to Figures 9 and 10.

[0079] In some embodiments, input port aResetn 706 receives an active low asynchronous reset input provided to slave devices that may originate from an external reset pin (e.g., external to the MMW transceiver 100, external to the SoC, external to the device that houses the MMW transceiver 100, etc.). Output port aResetnOut 718 can send an active low synchronous pulse that can be used as a reset signal in the sub-block 210. The pulse can be generated via software or hardware (e.g., a hardware processor in the sub-block 210). Input port aAddr<a:0> 710 can receive an address of width "a+1" that corresponds to a particular slave device. The sub-block 210 can match the received address with the address of the sub-block to determine whether to perform any operations. Input port aReadData<r:0> can receive data inputs of width "r+1." The sub-block 210 can serially shift the data out of the sub-block 210 on a read operation. Output port aWriteData<w:0> can send data of width "w+1." The data may be loaded on the execution of a write operation. Based on the mode selection, the sub-block 210 can

updates a subsection of the parallel outputs (e.g., the data written out of the sub-block 210).

[0080] In an embodiment, the data width is programmable per sub-block 210. Therefore, data writes may occur in separate transactions (e.g., 32 bit registers can be written one at a time) or the entire data transfer can be done in one operation.

[0081] A broadcast mode in the ABSCI protocol can ensure or attempt to ensure timing goals of critical SoC commands. The ABSCI control and monitoring system can provide the flexibility to either assign a special address for the purpose of broadcast or to reserve a special mode. When the broadcast or special mode is exercised, in one embodiment, some or all sub-blocks 210a-N are selected and data is loaded into the sub-blocks 210a-N simultaneously or nearly simultaneously. Depending on the user goals or requirements, the serially-transmitted data could be loaded into a separate set of registers, accessible during the broadcast mode. For large SoC designs, global-level changes may be exercised with this broadcast mode (e.g., all at once to meet timing goals). Thus, the ABSCI control and monitoring system, and specifically the external controller and the ABSCI interface device 205, can use addressing to communicate with and change the behavior of one sub-block 210a-N, a plurality of sub-blocks 210a-N simultaneously or nearly simultaneously, or all of the sub-blocks 210a-N simultaneously or nearly simultaneously.

ABSCI Word Format

[0082] Figure 8 illustrates an example packet 800 generated by an ABSCI interface device, such as the ABSCI interface device 205 of Figure 2. As illustrated in Figure 8, the packet 800 includes two portions: sub-block word header 810 and sub-block data 820. While the packet 800 includes the sub-block word header 810 and the sub-block data 820, this is not meant to be limiting. The ABSCI communication word format can be defined in many different ways and/or may be selected automatically from a set of word format options. The flexibility to define the ABSCI communication word format in many different ways can be built into the ABSCI protocol.

[0083] In an embodiment, the sub-block word header 810 includes at least one of a Read/Write_bar (referred to herein as “R/W_n”), a slave address, a mode

register, and a data register. The R/W_n can be a bit indicating a read operation when the bit is high (e.g., logic "1") and a write operation when the bit is low (e.g., logic "0"). The slave address can be a bit representing the slave address space. The slave address can be matched with the hardwired slave address (e.g., a preset address of a sub-block) prior to performing any operation. The mode register can include one or more bits used to indicate or select from different modes. For example, modes could include software reset, exit reset, common mode, broadcast mode, acknowledge, and so on. The data register includes one or more bits used to select from different data registers to be written into and/or read from. For example, the parallel outputs and read inputs can be segregated into sets of 32 bits each.

[0084] In some embodiments, the sub-block data 820 is payload data of variable length. The sub-block data 820 width could be programmed such that one or more sub-blocks 210a-N each receive a payload of a different width. In an embodiment, most sub-blocks 210a-N have sub-block data 820 widths in multiples of 32 bits. However, in special cases, such as when an off-chip microprocessor is interfaced with an on-chip memory, the sub-block data 820 width could be in kilobytes. The sub-block data 820 width can enable the transfer of multiple data pages into memory in a single transfer.

ABSCI Read Path

[0085] Figure 9 illustrates an example ABSCI read path 900 for one or more of the sub-blocks 210a-N of Figure 2. The ABSCI read path 900 may be common to some or all of the sub-blocks 210a-N. In an embodiment, a bus junction 920 is coupled to one or more sub-blocks 210a-N. For example, sub-block 210a and sub-block 210b can be coupled to the bus junction 920 as illustrated in Figure 9.

[0086] In an embodiment, sub-block 210a transmits aReadEnable 914a and aDataOut 916a to the bus junction 920. Likewise, sub-block 210b transmits aReadEnable 914b and aDataOut 916b to the bus junction 920. The bus junction 920 can function as an arbitration circuit, which is described in greater detail below with respect to Figure 10, and can provide aReadEnable 914c and aDataOut 916c to an external controller or master device via an ABSCI interface device.

[0087] For example, an external controller or master device can request data from one sub-block 210a or 210b at any given time, and the request may be

made through a write operation to that particular sub-block 210a or 210b. The requested sub-block 210a or 210b can transmit data to the bus junction 920, which then can forward the data to the external controller or master device. The requested sub-block 210a or 210b can keep aReadEnable high such that the bus junction 920 forwards the correct data to the external controller or master device.

[0088] Figure 10 illustrates a schematic diagram of a bus junction, such as the bus junction 920 of Figure 9. As illustrated in Figure 12, the bus junction 920 can include logic gates 1002, 1004, 1006, 1008, 1010, 1012, and 1014. For example, logic gates 1002 and 1004 could be inverters (e.g., NOT gates), logic gates 1006 and 1008 could be AND gates, logic gate 1010 could be an XOR gate, and logic gates 1012 and 1014 could be buffers.

[0089] In an embodiment, aReadEnable 914a, from the sub-block 210a, is received by the inverter 1004 and the AND gate 1006. aReadEnable 914b, from the sub-block 210b, can be received by the inverter 1002 and the AND gate 1008. In some embodiments, the inverter 1004 negates aReadEnable 914a and provides the negated version of aReadEnable 914a to AND gate 1008. The inverter 1002 can negate aReadEnable 914b and provide the negated version of aReadEnable 914b to AND gate 1006. Thus, AND gate 1006 can generate a low output (e.g., logic “0”) when aReadEnable 914b is high (e.g., sub-block 210b is trying to transmit data) or when aReadEnable 914a is low (e.g., sub-block 210a is not trying to transmit data). AND gate 1006 can generate a high output (e.g., logic “1”) when aReadEnable 914b is low and aReadEnable 914a is high. Likewise, AND gate 1008 can generate a low output when aReadEnable 914a is high (e.g., sub-block 210a is trying to transmit data) or when aReadEnable 914b is low (e.g., sub-block 210b is not trying to transmit data). AND gate 1008 can generate a high output when aReadEnable 914a is low and aReadEnable 914b is high.

[0090] The output of AND gate 1006 can be passed to the buffer 1012 as an enable/disable control and to the XOR 1010. The output of AND gate 1008 can be passed to the buffer 1014 as an enable/disable control and to the XOR 1010. The buffer 1012 can receive aDataOut 916a from the sub-block 210a, and the buffer 1014 can receive aDataOut 916b from the sub-block 210b. Thus, when AND gate 1006 is high (e.g., when sub-block 210a is trying to transmit data and sub-block 210b is not trying to transmit data), buffer 1012 can be enabled and aDataOut 916a can

pass to the ABSCI interface device as aDataOut 916c. Likewise, when AND gate 1008 is high (e.g., when sub-block 210b is trying to transmit data and sub-block 210a is not trying to transmit data), buffer 1014 can be enabled and aDataOut 916b can pass to the ABSCI interface device as aDataOut 916c. In an embodiment, as long as AND gate 1006 or AND gate 1008 is high, then aReadEnable 914c is set high. On the other hand, if AND gate 1006 and AND gate 1008 are both low or are both high, then aReadEnable 914c can be set low.

[0091] The ABSCI read path 900 architecture described herein can support different read and write data widths for each sub-block. Depending on the criticality of block operation in certain embodiments, some or all of the write path outputs may be looped back onto the read path, hence helping with debug and calibration operations.

[0092] Example digital circuits shown in Figures 9 and 10 include components such as AND gates, NOT gates, and the like. These components may be replaced with logically equivalent components in other embodiments while retaining the same or similar functionality, such as various AND gates, OR gates, NOT gates, NAND gates, NOR gates, XOR gates, XNOR gates, flip-flops, latches, combinations of the same, or the like.

Example PLL Start-Up Procedures

[0093] Figures 11-13 illustrate example automated start-up procedures for a PLL. In an embodiment, a PLL can be digitally controlled to have different startup modes. For example, the SPI or I2C protocol can be used in an automatic procedure to control the startup of different blocks of the PLL. As an example, the SPI or I2C protocol can be used to control the startup of different blocks of the PLL via the refreshing of SPI or I2C bits.

[0094] Figure 11 illustrates an example automated start-up procedure 1100 to reduce the likelihood of dual oscillations in an IF PLL, such as PLL 102 of Figure 1. The automated start-up procedure 1100 can be turned on or off using the SPI or I2C protocol. The various states 1101-1108 depict the state of operation of the IF PLL during various times t. In an embodiment, Tref defines a reference time period. As an example, the reference time period Tref can be approximately 37ns (e.g., between 34ns-40ns). When PLL is ON, such as in state 1106, this may signify

that divider blocks, a phase frequency detector (PFD), and/or a charge pump (CP) are in an ON state. In some embodiments, a master reset control is available (e.g., via software or a physical switch or button) that resets time t (e.g., resets a counter to set time at 0).

[0095] Figure 12 illustrates an example automated start-up procedure 1200 to incorporate delay in reference signals in an IF PLL. The automated start-up procedure 1200 can be turned on or off using the SPI or I2C protocol. The various states 1201-1203 depict the state of operation of the IF PLL during various times t. As described above with respect to Figure 11, Tref may define a reference time period. As an example, the reference time period Tref can be approximately 37ns (e.g., between 34ns-40ns). In some embodiments, a master reset control is available (e.g., via software or a physical switch or button) that resets time t (e.g., resets a counter to set time at 0).

[0096] Figure 13 illustrates an example automated start-up procedure 1300 for a fast locking mode in an IF PLL. The automated start-up procedure 1300 can be turned on or off using the SPI or I2C protocol. The various states 1301-1304 depict the state of operation of the IF PLL during various times t. As described above with respect to Figures 11 and 12, Tref may define a reference time period. As an example, the reference time period Tref can be approximately 37ns (e.g., between 34ns-40ns). In an embodiment, a programmable counter can be used to control the value of n illustrated with respect to state 1304. WBW mode illustrated in states 1303 and 1304 may refer to a mode in which there is a wide loop bandwidth. NBW mode illustrated in state 1304 may refer to a mode in which there is a narrow loop bandwidth. In some embodiments, a master reset control is available (e.g., via software or a physical switch or button) that resets time t (e.g., resets a counter to set time at 0).

[0097] Figure 14 illustrates a block diagram of an example switch controller 1400. In an embodiment, on/off signals of switches used in conjunction with the voltage supply and biasing circuits, such as the bias-T circuit 508, can be controlled by the switch controller 1400. For example, the switch controller 1400 can control the voltage supply and/or biasing circuits of an IF PLL. The switch controller 1400 can include digital logic, such as logic components 1402, a counter 1404, and a mux 1406.

[0098] The logic components 1402 can receive on/off controls 1430 formatted according to the SPI or I2C protocol. For example, the on/off controls 1430 can be received from a master device and determine whether a switch used in conjunction with the voltage supply or a biasing circuit should be turned on or off. The logic components 1402 can use the on/off controls 1430 and/or an initialization bit 1422 to generate an output 1432.

[0099] In some embodiments, during an automated start-up procedure, such as automated start-up procedures 1100, 1200, and/or 1300, the initialization bit 1422 is transferred from the counter 1404 to the logic components 1402. As an example, the initialization bit 1422 can bypass and/or modify some of the bits associated with the SPI or I2C protocol after initialization. In an embodiment, the switch controller 1400, such as the logic components 1402, can include an assigned bit that, when enabled, keeps a PLL on so that timing constraints can be met.

[0100] The counter 1402 can receive mode controls 1426 formatted according to the SPI or I2C protocol. The mode controls 1426 can be received from a master device. The counter 1404 can use the mode controls 1426, a reference frequency 1420 (e.g., 27 MHz), and/or data provided by the logic components 1402 to generate an output 1434. In an embodiment, the mux 1406 selects between the output 1432 and the output 1434 and provides controls 1436 to one or more switches.

[0101] In some embodiments, not shown, the controls 1436 generated by the switch controller 1400 can be overridden. For example, the switches can receive one or more override bits that override the controls 1436.

Flowchart

[0102] Figure 15 illustrates a flowchart of a method 1500 for adjusting a characteristic of a wireless data transceiver. In an embodiment, the method 1500 can be performed by any of the sub-blocks 210a-N discussed above with respect to Figure 2. Depending on the embodiment, the method 1500 may include fewer and/or additional blocks and the blocks may be performed in an order different than illustrated.

[0103] In block 1502, first data formatted according to a first protocol is transmitted by a first slave device to a master controller. In an embodiment, the first

data is transmitted to the master controller via an interface device that converts the first data from the first protocol format to a second protocol format.

[0104] In block 1504, a first instruction is received by the first slave device from the master controller via a first data bus. In an embodiment, the master controller transmits the first instruction to the interface device and the interface device forwards the first instruction via the first data bus.

[0105] In block 1506, a characteristic of the first slave device is adjusted by the first slave device based on the first instruction. In an embodiment, the first instruction is generated based on the first data. In a further embodiment, the packet has a destination address of a first slave address corresponding to the first slave device.

[0106] In block 1508, a second instruction is generated based on the first instruction by the first slave device. In block 1510, the second instruction is transmitted by the first slave device to a second slave device that adjusts a characteristic of the second slave device based on the second instruction.

Example Use Case

[0107] Figure 16 illustrates an example docking system 1600. As illustrated in Figure 16, the docking system 1600 can include an electronic device 1610 (e.g., a mobile phone, a tablet, a laptop, etc.) and a docking station 1620 (e.g., a television, a desktop computer, a tablet, a device that connects to another peripheral device like a television or a desktop computer, etc.). In an embodiment, the electronic device 1610 and the docking station 1620 each include a MMW transceiver, such as the MMW transceiver 100 described above. The MMW transceiver included in the electronic device 1610 and the docking station 1620 may include the features described herein. The electronic device 1610 and the docking station 1620 can communicate via wireless data transmissions using the MMW transceiver. For example, the electronic device 1610 can transmit data (e.g., RAW image files, video files, control signals, etc.) to the docking station 1620 using the MMW transceiver. Likewise, the docking station 1620 can transmit data (e.g., RAW image files, video files, control signals, etc.) to the electronic device 1610 using the MMW transceiver.

[0108] In some embodiments, the MMW transceiver is internal to the electronic device 1610 and/or the docking station 1620. For example, the MMW transceiver could be included with other radios (e.g., GSM, CDMA, Bluetooth, etc.) in the electronic device 1610 or docking station 1620. In other embodiments, not shown, the MMW transceiver can be connected to the electronic device 1610 and/or the docking station 1620 via an external connection. For example, the MMW transceiver could be included in a device that connects to the electronic device 1610 and/or the docking station 1620 via a wired connection (e.g., via USB, Ethernet, IEEE 1394, etc.). Data can then be routed between the electronic device 1610 or the docking station 1620 and the MMW transceiver via the wired connection.

Terminology

[0109] Although certain types of circuit components are shown and described herein, equivalent or similar circuit components may be used in their place in other embodiments. For instance, example field effect transistors (FETs) shown may be replaced with bipolar junction transistors (BJTs) in some embodiments. Further, NMOS FETs may be replaced with PMOS FETs and vice versa, or NPN BJTs may be replaced with PNP BJTs, and vice versa. Further, many types of FETs can be used interchangeably in the embodiments described herein with slight or no design differences, some examples of which include a CNFET, a DEPFET, a DNAFET, a FREDFET, a HEMT, an IGBT, an ISFET, a JFET, a MESFET, a MOSFET, a MODFET, a NOMFET, an OFET, and the like. Other circuit components shown, including passive components, may likewise be replaced with other electrical equivalents or similar circuits. Furthermore, the values of passive circuit elements, voltages, currents, and power (among other circuit parameters) may be chosen to satisfy any design criterion relevant to the electronic device in which the circuits are implemented.

[0110] Although the inventions disclosed herein have been described in the context of certain embodiments and examples, it should be understood that the inventions disclosed herein extend beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the inventions and certain modifications and equivalents thereof. Further, the disclosure herein of any particular feature, aspect, method, property, characteristic, quality, attribute, element,

or the like in connection with an embodiment may be used in all other embodiments set forth herein. Thus, it is intended that the scope of the inventions disclosed herein should not be limited by the particular disclosed embodiments described above. As will be recognized, certain embodiments of the inventions described herein can be embodied within a form that does not provide all of the features and benefits set forth herein, as some features can be used or practiced separately from others.

[0111] Many other variations than those described herein will be apparent from this disclosure. For example, depending on the embodiment, certain acts, events, or functions of any of the methods described herein can be performed in a different sequence, can be added, merged, or left out altogether (e.g., not all described acts or events are necessary for the practice of the methods).

[0112] Conditional language used herein, such as, among others, "can," "might," "may," "e.g.," "for example," "for instance," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment. The terms "comprising," "including," "having," and the like are synonymous and are used inclusively, in an open-ended fashion, and do not exclude additional elements, features, acts, operations, and so forth. Also, the term "or" is used in its inclusive sense (and not in its exclusive sense) so that when used, for example, to connect a list of elements, the term "or" means one, some, or all of the elements in the list. Further, the term "each," as used herein, in addition to having its ordinary meaning, can mean any subset of a set of elements to which the term "each" is applied.

[0113] While the above detailed description has shown, described, and pointed out novel features as applied to various embodiments, it will be understood that various omissions, substitutions, and changes in the form and details of the devices or algorithms illustrated can be made without departing from the spirit of the disclosure. As will be recognized, certain embodiments of the inventions described

herein can be embodied within a form that does not provide all of the features and benefits set forth herein, as some features can be used or practiced separately from others.

WHAT IS CLAIMED IS:

1. A wireless data transceiver, comprising:

a data bus;

a first layer comprising a first slave device, the first slave device coupled to the data bus such that the first slave device detects transmissions on the data bus;

a second layer comprising a second slave device, the second slave device coupled to the data bus;

an interface device coupled to the data bus, the interface device configured to convert first data packets formatted according to a first protocol to a second protocol and to convert second data packets formatted according to the first protocol to the second protocol;

a first master controller coupled to the interface device, the first master controller configured to receive first data packets formatted according to the second protocol and to output third data packets having a first slave address corresponding to the first slave device; and

a second master controller coupled to the interface device, the second master controller configured to receive second data packets formatted according to the second protocol and to output fourth data packets having a second slave address corresponding to the second slave device.

2. The wireless data transceiver of claim 1, wherein the first layer further comprises a third slave device, and wherein the first slave device is configured to output fifth data packets having a third slave address corresponding to the third slave device for reception by the third slave device.

3. The wireless data transceiver of claims 1 or 2, wherein the first slave device is configured to adjust a performance characteristic of the first slave device based on instructions included in the third data packets having the first slave address.

4. The wireless data transceiver of claim 3, wherein the first slave device is configured to transmit the first data formatted according to the first protocol to the interface device, and wherein the instructions included in the data packets having the first slave address are based on the first data.

5. The wireless data transceiver of claim 1, wherein the first slave device comprises:

a slave controller configured to execute instructions included in the third data packets having the first slave address;

an analog device coupled to the slave controller, wherein a characteristic of the analog device is controlled based on the instructions executed by the slave controller;

a sensor coupled to the slave controller, wherein the sensor is configured to monitor the characteristic of the analog device and transmit measurements corresponding to the characteristic to the slave controller; and

a bias circuit coupled between the analog device and the sensor, wherein the bias circuit is configured to reduce an amount of noise injected into the analog device by the sensor.

6. The wireless data transceiver of claim 5, wherein the bias circuit comprises a first transistor, and wherein a gate of the first transistor is coupled to the analog device.

7. The wireless data transceiver of claim 6, wherein the bias circuit further comprises a second transistor and a third transistor, wherein a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and wherein a source of the second transistor and a source of the third transistor are coupled to a supply voltage.

8. The wireless data transceiver of claim 7, wherein the bias circuit further comprises a fourth transistor and a low pass filter, wherein a drain of the third transistor and a drain and a gate of the fourth transistor are coupled to the low pass filter, and wherein an output of the low pass filter is coupled to the sensor.

9. The wireless data transceiver of claim 8, wherein a signal at the output of the low pass filter is a representation of a signal at the gate of the first transistor.

10. The wireless data transceiver of claims 1 or 9, wherein the first chip is an application layer chip, and wherein the second chip is a radio frequency (RF) analog front-end chip.

11. A method for adjusting a characteristic of a wireless data transceiver, the method comprising:

transmitting, by a first slave device, first data formatted according to a first protocol to a master controller;

receiving, by the first slave device from the master controller, a first instruction in a packet from a data bus, wherein the first instruction is

generated based on the first data, and wherein the packet has a destination address of a first slave address corresponding to the first slave device;

adjusting, by the first slave device, a characteristic of the first slave device based on the first instruction;

generating, by the first slave device, a second instruction based on the first instruction; and

transmitting, by the first slave device, the second instruction to a second slave device that adjusts a characteristic of the second slave device based on the second instruction.

12. The method of claim 11, further comprising:

receiving, by the first slave device from the master controller, a second packet from the data bus, wherein the second packet has a destination address of a second slave address corresponding to a third slave device; and

discarding the second packet.

13. The method of claim 11, further comprising:

receiving, by the first slave device from the master controller, a second packet from the data bus, wherein the second packet has a destination address of a broadcast address; and

adjusting the characteristic of the first slave device based on instructions included in the second packet.

14. The method of any of claims 11-13, wherein transmitting first data formatted according to a first protocol to a master controller comprises:

obtaining a measurement of an analog device comprised within the first slave device using a bias circuit and a sensor, wherein the bias circuit is coupled between the analog device and the sensor, and wherein the bias circuit is configured to reduce an amount of noise injected into the analog device by the sensor; and

generating the first data, wherein the first data comprises the measurement.

15. The method of claim 14, wherein the bias circuit comprises a first transistor, and wherein a gate of the first transistor is coupled to the analog device.

16. The method of claim 15, wherein the bias circuit further comprises a second transistor and a third transistor, wherein a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and wherein

a source of the second transistor and a source of the third transistor are coupled to a supply voltage.

17. The method of claim 16, wherein the bias circuit further comprises a fourth transistor and a low pass filter, wherein a drain of the third transistor and a drain and a gate of the fourth transistor are coupled to the low pass filter, and wherein an output of the low pass filter is coupled to the sensor.

18. The method of claim 17, wherein a signal at the output of the low pass filter is a representation of a signal at the gate of the first transistor.

19. The method of claims 11 or 18, wherein the first slave device is comprised within at least one of an application layer chip, a baseband chip, or a radio frequency (RF) analog front-end chip.

20. A wireless data transceiver, comprising:

a data bus;

a first slave device coupled to the data bus, the first slave device configured to read a first data packet comprising a first slave address and to transmit a second data packet;

an interface device coupled to the data bus, wherein the interface device is configured to convert the first data packet formatted according to the second protocol to the first protocol;

a master controller configured to transmit the first data packet to the interface device based on the second data packet received from the first slave device, wherein the first data packet comprises a first instruction, wherein the first data packet comprises a destination address of the first slave address, and wherein the interface device is further configured to transmit the first data packet over the data bus; and

a second slave device configured to receive a third data packet from the first slave device, wherein the third data packet comprises a second instruction, wherein the first slave device is configured to execute the first instruction, and wherein the second instruction is based on the first instruction.

21. The wireless data transceiver of claim 20, wherein the first slave device is configured to adjust a performance characteristic of the first slave device based on the first instruction.

22. The wireless data transceiver of claims 20 or 21, wherein the first slave device comprises:

a slave controller configured to execute the first instruction included in the first data packet having the first slave address;

an analog device coupled to the slave controller, wherein a characteristic of the analog device is controlled based on the first instruction executed by the slave controller;

a sensor coupled to the slave controller, wherein the sensor is configured to monitor the characteristic of the analog device and transmit measurements corresponding to the characteristic to the slave controller; and

a bias circuit coupled between the analog device and the sensor, wherein the bias circuit is configured to reduce an amount of noise injected into the analog device by the sensor.

23. The wireless data transceiver of claim 22, wherein the bias circuit comprises a first transistor, and wherein a gate of the first transistor is coupled to the analog device.

24. The wireless data transceiver of claim 23, wherein the bias circuit comprises a second transistor and a third transistor, wherein a gate of the second transistor is coupled to a gate of the third transistor and a drain of the first transistor, and wherein a source of the second transistor and a source of the third transistor are coupled to a supply voltage.

25. The wireless data transceiver of claim 24, wherein the bias circuit comprises a fourth transistor and a low pass filter, wherein a drain of the third transistor and a drain and a gate of the fourth transistor are coupled to the low pass filter, and wherein an output of the low pass filter is coupled to the sensor.

26. The wireless data transceiver of claim 25, wherein a signal at the output of the low pass filter is a representation of a signal at the gate of the first transistor.

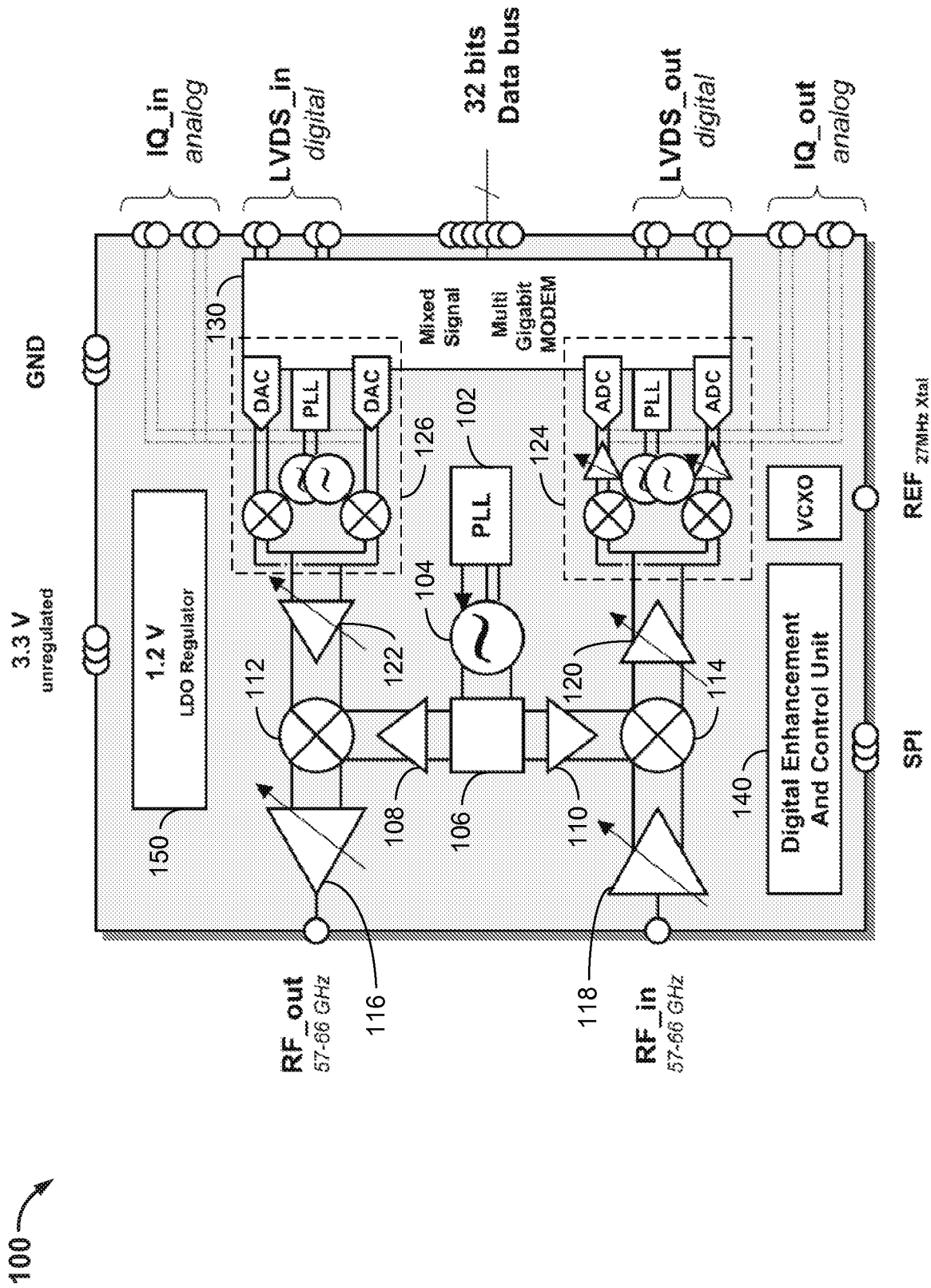
100
IQ_in
analog
LVDS_in
digital
32 bits
Data bus
LVDS_out
digital
IQ_out
analog
GND
3.3 V
unregulated
1.2 V
LDO Regulator
150
130
Mixed
Signal
Multi
Gigabit
MODEM
DAC
PLL
DAC
126
102
PLL
104
124
ADC
PLL
ADC
VCXO
REF 27MHz Xtal
112
122
120
114
108
106
110
140
Digital Enhancement
And Control Unit
SPI
RF_out
57-66 GHz
116
118
RF_in
57-66 GHz

FIG. 1

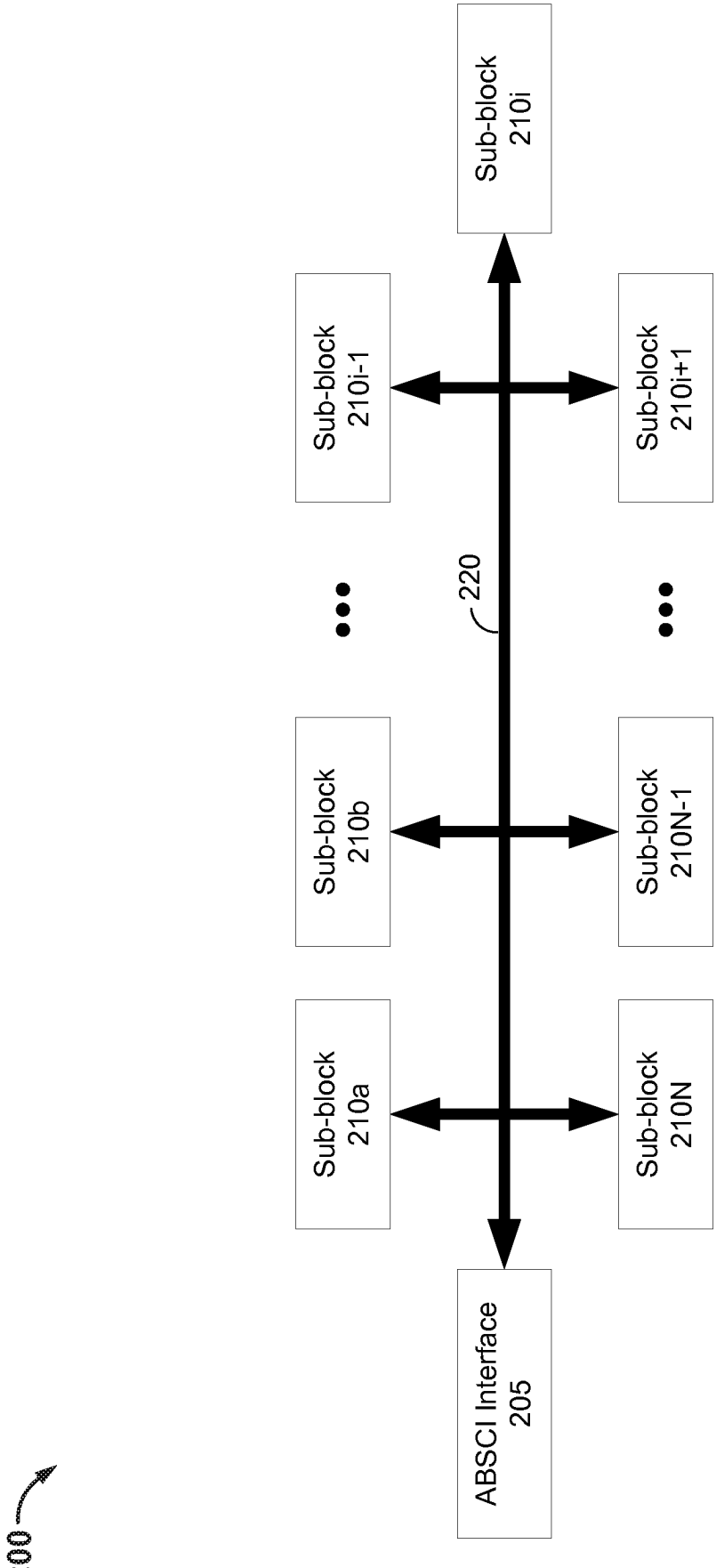
200
ABSCI Interface 205
Sub-block 210a
Sub-block 210b
Sub-block 210i-1
Sub-block 210i
Sub-block 210N
Sub-block 210N-1
Sub-block 210i+1
220

FIG. 2

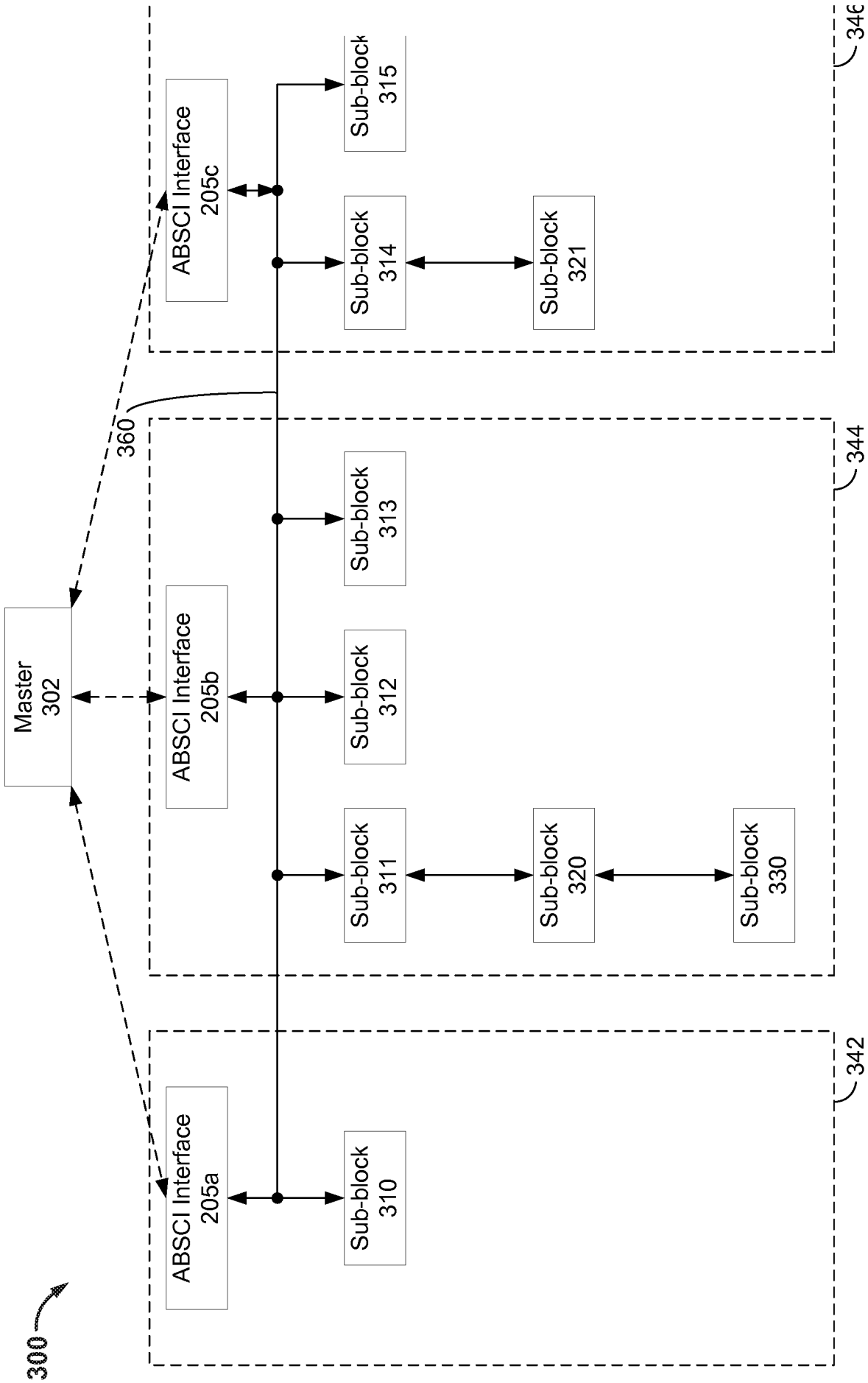
300
Master 302
ABSCI Interface 205a
ABSCI Interface 205b
ABSCI Interface 205c
Sub-block 310
Sub-block 311
Sub-block 312
Sub-block 313
Sub-block 314
Sub-block 315
Sub-block 320
Sub-block 321
Sub-block 330
342
344
346
360

FIG. 3

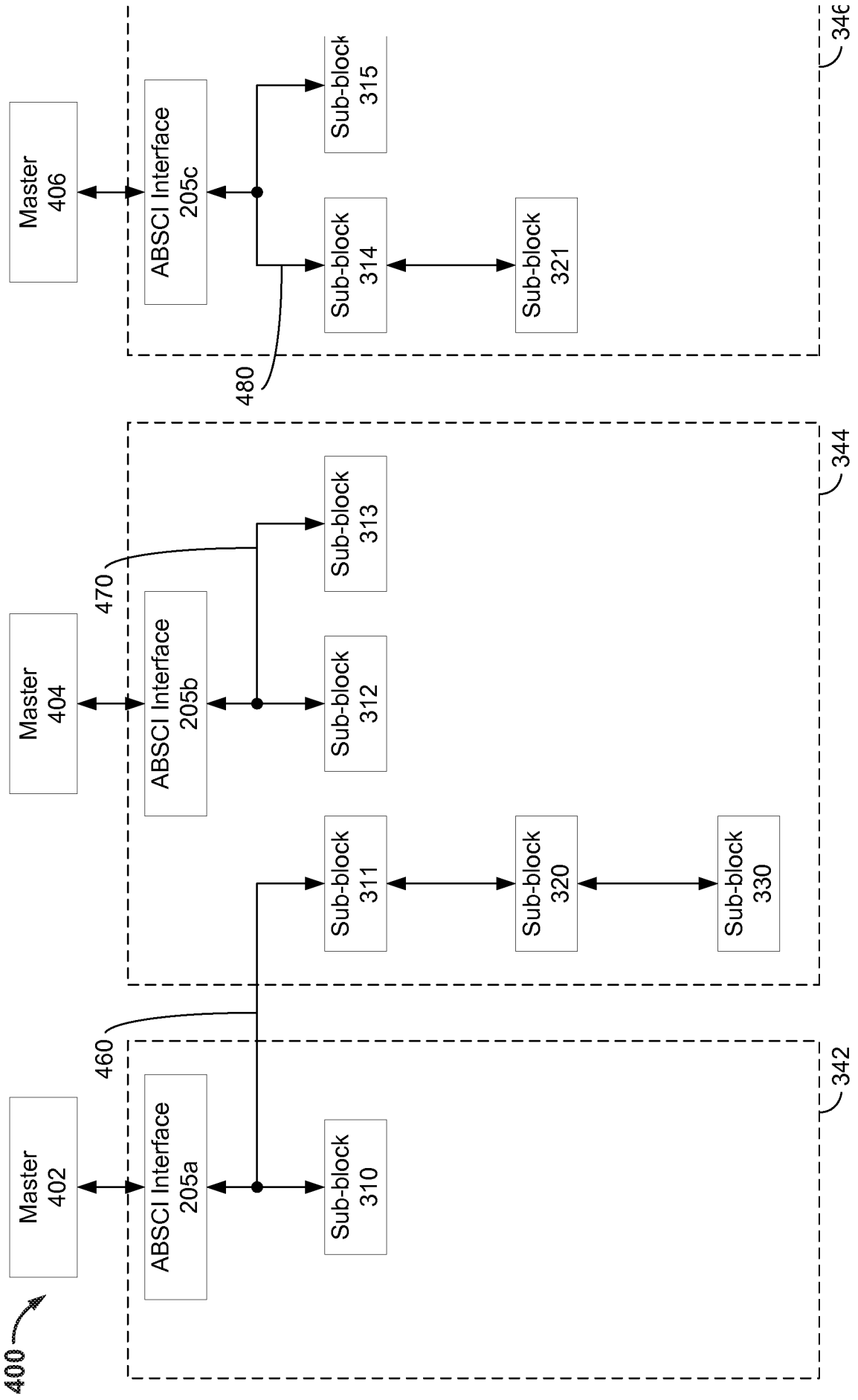
400
Master 402
ABSCI Interface 205a
Sub-block 310
342
460
Master 404
ABSCI Interface 205b
Sub-block 311
Sub-block 320
Sub-block 330
Sub-block 312
Sub-block 313
344
470
Master 406
ABSCI Interface 205c
Sub-block 314
Sub-block 321
Sub-block 315
346
480

FIG. 4

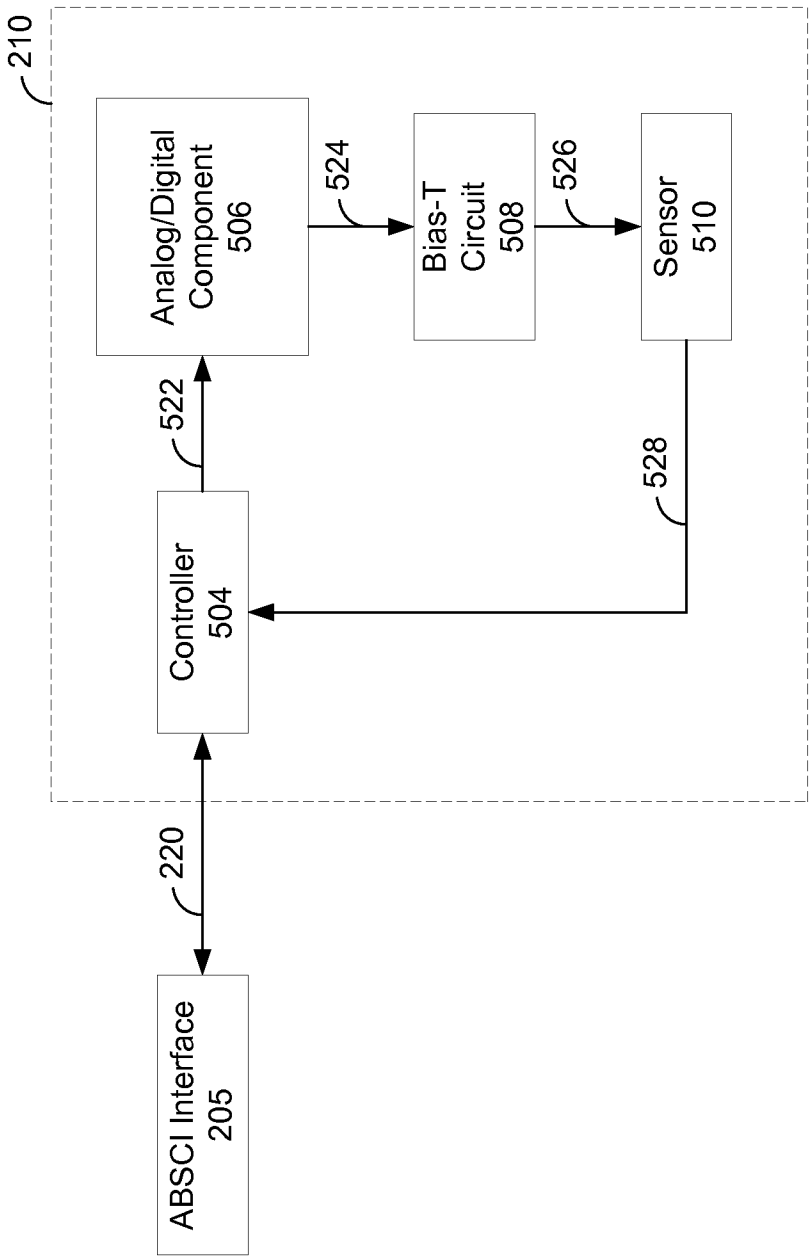
210
Analog/Digital Component 506
524
Bias-T Circuit 508
526
Sensor 510
522
528
Controller 504
220
ABSCI Interface 205

FIG. 5

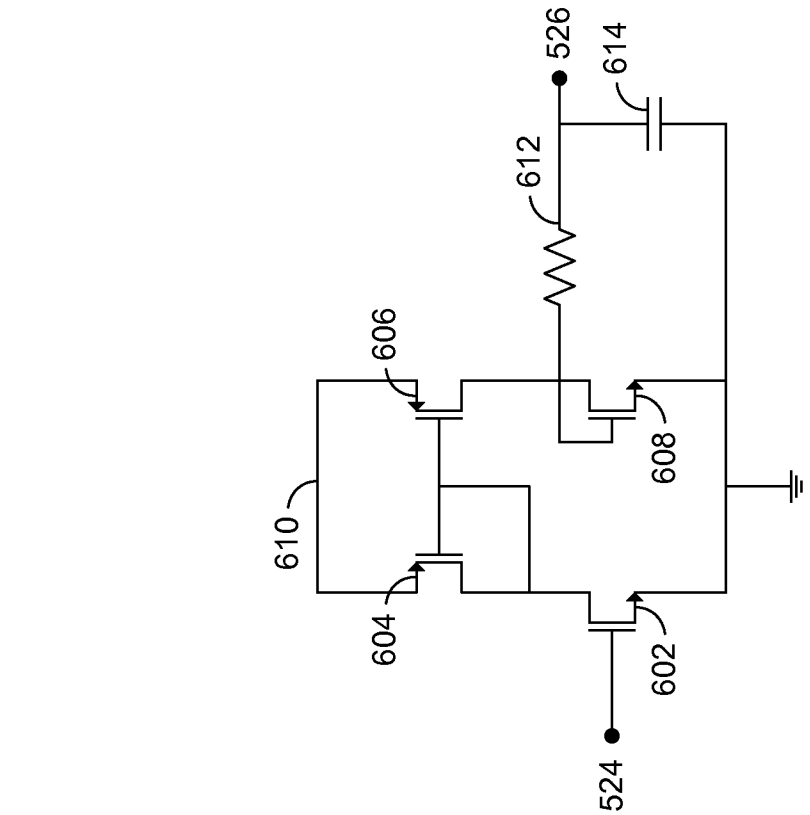

FIG. 6

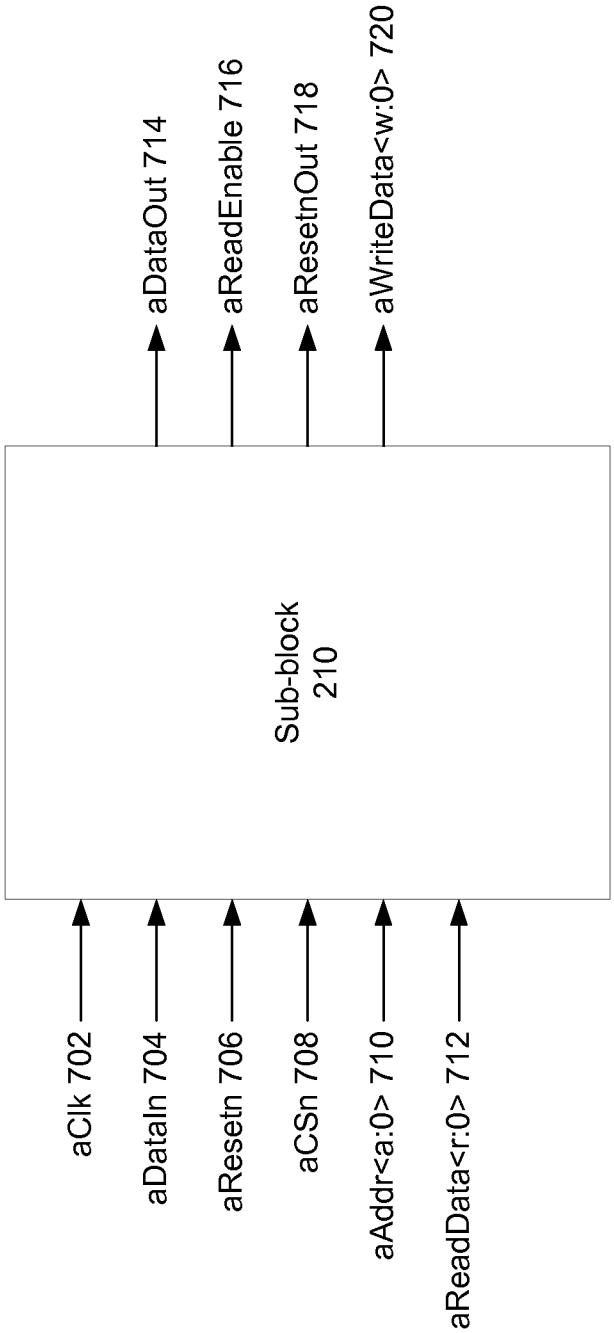
aClk 702
aDataIn 704
aResetn 706
aCSn 708
aAddr<a:0> 710
aReadData<r:0> 712
Sub-block 210
aDataOut 714
aReadEnable 716
aResetnOut 718
aWriteData<w:0> 720

FIG. 7

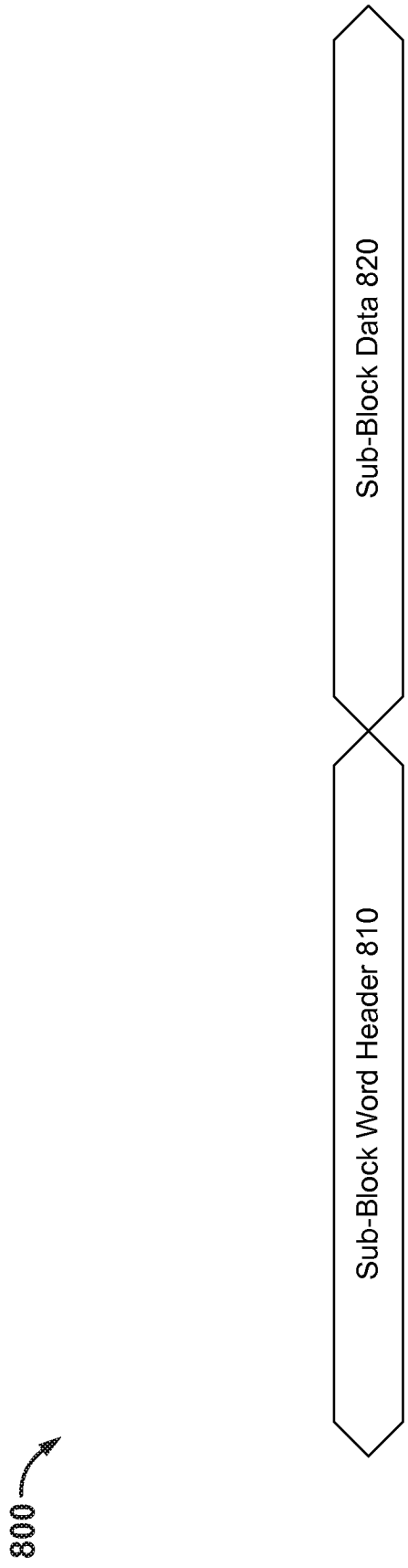

FIG. 8

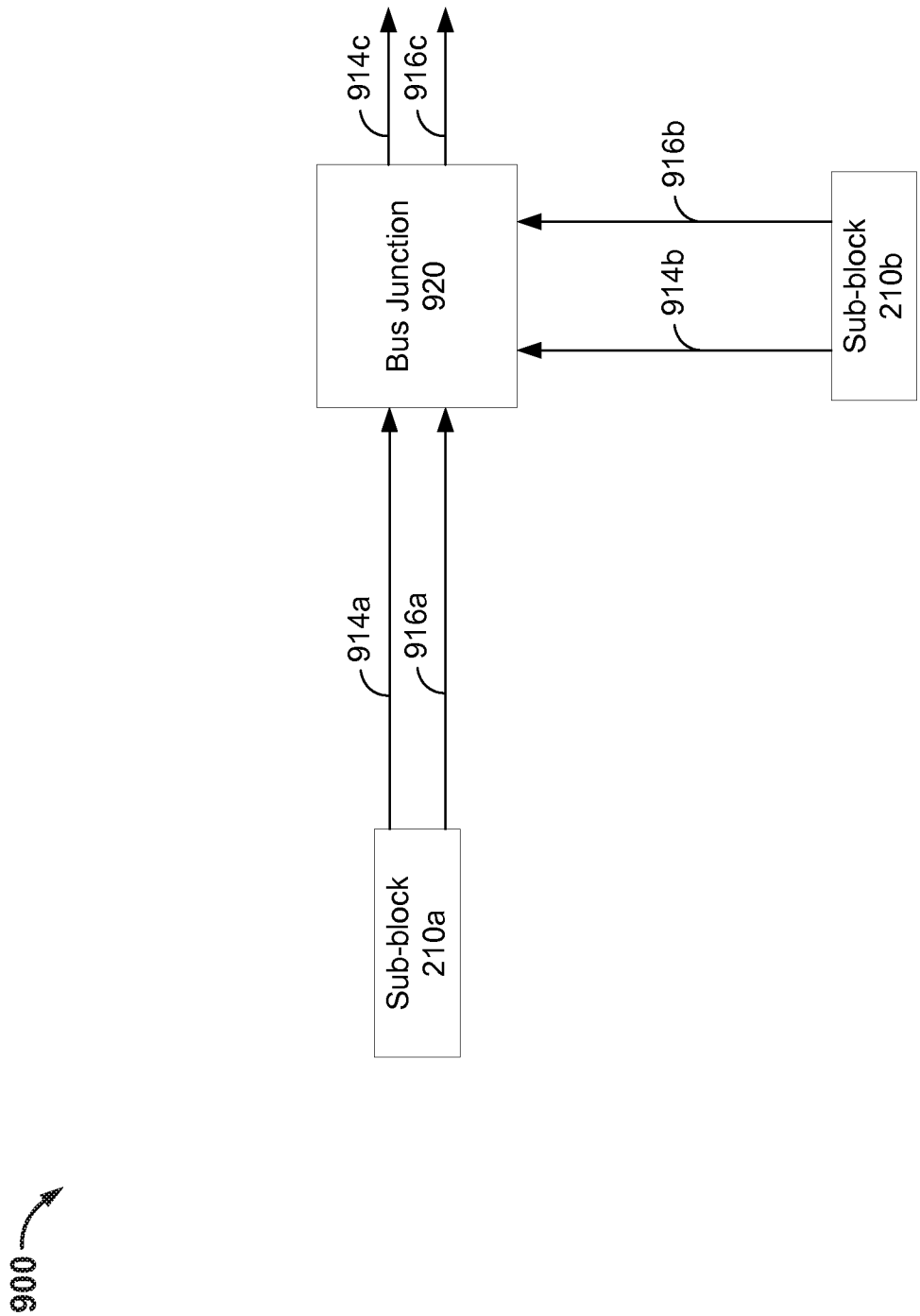
900
Sub-block 210a
914a
916a
Bus Junction 920
914c
916c
916b
914b
Sub-block 210b

FIG. 9

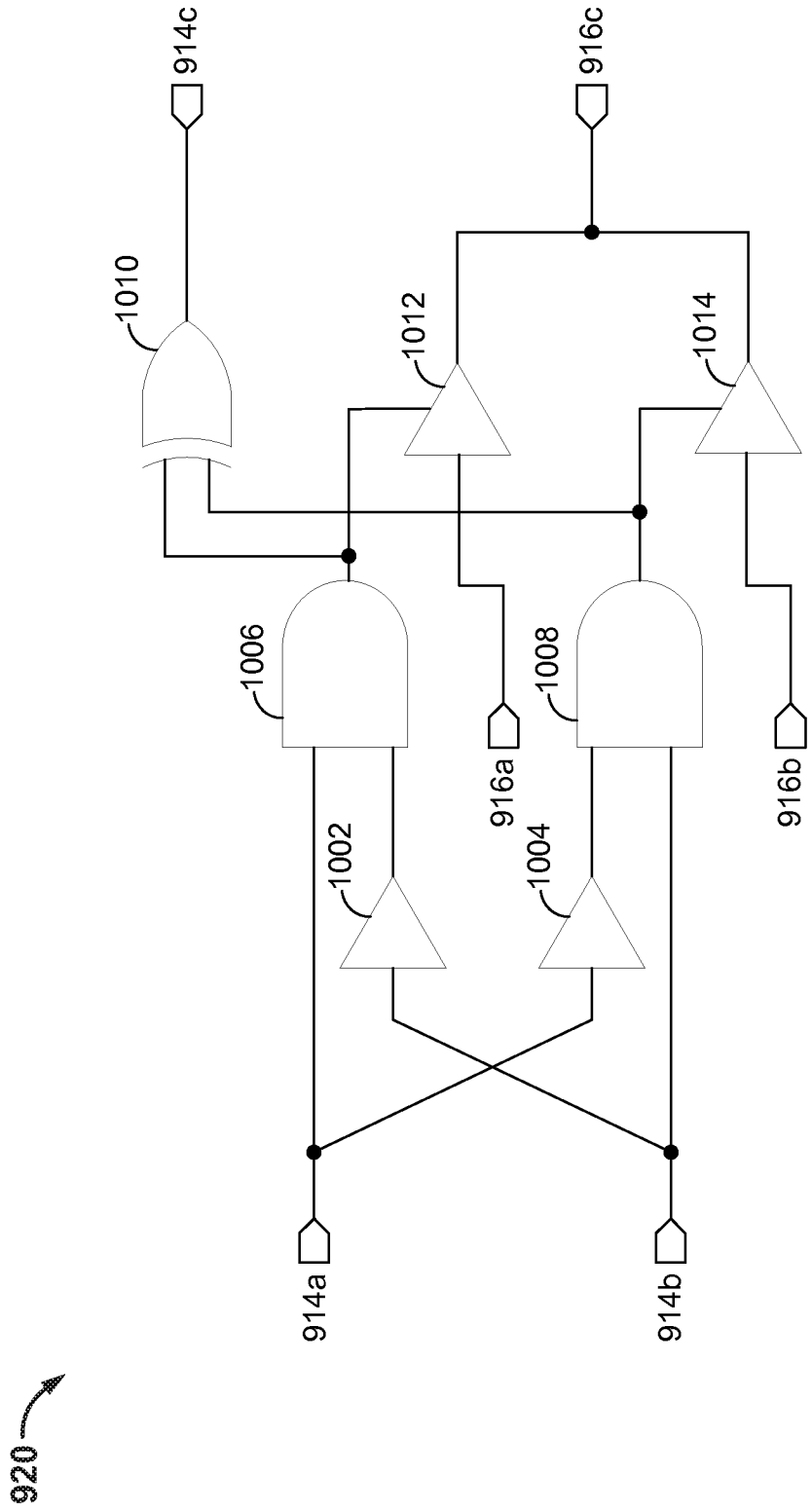
914c
916c
1010
1012
1014
1006
1008
916a
916b
1002
1004
914a
914b
920

FIG. 10


1100
t = 0
State 1101
Circuits OFF
REF OFF
INIT_DONE = 0
t = 6*Tref
State 1102
Bias Circuits ON
VCO & PLL OFF
REF OFF
t = 12*Tref
State 1103
Buffer_Vtune = 1
Buffer_PLL = 1
VCO & PLL OFF
REF OFF
t = 18*Tref
State 1104
Buffer_Vtune = 1
Buffer_PLL = 1
VCO ON
PLL & REF OFF
t = 30*Tref
State 1105
Buffer_Vtune = 0
Buffer_PLL = 1
VCO ON
PLL & REF OFF
t = 36*Tref
State 1106
Buffer_Vtune = 0
Buffer_PLL = 1
VCO & PLL ON
REF OFF
t = 42*Tref
State 1107
REF ON
INIT_DONE = 0
t = 191*Tref
State 1108
REF ON
INIT_DONE = 1

FIG. 11

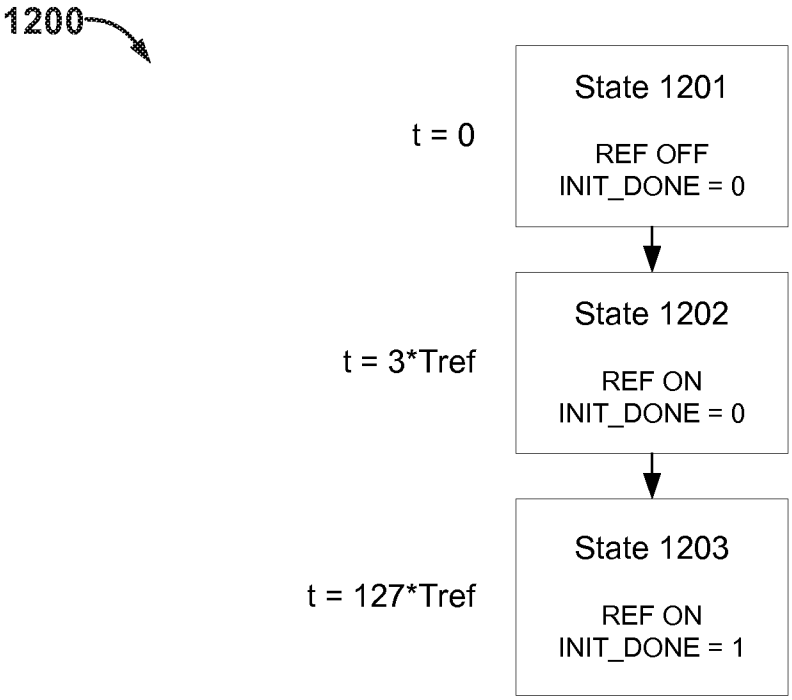
1200
t = 0
State 1201
REF OFF
INIT_DONE = 0
t = 3*Tref
State 1202
REF ON
INIT_DONE = 0
t = 127*Tref
State 1203
REF ON
INIT_DONE = 1

FIG. 12

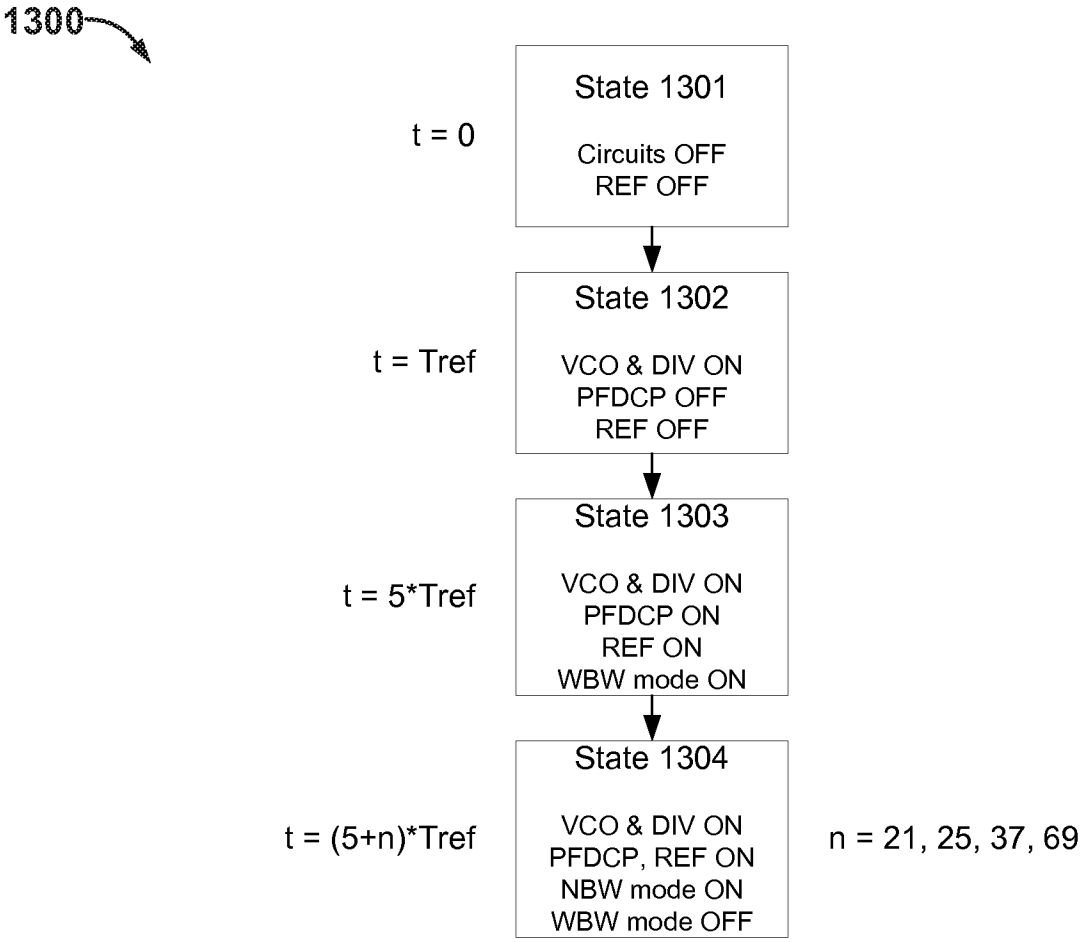
1300
t = 0
State 1301
Circuits OFF
REF OFF
t = Tref
State 1302
VCO & DIV ON
PFDCP OFF
REF OFF
t = 5*Tref
State 1303
VCO & DIV ON
PFDCP ON
REF ON
WBW mode ON
t = (5+n)*Tref
State 1304
VCO & DIV ON
PFDCP, REF ON
NBW mode ON
WBW mode OFF
n = 21, 25, 37, 69

FIG. 13

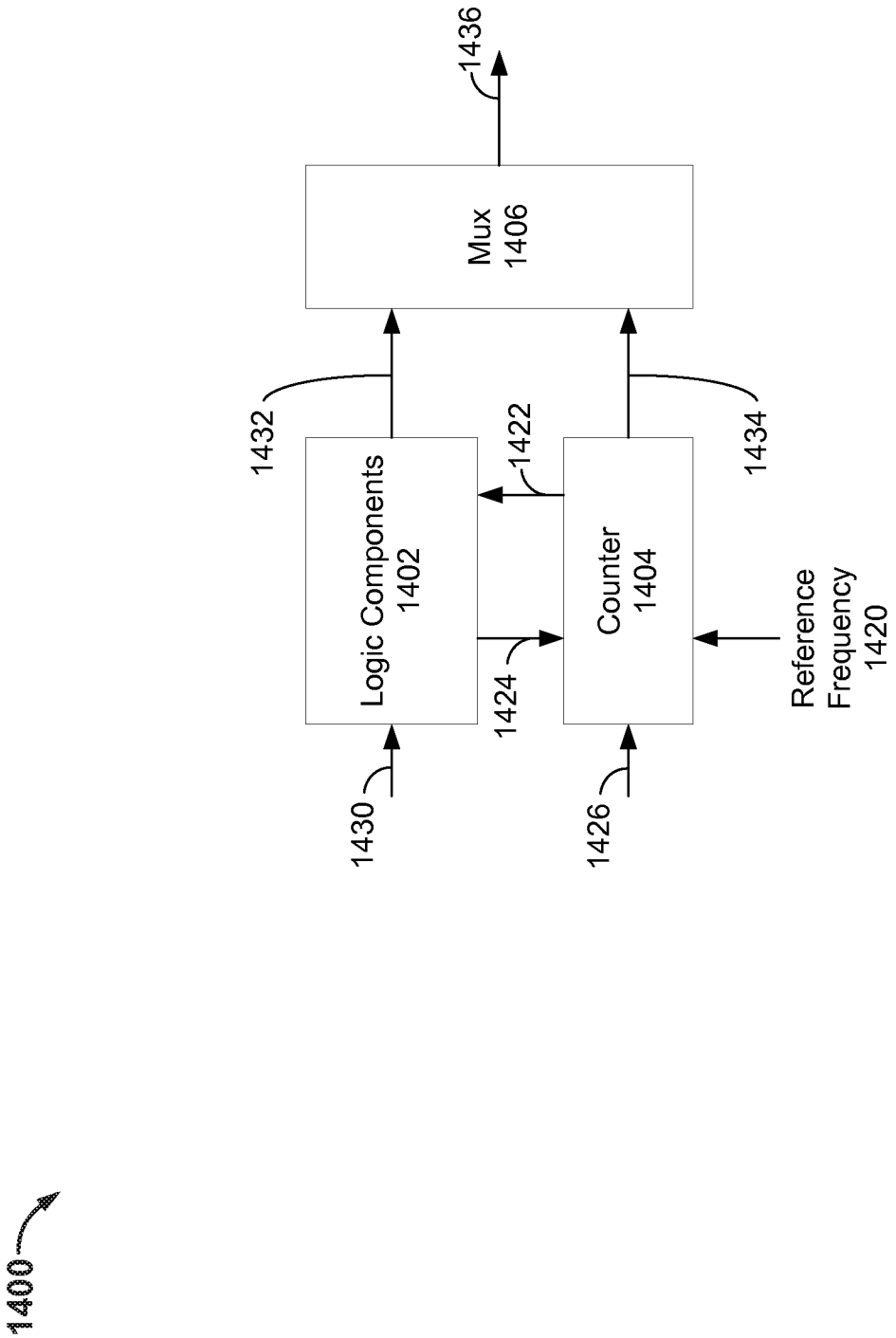
1400
1436
Mux
1406
1432
1422
1434
Logic Components
1402
Counter
1404
Reference
Frequency
1420
1424
1430
1426

FIG. 14

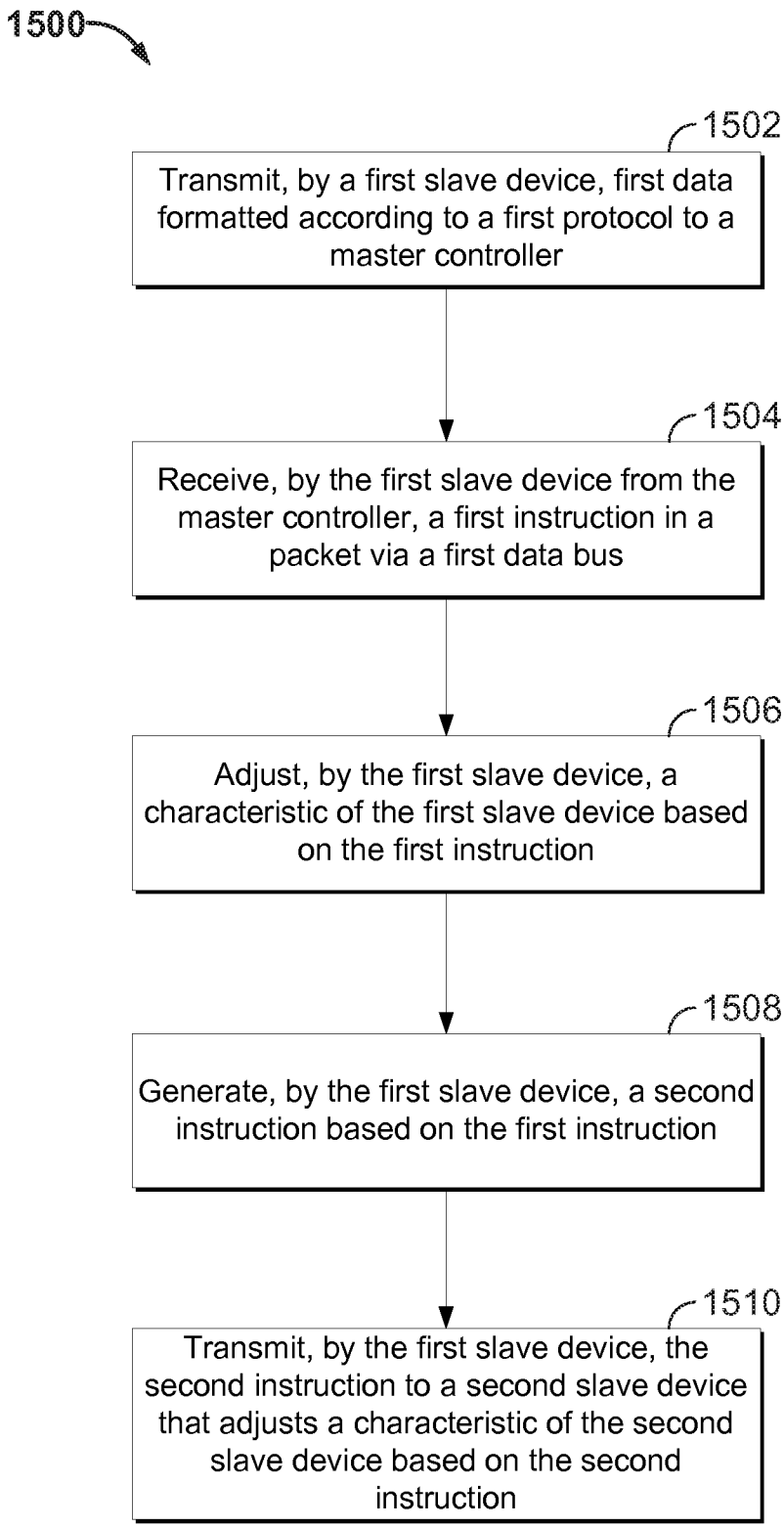
1500
1502
Transmit, by a first slave device, first data formatted according to a first protocol to a master controller
1504
Receive, by the first slave device from the master controller, a first instruction in a packet via a first data bus
1506
Adjust, by the first slave device, a characteristic of the first slave device based on the first instruction
1508
Generate, by the first slave device, a second instruction based on the first instruction
1510
Transmit, by the first slave device, the second instruction to a second slave device that adjusts a characteristic of the second slave device based on the second instruction

FIG. 15

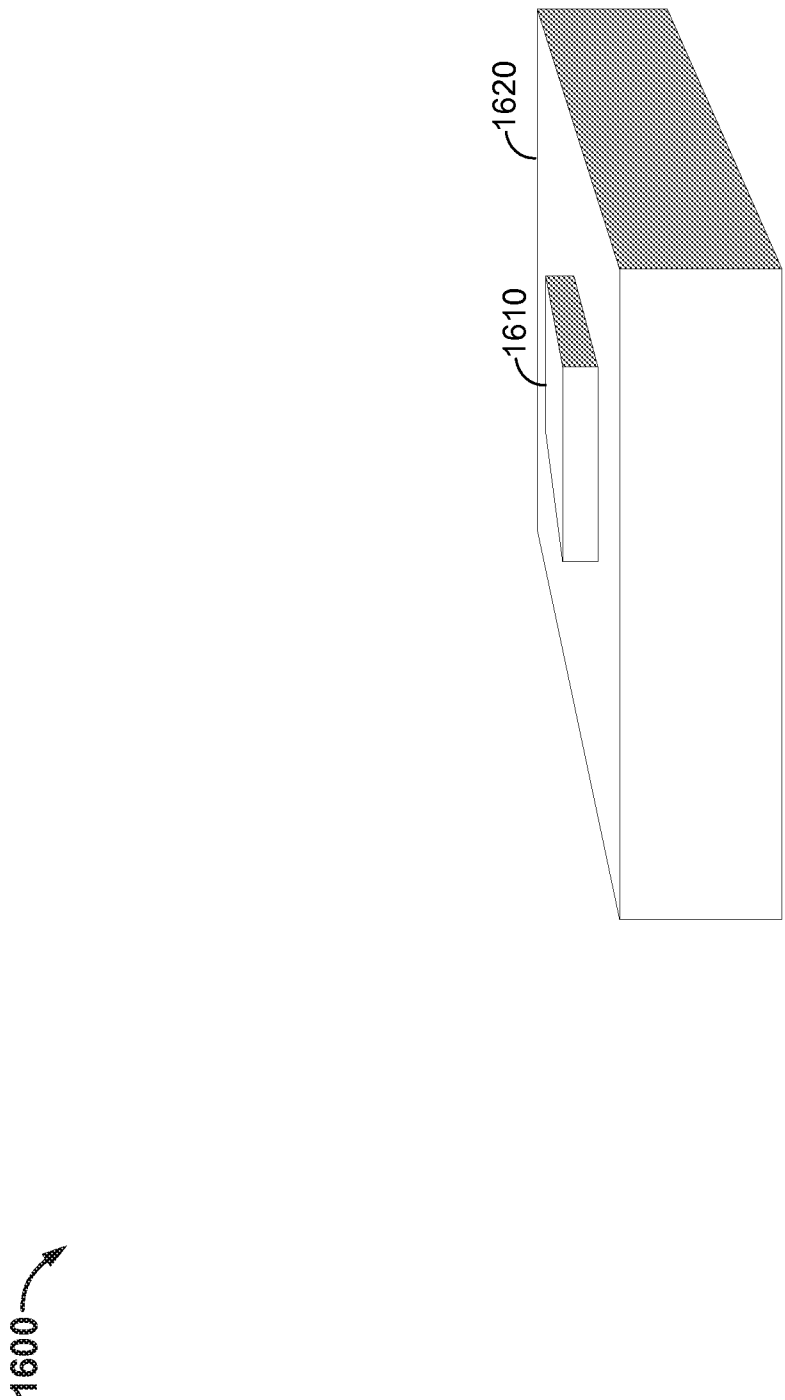

FIG. 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US13/67318

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 15/16; H04L 12/40; H04B 17/02 (2014.01)
USPC - 709/208; 370/257; 375/228
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) Classification(s): G06F 15/16; H04L 12/40; H04B 17/02 (2014.01)
USPC Classification(s): 709/208; 370/257; 375/228

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); ProQuest; IP.com; Google
master, slave, bus, protocol, interface

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y --- A	US 2012/0110106 A1 (DE LESCURE, B et al.) 3 May 2012, paragraphs [0035], [0037], and [0041]-[0043].	1 --- 2-4, 10/1 --- 5-9, 10/9, 11-26
Y	US 6160795 A (HOSEMANN, A) 12 December 2000, column 3, lines 28-47 and column 4, lines 1-15.	2-4
Y	US 2011/0002373 A1 (JEON, B) 6 January 2011, paragraphs [0077]-[0078].	10/1
A	US 2006/0222128 A1 (RAPHAELI, D) 5 October 2006, paragraphs [0019], [0020], and [0039].	5
A	US 2005/0088236 A1 (MATSUMOTO, H et al.) 28 April 2005, figure 11.	6-9, 15-18, and 23-26

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2014 (14.01.2014)	24 JAN 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774