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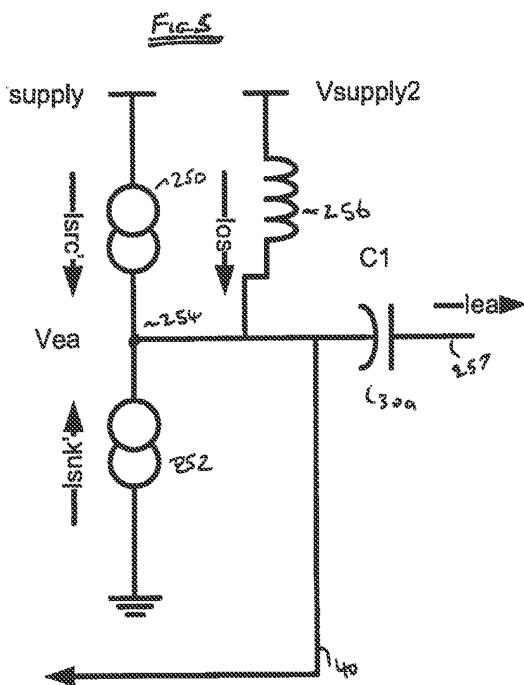
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(54) Title of the Invention: Improved efficiency for linear amplifier of envelope tracking modulator

Abstract Title: An envelope-tracking amplifier with a linear amplifier having an output offset current for improved efficiency

(57) The dissipations in the sourcing 250 and sinking 252 output portions of a linear amplifier in an envelope tracking power supply are made equal, despite the asymmetric nature of the envelope waveform (figure 4), by providing an offset current I_{os} that makes the average pull-up current less than the average pull-down current, thereby improving the efficiency of the output stage. The offset current may be fed through an inductor 256 from a controlled voltage $V_{supply2}$ provided by a switch mode converter under control of a loop (figure 8) acting to equalise the dissipations in the sourcing and sinking parts. Alternatively the control loop may apply an offset current proportional to the difference between the mean and mid-point voltages of the envelope waveform



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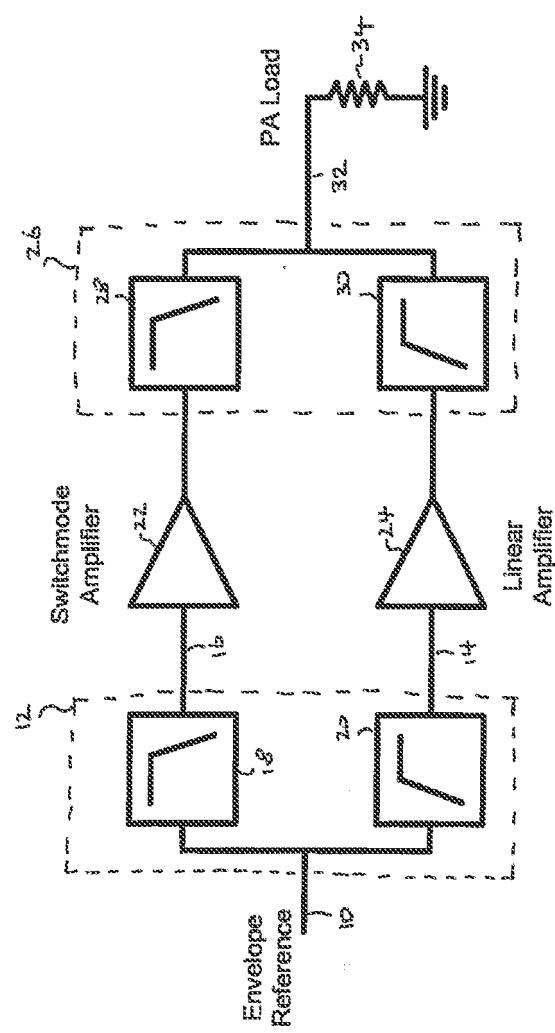


Fig1

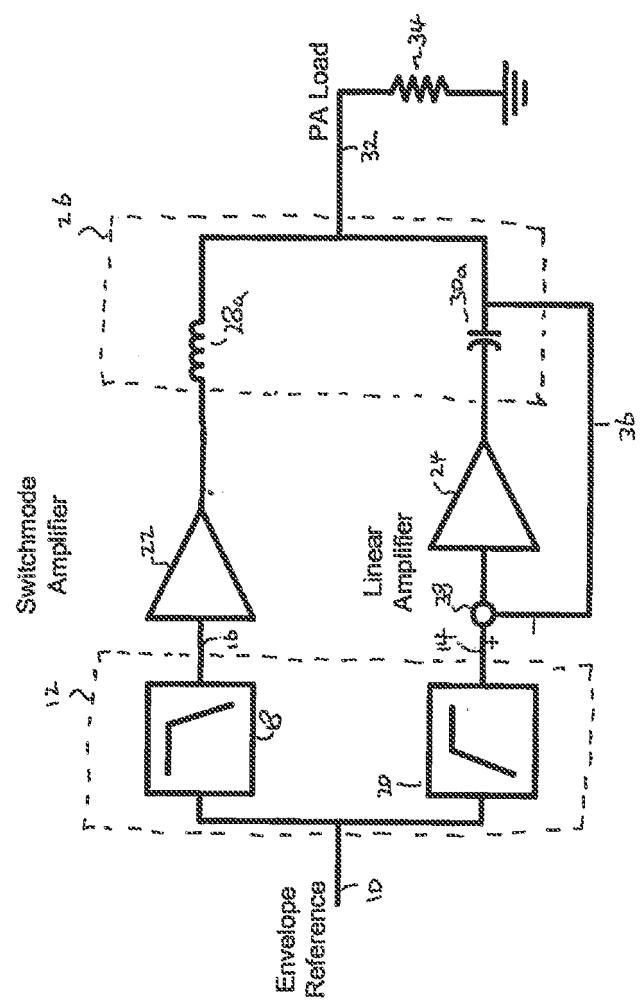


Fig2

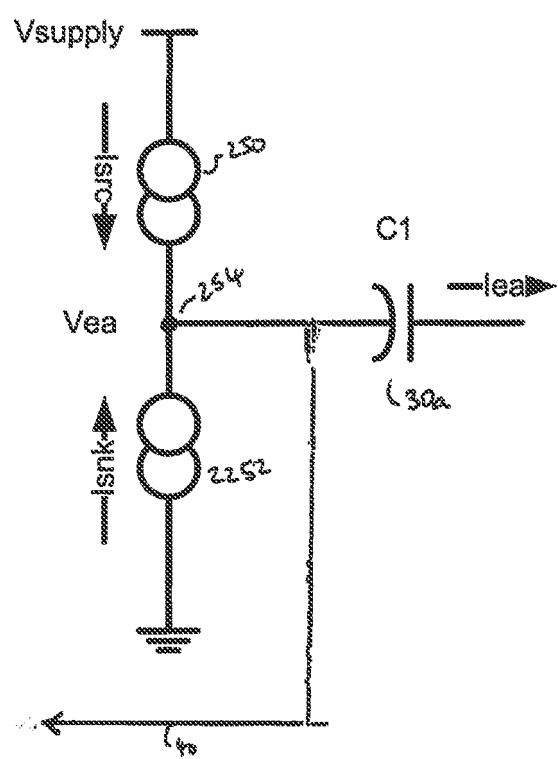
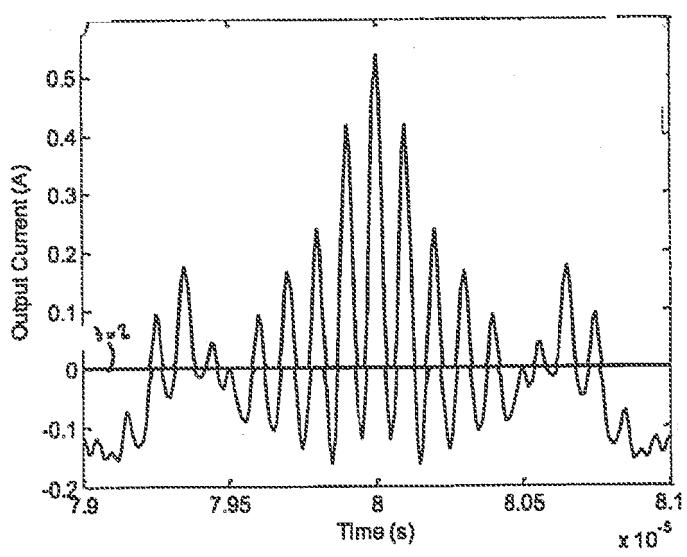
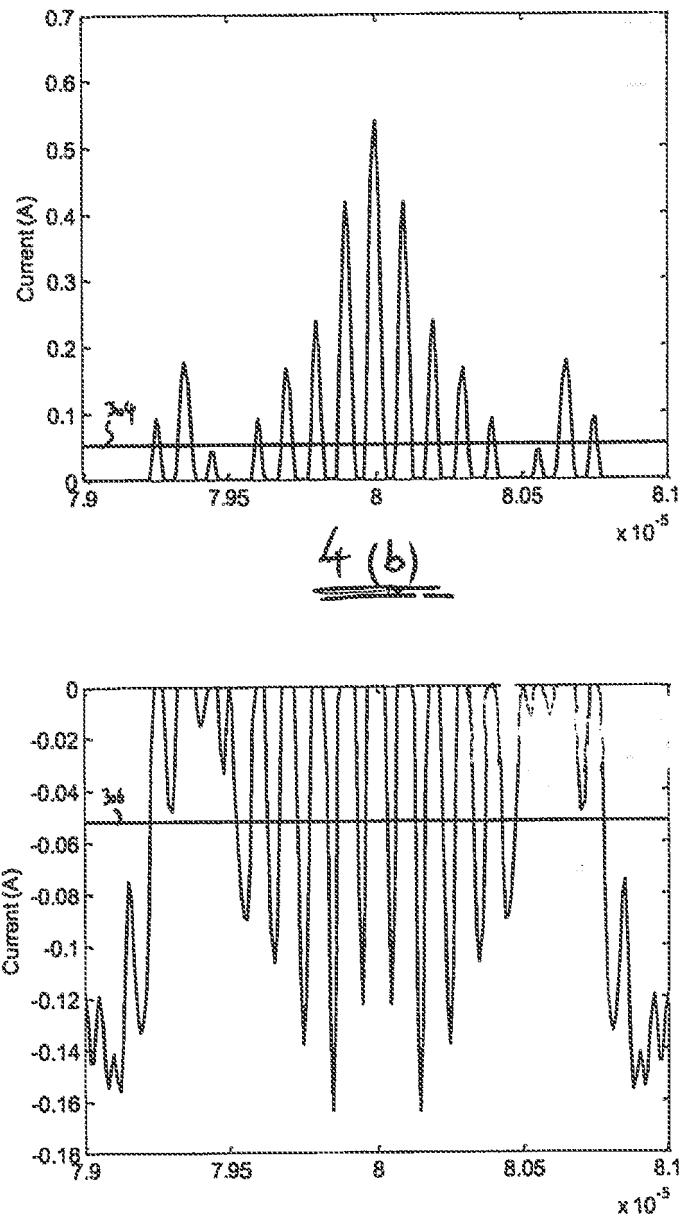


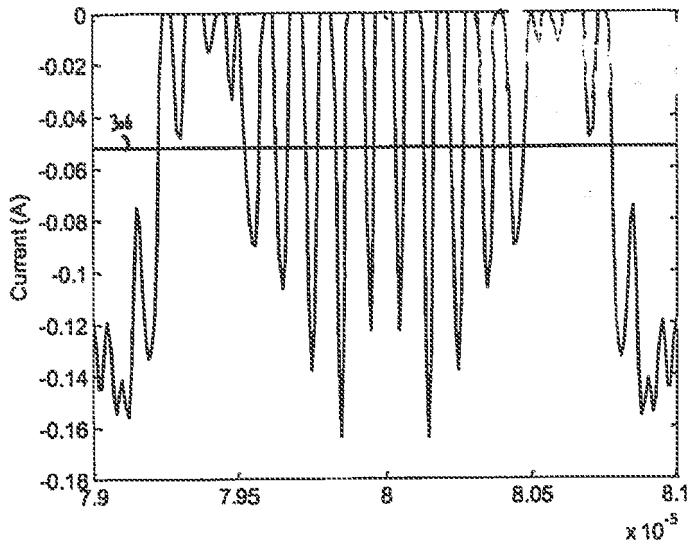
Fig. 3.



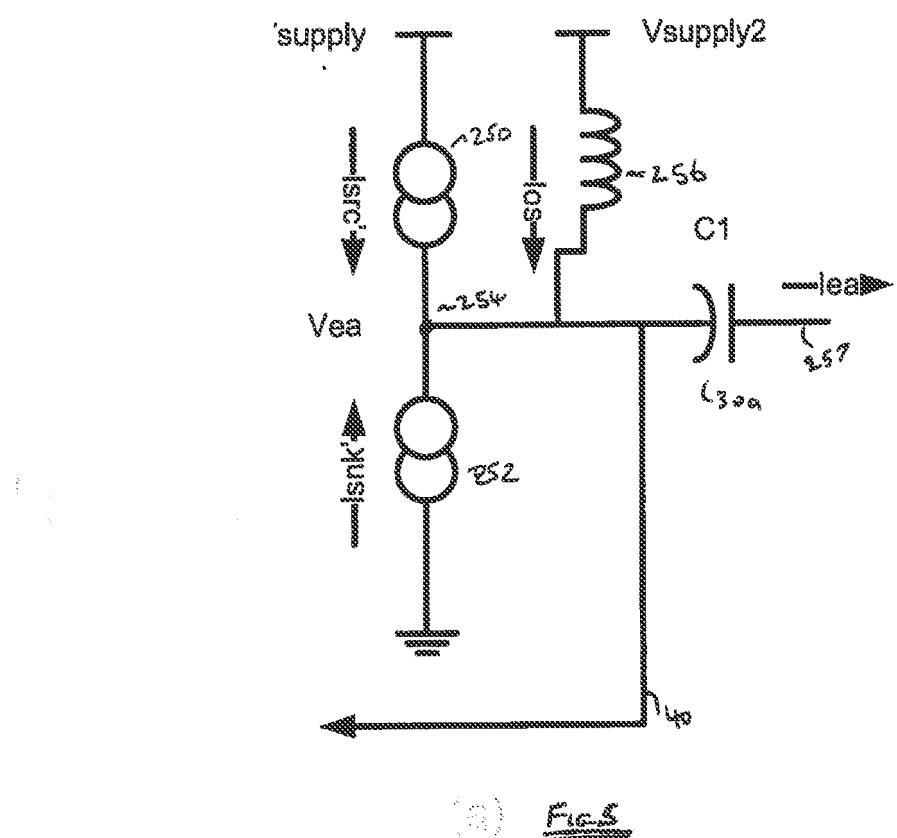
4 (a)

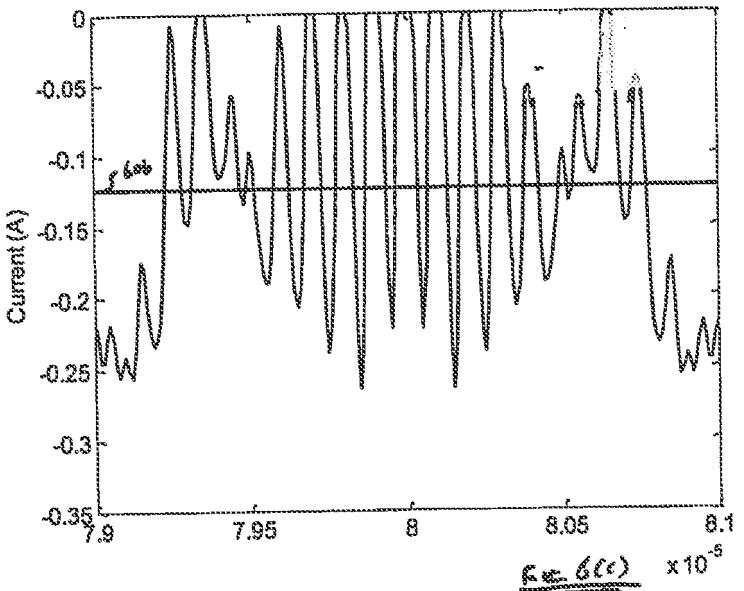
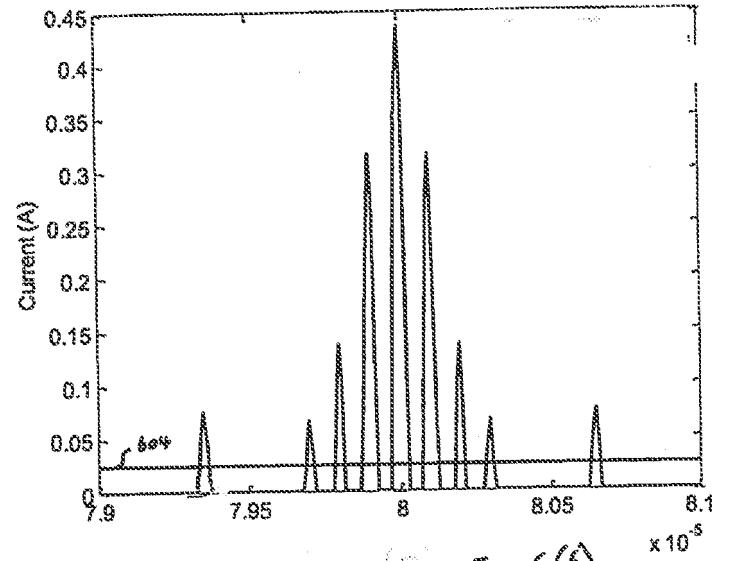
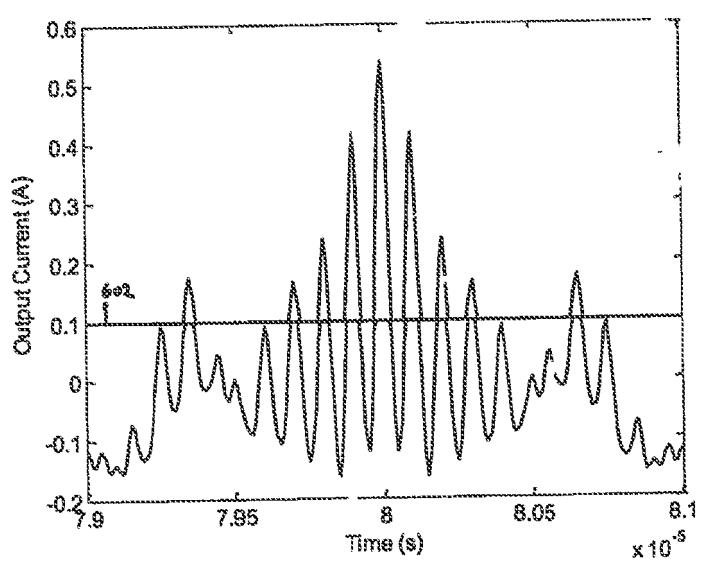


4 (b)



4 (c)





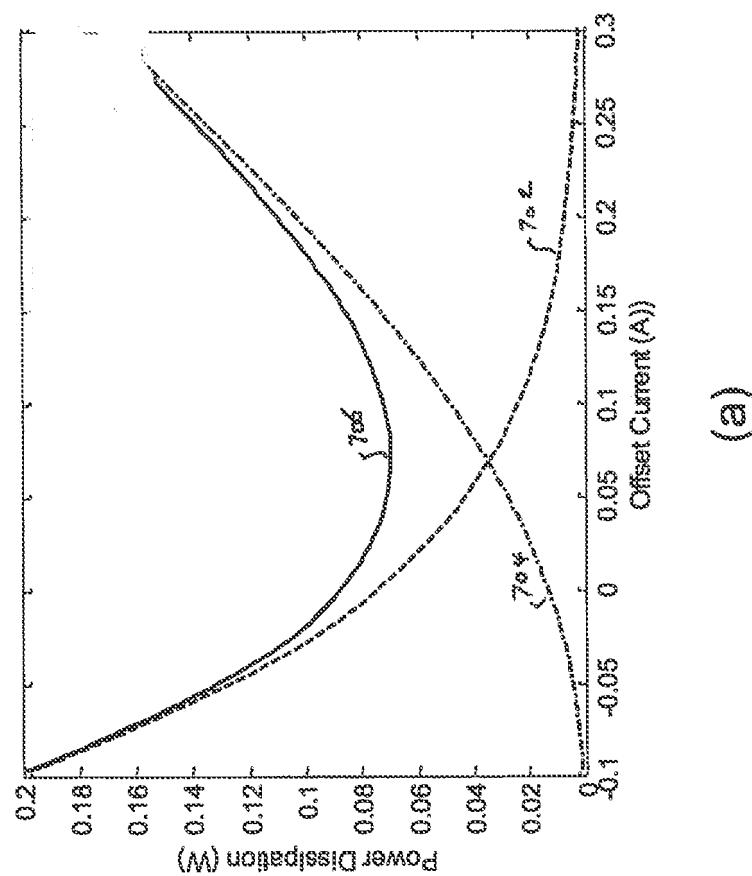
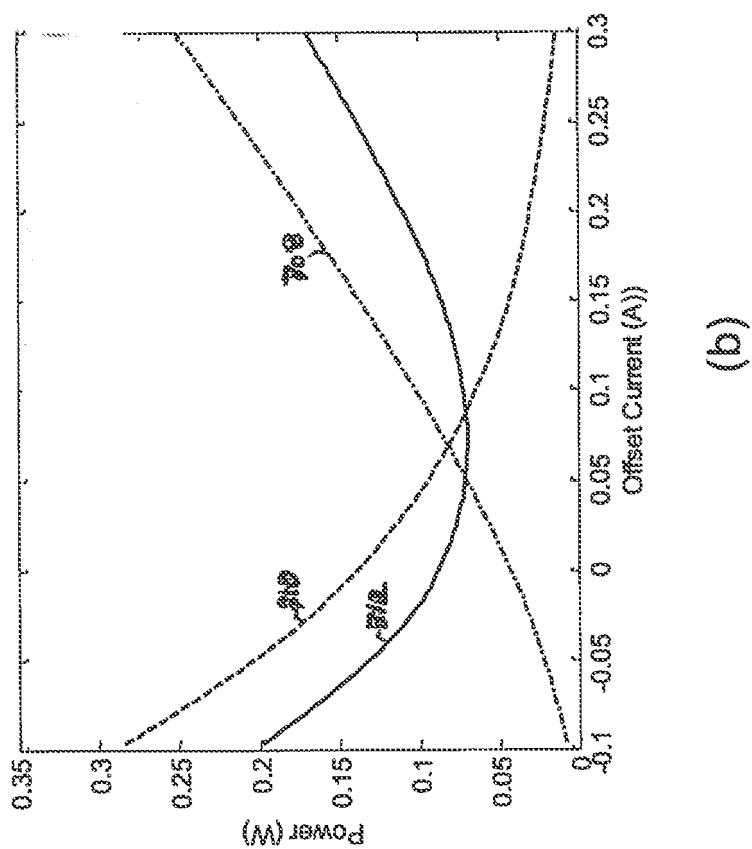


Fig 7

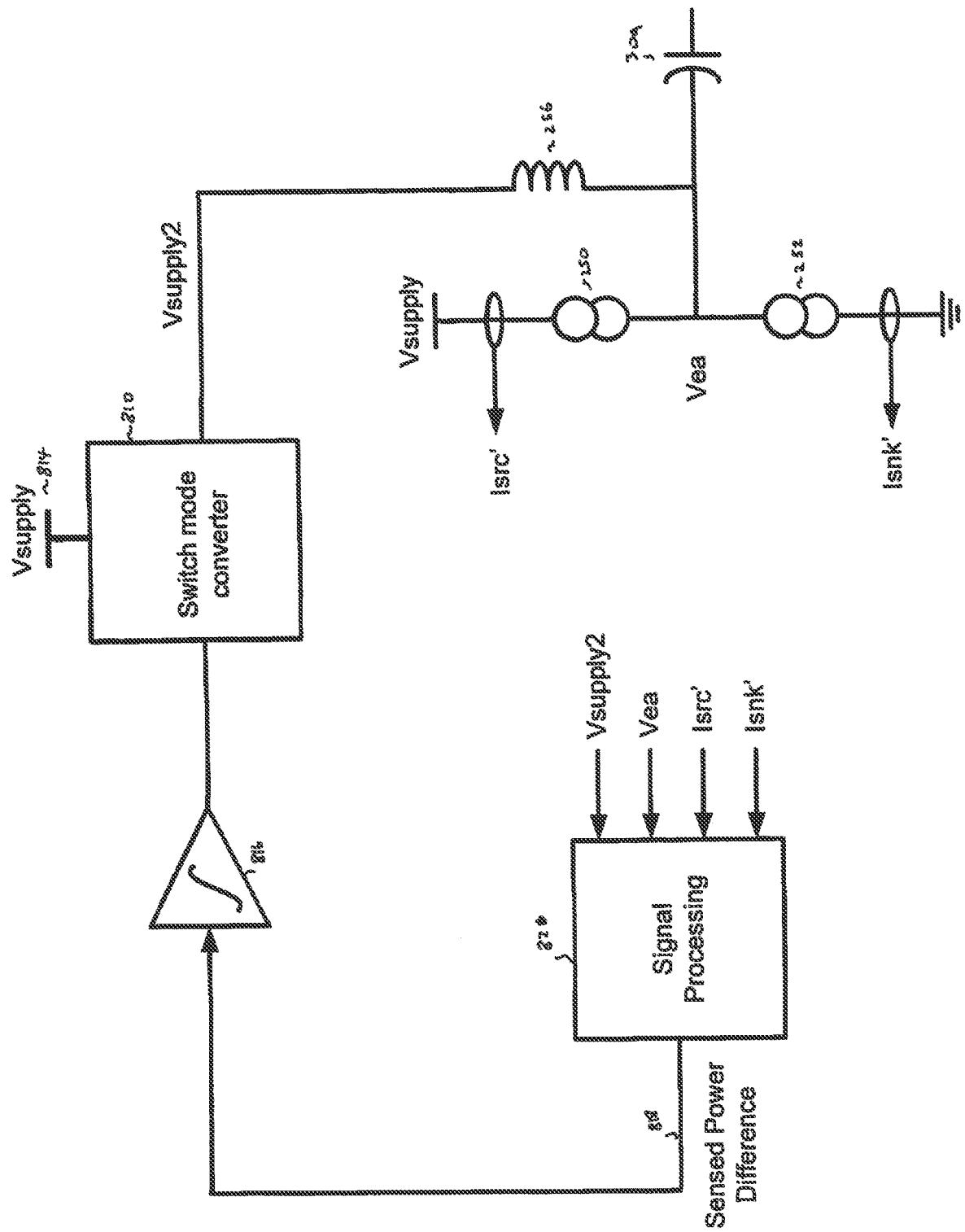
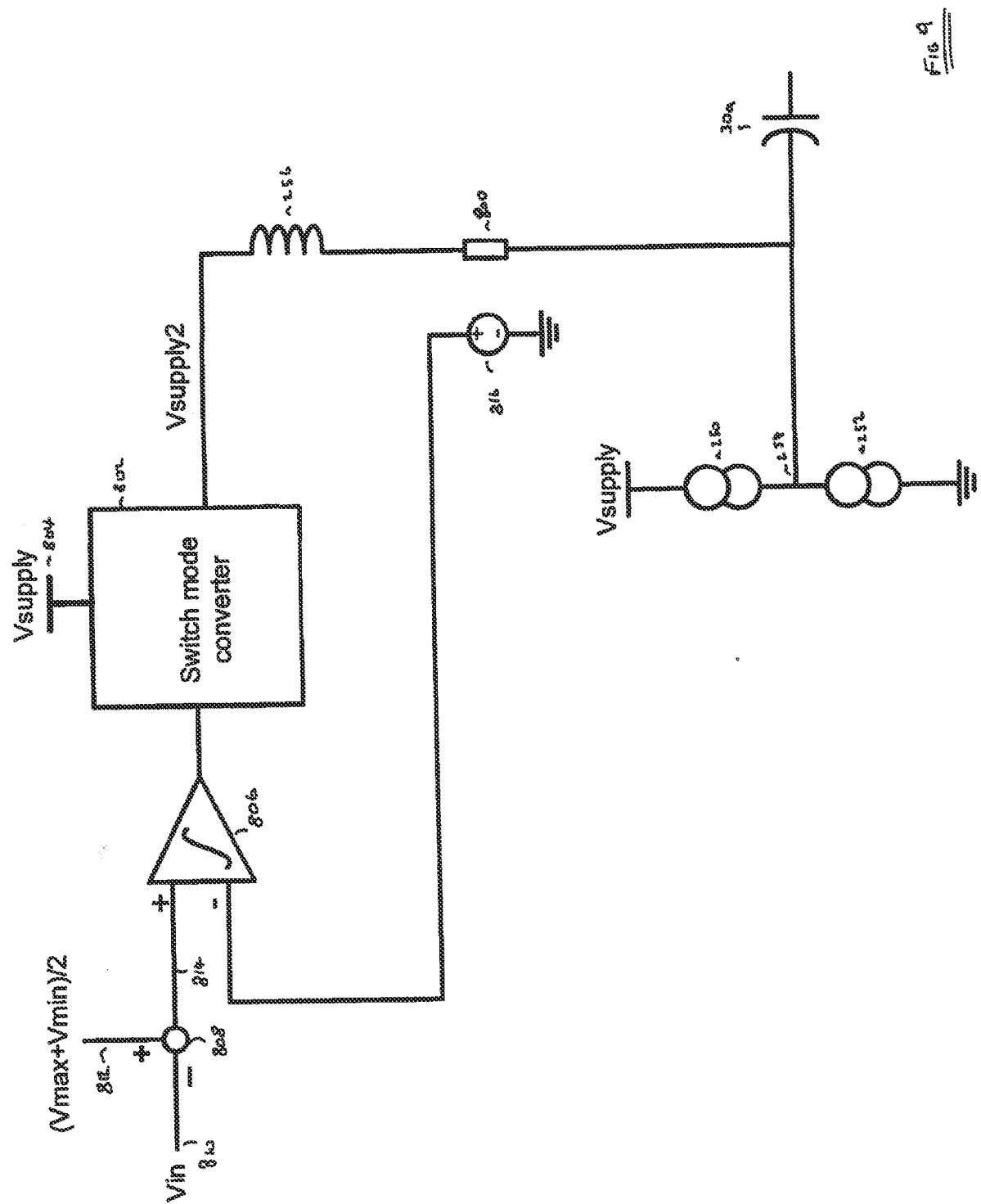


Fig. 4

Fig. 8



IMPROVED EFFICIENCY FOR LINEAR AMPLIFIER OF ENVELOPE TRACKINGMODULATOR

BACKGROUND TO THE INVENTION:

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Field of the Invention:

The invention relates to envelope tracking modulated power supplies suitable for radio frequency power amplifier applications. The invention is particularly concerned with 10 such power supplies in which a reference signal is used as an input to a low frequency path and a high frequency path, and in which each path generates separate outputs which are combined to form a supply voltage.

15 Description of the Related Art:

Envelope tracking power supplies for radio frequency power amplifiers are well-known in the art. Typically a reference signal is generated based on an envelope of an input signal to be amplified. An envelope tracking power supply generates a 20 supply voltage for the power amplifier which tracks the reference signal.

Figure 1 shows a prior art envelope tracking (ET) modulator architecture in which a frequency splitter 12 is used to divide an incoming envelope reference signal on line 10 into a 25 high frequency (HF) path signal on line 14 and a low frequency (LF) path signal on line 16. The frequency splitter 12 may include a low pass filter 18 in the low frequency path and a high pass filter 20 in the high frequency path. The signal in the LF path on line 16 is amplified by an efficient switched 30 mode amplifier 22, and the signal in the HF path on line 14 is amplified by a wideband linear amplifier 24. A frequency

selective combiner 26 is used to combine the signals in the LF and HF paths after amplification. In Figure 1 the combiner 26 is illustrated as including a low frequency combining element (and high frequency blocking element) 28 in the low frequency path, and a high frequency combining element (and low frequency blocking element) 30 in the high frequency path. A combined signal from the combiner 26 on line 32 provides a feed to a load 34 which for the purposes of example is illustrated as a resistor. In a typical application the load 10 is a power amplifier (PA), and the reference signal is derived from an input signal to be amplified by the power amplifier.

An example of a power amplifier system incorporating a supply architecture such as illustrated in Figure 1 can be found in "Band Separation and Efficiency Optimisation in 15 Linear-Assisted Switching Power Amplifiers", Yousefzadeh et al, [IEEE Power Electronics Specialists Conference 2006].

Figure 2 shows an alternative prior art arrangement in which the frequency selective combiner 26 is an inductor-capacitor (LC) combiner. The low frequency combining element is an 20 inductor 28a, and the high frequency combining element is a capacitor 30a. In this arrangement a feedback path 36 takes a signal from the combiner (or modulator) output on line 32, to the input of the linear amplifier 24. The signal on the feedback path 36 is subtracted from the signal in the high 25 frequency path on line 14 by subtractor 38, to provide an input to the linear amplifier 24. The inclusion of the feedback path 36 achieves improved tracking accuracy compared to the arrangement of Figure 1.

An example of a power amplifier system incorporating a 30 supply architecture such as illustrated in Figure 2 can be found in "Efficiency Optimisation in Linear-Assisted Switching Power Converters for Envelope Tracking in RF Power

Amplifiers", Yousefzadeh et al, [IEEE Symposium on Circuits and Systems 2005].

It is an aim of the invention to provide an envelope tracking modulated power supply which offers improvements over 5 the prior art, such as the arrangements of Figures 1 and 2.

SUMMARY OF THE INVENTION:

The invention provides an envelope tracking power supply arranged to generate a modulated supply voltage in dependence 10 on a reference signal, comprising a first path for tracking low frequency variations in the reference signal and a second path for tracking high frequency variations in the reference signal, the second path including a linear amplifier, wherein the output stage of the linear amplifier comprises a current 15 source and a current sink connected to the high frequency output, there further being provided a DC offset current at the high frequency output.

The DC offset current may be chosen to minimise the power dissipated in the output stage of the linear amplifier.

20 The DC offset current may be derived from a further voltage supply which is lower than the output stage voltage supply.

25 The DC offset current may be provided via an inductor connected between the further power supply and the high frequency output.

The envelope tracking power supply may further comprise sensing the power difference in an output, and integrating the sensed power difference to control a switch mode converter to generate a second supply voltage to generate the DC offset

current. Sensing the power difference may comprise measuring a supply voltage for generating the DC offset current, the output voltage, the source current and the sink current.

A target DC offset current may be determined in dependence on the difference between the input voltage waveform and the halved sum of the maximum and minimum voltage levels of the input waveform voltage. An error between the target DC offset current and a measured DC offset current may be integrated and used to control a switch mode converter to generate a second supply voltage to generate the DC offset current.

An RF amplifier may include an envelope tracking power supply.

A mobile device for a mobile communication system may include an envelope tracking power supply.

An infrastructure element for a mobile communications system may include an envelope tracking power supply.

The invention further provides a method for an envelope tracking power supply arranged to generate a modulated supply voltage in dependence on a reference signal, comprising providing a first path for tracking low frequency variations in the reference signal and providing a second path for tracking high frequency variations in the reference signal, the second path including a linear amplifier, wherein the output stage of the linear amplifier comprises a current source and a current sink connected to the high frequency output, the method further comprising providing a DC offset current at the high frequency output.

BRIEF DESCRIPTION OF THE FIGURES:

The invention is now described by way of example with reference to the accompanying Figures, in which:

5 Figure 1 illustrates a prior art envelope tracking modulated supply with high and low frequency paths;

Figure 2 illustrates a prior art envelope tracking modulated supply incorporating feedback in the high frequency path;

10 Figure 3 illustrates a modified implementation an output of a linear amplifier in accordance with the arrangement of Figure 1 or Figure 2;

Figure 4(a) to 4(c) illustrate current flow in the arrangement of Figure 3;

15 Figure 5 illustrates the implementation of the output of a linear amplifier in the arrangement of Figure 1 or Figure 2 in accordance with an embodiment of the present invention;

Figures 6(a) to 6(c) illustrate current flow in the the arrangement of Figure 5;

20 Figures 7(a) and 7(d) illustrate waveform plots in the arrangement of Figures 3 and 5;

Figure 8 illustrates the implementation of the output of a linear amplifier in the arrangement of Figure 1 or Figure 2 in accordance with an exemplary embodiment of the present invention; and

25 Figure 9 illustrates the implementation of the output of a linear amplifier in the arrangement of Figure 1 or Figure 2 in accordance with another exemplary embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS:

In the following description the invention is described with reference to exemplary embodiments and implementations. The invention is not limited to the specific details of any 5 arrangements as set out, which are provided for the purposes of understanding the invention.

Embodiments of the invention may apply to different feedback architectures for the linear amplifier in the high frequency path. The invention and its embodiments are not limited to a 10 particular feedback arrangement in the high frequency path. For example in the foregoing illustration of Figure 2 an arrangement is illustrated in which the linear amplifier receives a feedback from the output of the combiner. The present invention may also apply, for example, to an 15 arrangement in which the linear amplifier receives a feedback from the output of the linear amplifier at the input to the combiner, and in which the path containing the linear amplifier does not include a high frequency filter such as filter 20 in Figure 2, the linear amplifier path receiving the 20 full-spectrum reference signal.

In general in a hybrid envelope tracking modulator (i.e. an architecture using a switched mode amplifier and a linear amplifier) as illustrated in Figure 2, a significant proportion of the total modulator power dissipation occurs in 25 the output stage of the linear amplifier.

This can be understood with reference to Figure 3, which illustrates an exemplary implementation of the linear amplifier 24 Class B output stage. As illustrated, a current source 250 is connected between a supply voltage V_{SUPPLY} and a 30 common node 254, and a current sink 252 is connected between the common node 254 and electrical ground V_{GND} . An

instantaneous source current I_{SRC} flows in the current source element 250, and an instantaneous current I_{SNK} flows in the current sink element 252. At any given instant current flows in either the source device 250 or the sink device 252, and the current in the inactive device is zero. An output voltage V_{EA} is formed at node 254. The combiner capacitor 30a of Figure 2 is illustrated as connected between the node 254 and the output of the combiner. A current I_{EA} flows in the combiner capacitor 30a.

For the purposes of example, the arrangement of Figure 3 shows a feedback path 40 which represents a feedback from the output of the linear amplifier, before the combiner, to the input of the linear amplifier. The feedback is not described in more detail herein because it does not form part of the present invention. The current flow in the feedback path is assumed to be sufficiently low to be ignored.

No DC current can flow through the combiner capacitor 30a. Hence in the prior art arrangement of Figure 3 the value of the average source current I_{SRC} from current source 250 must be equal to the value of the average sink current I_{SNK} from current sink 252.

In general the required modulator output voltage provided by the linear amplifier 24 may typically exhibit significant asymmetry, and this in turn results in asymmetry of the output current I_{EA} of the linear amplifier 24.

This is illustrated by the waveform of Figure 4(a) which shows a plot of output current I_{EA} against time. The current above the zero level 302 represents output positive currents which flow in the source transistor 250, and the current below the zero level 302 represents the output negative currents

which flow in the sink transistor 252. The combined source and sink currents represent the output current I_{BA} .

The values of each of the average source I_{SRC} and sink I_{SNK} currents are equal as shown in Figures 4(b) and 4(c), which 5 shows plots of the source and sink currents against time.

The line 304 in Figure 4(b) shows the average current in source device 250 and the line 306 in Figure 4(c) shows the average current in the sink device 252. The average current in source device 250 is equal to the average current in sink 10 device 252.

However in the example as shown the power dissipated in the upper device (the current source 250) is much greater than the power dissipated in the lower device (current sink 252). This 15 disparity in power dissipation is due to the waveform asymmetry and results in much higher voltages across the upper (source) device.

It can thus be seen that the necessity for the average sink and source currents to be equal for the output topology of Figure 3 is disadvantageous.

20 In accordance with a preferred embodiment of the invention, an extra voltage supply is used to add a DC (or low frequency) offset current via an inductor to the output node of the linear amplifier 24. There is thus no longer a requirement for the average source and sink currents to be equal.

25 Figure 5 shows such a modified topology. The arrangement of Figure 3 is modified such that an inductor 256 is included between a second supply voltage $V_{SUPPLY2}$ and the node 254. The inductor 256 provides an offset current I_{OS} , which flows in the inductor 256 from the voltage supply $V_{SUPPLY2}$.

The instantaneous current in the current source 250 is modified to $I_{SRC'}$ and the instantaneous current in the current sink 252 is $I_{SNK'}$. The output current I_{EA} flows in the output capacitor 30a, and the output voltage V_{EA} is formed at the node 5 254.

The waveform of Figure 6(a) shows the output current I_{EA} of the linear amplifier 24, which is the same as that shown in Figure 4(a). In accordance with the invention therefore, the output current I_{EA} of the linear amplifier is unchanged. As 10 illustrated in Figure 6, the portion of the output current above the line 602 is provided by the source transistor 250. The portion of the output current below the line 602 is provided by the sink transistor 252.

Figures 6(b) and 6(c) show the modified source $I_{SRC'}$ and sink 15 $I_{SNK'}$ currents from the current source element 250 and current sink element 252 respectively. In the example shown the modified source current $I_{SRC'}$ is decreased by offset current I_{os} and the modified sink current is increased by offset current I_{os} . The lines 604 and 606 in the respective Figures 6(b) and 20 6(c) represent the modified average currents flowing in the respective source and sink transistors.

As illustrated, by comparing Figures 4(b) and 4(c) with Figures 6(b) and 6(c), the effect of the additional offset current I_{os} supplied via inductor 256 is to reduce the average 25 source current by I_{os} from I_{SRC} to $I_{SRC'}$, and increase the average sink current by I_{os} from I_{SNK} to $I_{SNK'}$. This reduces the power dissipated in the current source 250 and increases the power dissipated in the current sink 252.

Figure 7(a) shows the dissipation 702, 704 in the output 30 stage source and sink current devices 250 and 252

respectively, and the total dissipation 706, as a function of the offset current I_{os} for the arrangement of Figure 5.

It can be seen that for the particular waveform illustrated the minimum dissipation in Figure 7(a) is approximately 20% less than the dissipation with no offset current. This difference in dissipation is strongly dependant on the waveform asymmetry and is larger for more asymmetric waveforms.

The instantaneous power dissipation in the source and sink output devices 250 and 252 cannot easily be directly measured, but the average current through the source and sink devices 250 and 252 and the average output voltage can all be readily measured. Hence it is possible to calculate the 'sensed' powers as a proxy for the dissipated powers using these average parameters.

Figure 7(b) shows the sensed powers for the source device 710, sink device 708 and the total sensed power 712.

Inductor 250 ideally has zero DC resistance, hence the DC voltage at both terminals of the inductor 250 is the same.

Referring to Figure 5, the sensed source power can be calculated as:

$$\text{avg}(V_{\text{SUPPLY}} - V_{\text{SA}}) \times \text{avg}(I_{\text{SRC}})$$

The sensed sink power can be calculated as:

$$\text{avg}(V_{\text{SA}}) \times \text{avg}(I_{\text{SNK}})$$

where:

V_{SUPPLY} = the supply voltage applied to the feed inductor;

V_{SA} = the output voltage of the stage;

$\text{avg}(I_{\text{SRC}})$ = the average source current; and

avg(I_{SNX}) = the average sink current.

The minimum in total sensed power occurs at the same value of offset current as the minimum dissipated power, as shown in Figure 7, hence minimising sensed power maximises the 5 efficiency of the supply modulator.

The additional voltage supply $V_{SUPPLY2}$ in Figure 5 is assumed to be generated using a high efficiency power converter, and the power loss in feed inductor 256 is assumed to be minimal.

Figure 8 shows a direct technique for generating the offset 10 current in which a negative feedback loop may be used to minimise the total sensed power by minimising the difference between the two sensed powers, by integrating the error to make small adjustments to the output voltage of the second supply $V_{SUPPLY2}$.

15 Figure 8 shows the output stage of the error amplifier comprising current source 250, current sink 252, combining capacitor 30a and DC current offset feed inductor 256. The supply voltage $V_{SUPPLY2}$ is provided by a switch mode converter 810, which is connected to a supply voltage V_{SUPPLY} denoted by 20 reference numeral 814.

The input to the switch mode converter 810 is provided by an integrator 816. The input to the integrator 816 is provided by a signal processing block 818, which generates a signal representing the sensed power difference on line 818 to the 25 input of the integrator 816 based on the second supply voltage $V_{SUPPLY2}$, the average output voltage V_{ea} , and the average of the source and sink currents I_{SC} and I_{SNX} .

An indirect method of controlling the offset current exploits the fact that the offset current required depends on 30 the asymmetry of the waveform. If the waveform is symmetrical

the mean voltage lies midway between the minimum and maximum values of the waveform. If the mean voltage is less than midway between the minimum and maximum values of the waveform a positive offset current is required to minimise the output 5 stage power dissipation. Similarly if the mean voltage is greater than midway between the minimum and maximum values of the waveform a negative offset current is required to minimise the output stage dissipation.

Figure 9 shows a control loop for implementing this indirect 10 concept.

The control loop includes the current source 250 and current sink 252 of the output stage, the combining capacitor 30a, and the DC current offset feed inductor 256. The inductor 256 is connected to the node 254 via current sense resistor 800.

15 The supply voltage $V_{\text{supply}2}$ is provided by a switch mode converter 802, which is connected to a supply voltage V_{supply} denoted by reference numeral 804.

The input to the switch mode converter is provided by an 20 integrator 806. A first input of the integrator is provided by a subtractor 808, which provides a difference on line 812 between the voltage which is midway between the minimum and maximum values of the input waveform (equal to $(V_{\text{max}}+V_{\text{min}})/2$) and the input waveform V_{in} 810 to give a voltage 25 representative of the offset current target on line 814 at the first input to the integrator 806. The second input to the integrator 806 is provided by a voltage source 816, which measures the current in the resistor 800 and provides a voltage representing the offset current.

The current offset target on line 814 is set as the 30 difference between the mean and median waveform voltages as

described above. The error between the target and measured offset current is integrated by integrator 806 and used to control the switch mode converter 802 which generates the second supply voltage $V_{SUPPLY2}$ which supplies the offset current 5 to the linear amplifier output stage via the inductor 256.

The generation of the offset current and the second supply may be achieved in a number of ways, both indirectly and directly, and the invention is not limited to any particular technique.

10 As discussed above the present invention may be applied to the output of a linear amplifier in a correction path of a modulated power supply, such as the linear amplifier of Figure 1 or Figure 2.

15 Such modulated power supplies may be used to provide the modulated power supply to an RF amplifier, which may comprises the load of Figure 1 or Figure 2.

RF amplifiers are used in mobile communication systems, in wireless devices and wireless infrastructure.

20 The invention and its embodiments relates to the application of envelope tracking (ET) to radio frequency (RF) power amplifiers, and is applicable to a broad range of implementations including cellular handsets, wireless infrastructure, and military power amplifier applications at high frequencies to microwave frequencies.

25 The invention has been described herein by way of example with reference to embodiments. The invention is not limited to the described embodiments, nor to specific combinations of features in embodiments. Modifications may be made to the embodiments within the scope of the invention. The scope of 30 the invention is defined by the appended claims.

CLAIMS:

1. An envelope tracking power supply arranged to generate a modulated supply voltage in dependence on a reference signal, comprising a first path for tracking low frequency variations in the reference signal and a second path for tracking high frequency variations in the reference signal, the second path including a linear amplifier, wherein the output stage of the linear amplifier comprises a current source and a current sink connected to the high frequency output, there further being provided a DC offset current at the high frequency output.
2. The envelope tracking power supply of claim 1 wherein the DC offset current is chosen to minimise the power dissipated in the output stage of the linear amplifier.
3. The envelope tracking power supply of claim 1 or claim 2 wherein the DC offset current is derived from a further voltage supply which is lower than the output stage voltage supply.
4. The envelope tracking power supply of any preceding claim wherein the DC offset current is provided via an inductor connected between the further power supply and the high frequency output.
5. The envelope tracking power supply of any preceding claim further comprising sensing the power difference in an output, and integrating the sensed power difference to control a switch mode converter to generate a second supply voltage to generate the DC offset current.

6. The envelope tracking power supply of claim 5 wherein sensing the power difference comprises measuring a supply voltage for generating the DC offset current, the output voltage, the source current and the sink current.

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7. The envelope tracking power supply of any one of claims 1 to 4 wherein a target DC offset current is determined in dependence on the difference between the input voltage waveform and the halved sum of the maximum and minimum voltage levels of the input waveform voltage.

10 8. The envelope tracking power supply of claim 7 wherein an error between the target DC offset current and a measured DC offset current is integrated and used to control a switch mode converter to generate a second supply voltage to generate the DC offset current.

15 9. An RF amplifier including an envelope tracking power supply according to any one of claims 1 to 8.

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10. A mobile device for a mobile communication system including an envelope tracking power supply according to any one of claims 1 to 9.

25 11. An infrastructure element for a mobile communications system including an envelope tracking power supply according to any one of claims 1 to 10.

30 12. A method for an envelope tracking power supply arranged to generate a modulated supply voltage in dependence on a reference signal, comprising providing a first path for tracking low frequency variations in the reference signal and

providing a second path for tracking high frequency variations in the reference signal, the second path including a linear amplifier, wherein the output stage of the linear amplifier comprises a current source and a current sink connected to the 5 high frequency output, the method further comprising providing a DC offset current at the high frequency output.

13. The method of claim 12 wherein the DC offset current is chosen to minimise the power dissipated in the output stage of 10 the linear amplifier.

14. The method of claim 12 or claim 13 wherein the DC offset current is derived from a further voltage supply which is lower than the output stage voltage supply.

15 15. The method of any one of claims 11 to 14 wherein the DC offset current is provided via an inductor connected between the further power supply and the high frequency output.

20 16. The method of any one of claims 11 to 15 further comprising sensing the power difference in an output, and integrating the sensed power difference to control a switch mode converter to generate a second supply voltage to generate the DC offset current.

25 17. The method of claim 16 wherein sensing the power difference comprises measuring a supply voltage for generating the DC offset current, the output voltage, the source current and the sink current.

30 18. The method of any one of claims 11 to 15 wherein a target DC offset current is determined in dependence on the

difference between the input voltage waveform and the halved sum of the maximum and minimum voltage levels of the input waveform voltage.

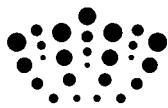
5 19. The method of claim 18 wherein an error between the target DC offset current and a measured DC offset current is integrated and used to control a switch mode converter to generate a second supply voltage to generate the DC offset current.

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Application No: GB1301852.8
Claims searched: 1-19

Examiner: Mr K Sylvan
Date of search: 24 July 2013

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	GB2424137 A Audio Partnership. See the output offset current source 12 in figure 7.
A	-	WO2012/110410 A1 Nujira. See figure 3.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^X :

Worldwide search of patent documents classified in the following areas of the IPC

H03F

The following online and other databases have been used in the preparation of this search report

WPI, EPDOC

International Classification:

Subclass	Subgroup	Valid From
None		