



- (51) **International Patent Classification:**  
*H04L 7/02* (2006.01)     *H04L 25/02* (2006.01)
- (21) **International Application Number:**  
PCT/US2013/046666
- (22) **International Filing Date:**  
19 June 2013 (19.06.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**  
13/537,823     28 June 2012 (28.06.2012)     US
- (71) **Applicant:** INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).
- (72) **Inventor:** YANG, Wei-Lien; 14405 S. 12th Pl., Phoenix, Arizona 85048 (US).
- (74) **Agent:** GARZA, John C.; TROP, PRUNER & HU, P.C., 1616 S. Voss Rd., Ste. 750, Houston, Texas 77057-2631 (US).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

[Continued on next page]

(54) **Title:** LOW POWER DATA RECOVERY

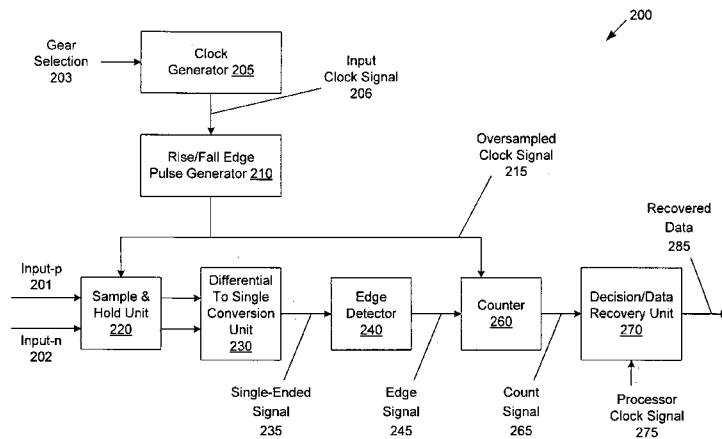


FIG. 3

(57) **Abstract:** In one embodiment, an apparatus may include a pulse generator to generate an oversampled clock signal. The apparatus may also include a sample and hold unit to provide at least two differential input signals based on the oversampled clock signal. The apparatus may further include a conversion unit to generate a single-ended signal based on the at least two differential input signals. The apparatus may also include a counter to determine a count of rising and falling edges of the single-ended signal based on the oversampled clock signal.

WO 2014/004225 A1

**Published:**

— *with international search report (Art. 21(3))*

## LOW POWER DATA RECOVERY

### Background

[0001] Embodiments relate generally to data interfaces for electronic devices.

[0002] Many electronic devices include multiple components coupled together by one or more data interfaces. For example, a cellular telephone may include a processor core coupled to a radio transceiver, a sound input device, a sound output device, a camera, a display device, a memory device, etc. The functionality of such components has been continually improved to meet market demands. Accordingly, the data interfaces between the components may need to be adapted to increasing bandwidth requirements.

### Brief Description of the Drawings

[0003] FIG. 1 is a block diagram of a system in accordance with one or more embodiments.

[0004] FIG. 2 is an example timing diagram in accordance with one or more embodiments.

[0005] FIG. 3 is a block diagram of a system in accordance with one or more embodiments.

[0006] FIG. 4 is a flow chart of a method in accordance with one or more embodiments.

[0007] FIG. 5 is an example timing diagram in accordance with one or more embodiments.

[0008] FIG. 6 is a block diagram of a processor in accordance with one or more embodiments.

[0009] FIG. 7 is a block diagram of an example system in accordance with one or more embodiments.

[0010] FIG. 8 is a block diagram of an example system in accordance with one or more embodiments.

Detailed Description

[0011] Referring to FIG. 1, shown is a block diagram of an apparatus 100 in accordance with one or more embodiments. As shown in FIG. 1, the apparatus 100 may include a link 120 connecting a transmitter 110 and a receiver 150. In accordance with some embodiments, the apparatus 100 may be any electronic device, such as a cellular telephone, a computer, a media player, a network device, etc.

[0012] In some embodiments, the transmitter 110 and the receiver 150 may exist to connect any components or peripherals of the apparatus 100, such as a processor, a processor core, a memory device, a display device, a sound device, a wireless transceiver, a camera, etc. For example, in one or more embodiments, the receiver 150 may connect to a processor having a ten bit parallel data path. Note that, while only one pair of transmitter 110 and receiver 150 is shown for the sake of clarity, the example shown in FIG. 1 is not intended to be limiting. Accordingly, it should be appreciated that any number of such transmitter-receiver pairs may exist to connect various components of the apparatus 100.

[0013] In accordance with some embodiments, the link 120 may be any electrical or data connection(s) (e.g., motherboard connection, input/output cable, network connector, bus, wireless link, etc.). In one or more embodiments, the transmitter 110 may include transmit logic 115 to manage data connections to the receiver 150. Further, in some embodiments, the receiver 150 may include receive logic 155 to manage the data connections from the transmitter 110.

[0014] In accordance with some embodiments, the link 120, the transmit logic 115, and the receive logic 155 may use one or more data interface protocols. For example, in some embodiments, the link 120, the transmitter 110, and the receiver 150 may use the M-PHY specification of the Mobile Industry Processor Interface (MIPI) Alliance (MIPI Specification for M-PHY Version 1.00.00 of February 8, 2011, approved April 28, 2011). In such embodiments, the link 120 may include serial lines carrying differential pulse width modulated (PWM) signals. Optionally, the PWM signals may be referred to as "self-clocking" if clock information is included in the period of the PWM waveform.

[0015] In one or more embodiments, the PWM signals of the link 120 may operate under one or more data rate ranges of the M-PHY specification (referred to as "GEARs"). For example, the link 120 may operate under GEAR 1 (3 Mbps to 9 Mbps), GEAR 2 (6 Mbps to 18 Mbps), GEAR 3 (12 Mbps to 36 Mbps), GEAR 4 (24 Mbps to 72 Mbps), GEAR 5 (48 Mbps to 144 Mbps), GEAR 6 (96 Mbps to 288 Mbps), GEAR 7 (192 Mbps to 576 Mbps), etc.

[0016] In accordance with some embodiments, the receive logic 155 may include functionality to recover data received from the transmitter 110 (e.g., PWM signals of the link 120). In some embodiments, the receive logic 155 may use an oversampled clock signal to recover the data. Further, in some embodiments, the oversampled clock signal may be generated using less power than that required by conventional techniques (e.g., analog circuits, clock data recovery circuits, etc.). This functionality of the receive logic 155 is described further below with reference to FIGs. 2-5.

[0017] In one or more embodiments, the transmit logic 115 and/or the receive logic 155 may be implemented in hardware, software, and/or firmware. In firmware and software embodiments, they may be implemented by computer executed instructions stored in a non-transitory computer readable medium, such as an optical, semiconductor, or magnetic storage device. While shown with this particular implementation in the embodiment of FIG. 1, the scope of the various embodiments discussed herein is not limited in this regard.

[0018] Referring to FIG. 2, shown is a timing chart of a system in accordance with one or more embodiments. The timing chart shows an example of power states (i.e., voltage levels) of differential-p line 121 and differential-n line 122 with respect to time. In some embodiments, the differential lines 121 and 122 may transport differential PWM signals, and may together correspond generally to the link 120 shown in FIG. 1.

[0019] In one or more embodiments, the differential lines 121 and 122 may be sampled for a designated time period of data transfer between transmitter and receiver to determine how the transferred data (e.g., a single PWM data bit) may be expressed. For example, as shown, the transferred data bit may constitute a

differential-p signal 123 when the differential-p line 121 is in a high power state and the differential-n line 122 is in a low power state during the sampled time period. Otherwise, the transferred data bit may constitute a differential-n signal 124 when the differential-n line 122 is in a high power state and the differential-p line 121 is in a lower power state during the sampled time period. In one or more embodiment, the differential lines 121 and 122 may be received and processed by the receive logic 155 shown in FIG. 1.

[0020] Referring to FIG. 3, shown is a block diagram of a receive logic 200 in accordance with one or more embodiments. More specifically, the receive logic 200 may generally correspond to all or a portion of the receive logic 155 shown in FIG. 1. As shown, in some embodiments, the receive logic 200 may include a clock generator 205, a rise/fall edge pulse generator 210, a sample and hold unit 220, a differential-to-single conversion unit 230, an edge detector 240, a counter 260, and a decision/data recovery unit 270.

[0021] In accordance with some embodiments, the clock generator 205 may receive a gear selection input 203. The gear selection input may be any identifier or other selective means used to identify any one of a number of gears. In some embodiments, the gear selection input may correspond generally to one of the gears defined by the MIPI Alliance M-PHY specification.

[0022] In one or more embodiments, the clock generator 205 may include functionality to generate an input clock signal 206. For example, in some embodiments, the clock generator 205 may include a delay locked loop (DLL), a phase locked loop (PLL), and/or any similar components. Further, in one or more embodiments, the clock generator 205 may generate the input clock signal 206 by oversampling a received reference clock signal. For example, in some embodiments, the clock generator 205 may receive a processor clock signal (not shown), and may generate the input clock signal 206 to be a multiple (e.g., 6X, 12X, etc.) of the processor clock signal.

[0023] In one or more embodiments, the input clock signal 206 may be provided to the rise/fall edge pulse generator 210. In some embodiments, the rise/fall edge

pulse generator 210 may include functionality to oversample the input clock signal 206 to obtain an oversampled clock signal 215. For example, the rise/fall edge pulse generator 210 may generate a pulse at every rising and falling edge of the input clock signal 206. As such, the frequency of the input clock signal 206 may be doubled by the oversampling logic of the rise/fall edge pulse generator 210 to generate the oversampled clock signal 215. In this manner, generating the oversampled clock signal 215 may require less power than conventional techniques for generating clock signals to match a selected gear. In some embodiments, the oversampled clock signal 215 may correspond to a pair of differential clock signals.

[0024] In accordance with some embodiments, the sample and hold unit 220 may receive two differential signals input-p 201 and input-n 202 (e.g., PWM signals received over the differential-p line 121 and the differential-n line 122 shown in FIG. 2). The sample and hold unit 220 may also receive the oversampled clock signal 215 as an input.

[0025] In one or more embodiments, the sample and hold unit 220 may include functionality to sample differential signals input-p 201 and input-n 202 for some time period based on the oversampled clock signal 215 (e.g., a cycle, half a cycle, etc.). Further, the sample and hold unit 220 may also include functionality to hold the differential signals 201, 202 for another time period based on the oversampled clock signal 215. In some embodiments, the sample time period and the hold time period may be equal. After holding the differential signals 201, 202 for the designated time period, the sample and hold unit 220 may transmit the differential signals 201, 202 to the differential-to-single conversion unit 230. In this manner, the sample and hold unit 220 may enable the input differential signals 201, 202 to be synchronized with the oversampled clock signal 215, thus facilitating data recovery (described below). In one or more embodiments, the sample and hold unit 220 may be any device or circuit capable of sampling a series of input signals that are buffered and then released upon the completion of a specified timing period.

[0026] In one or more embodiments, the differential-to-single conversion unit 230 receives the differential signals 201, 202 from the sample and hold unit 220. Further, the differential-to-single conversion unit 230 may include functionality to convert the

two differential signals 201, 202 to a single-ended signal 235 (e.g., a PWM signal). As shown, in one or more embodiments, the single-ended signal 235 may be provided to the edge detector 240.

[0027] In accordance with some embodiments, the edge detector 240 may include functionality to process the single-ended signal 235 to determine the occurrence of rising and falling edges in the single-ended signal 235. Further, in some embodiments, the edge detector 240 may provide an edge signal 245 to indicate the detection of rising and falling edges in the single-ended signal 235. For example, in one or more embodiments, the detection of a rising edge may result in the edge detector 240 providing a count-up indication in the edge signal 245 (e.g., a positive bit, number, symbol, etc.). Further, the detection of a falling edge may result in the edge detector 240 providing a count-down/reset indication in the edge signal 245.

[0028] In one or more embodiments, the counter 260 may include functionality to determine a count based on the edge signal 245 and the oversampled clock signal 215. For example, in some embodiments, the counter 260 may increase the count based on receiving a count-up indication of the edge signal 245 during a time period of the oversampled clock signal 215 (e.g., a cycle, a pulse, etc.). Further, in some embodiments, the counter 260 may decrease the count based on receiving a count-down indication of the edge signal 245 during a time period of the oversampled clock signal 215. In addition, the counter 260 may also include functionality to provide a count signal 265 based on the determined count.

[0029] In accordance with some embodiments, the decision/data recovery unit 270 may include functionality to recover data bits based on the count signal 265 and a processor clock signal 275 (e.g., a reference clock signal of a central processor). In one or more embodiments, the decision/data recovery unit 270 may determine a logical high bit value or a logical low bit value based on comparing the count signal 265 to a predefined threshold. For example, in some embodiments, a logical high bit value may be determined if the count is greater than or equal to a threshold value, and a logical low bit value may be determined if the count is less than the threshold value.

[0030] In one or more embodiments, the decision/data recovery unit 270 may recover a data bit based on whether it is received during a time period of the processor clock signal 275. For example, in some embodiments, the decision/data recovery unit 270 may include an elastic buffer to store and release data bits in synchronization with time period(s) of the processor clock signal 275.

[0031] Note that the examples shown in FIGs. 1-3 are provided for the sake of illustration, and are not intended to limit any embodiments. For example, embodiments may include any number and/or arrangement of transmitters 110 and/or receivers 150. In another example, it is contemplated that some embodiments may include any number of components in addition to those shown, and that different arrangement of the components shown may occur in certain implementations. Further, it is contemplated that specifics in the examples shown in FIGs. 1-3 may be used anywhere in one or more embodiments.

[0032] FIG. 4 shows a sequence 400 for data recovery in accordance with one or more embodiments. In one embodiment, the sequence 400 may be part of the receive logic 155 shown in FIG. 1. In other embodiments, the sequence 400 may be implemented by any other part of receiver 150. The sequence 400 may be implemented in hardware, software, and/or firmware. In firmware and software embodiments it may be implemented by computer executed instructions stored in a non-transitory computer readable medium, such as an optical, semiconductor, or magnetic storage device.

[0033] At step 410, differential input signals may be received from a transmitter. For example, referring to FIG. 3, the sample and hold unit 220 may receive two differential signals input-p 201 and input-n 202. In some embodiments, the differential signals may be received from a transmitter (e.g., transmitter 110 shown in FIG. 1). In one or more embodiments, the received differential signals may be PWM signals under the M-PHY specification.

[0034] At step 420, an oversampled clock signal may be generated based on a gear selection input. In accordance with some embodiments, the gear selection input may be any identifier or datum indicative of an enumerated gear (e.g., G1-G7)

defined by the MIPI Alliance's M-PHY specification or another specification. For example, referring to FIG. 3, the clock generator 205 may generate an input clock signal 206 based on the gear selection input 203. The rise/fall edge pulse generator 210 may then generate an oversampled clock signal 215 based on every rising and falling edge of the input clock signal 206. In one example, the frequency of the input clock signal 206 may be equivalent to six times the frequency of a reference clock signal (e.g., processor clock signal 275 shown in FIG. 3). Further, in this example, the frequency of the oversampled clock signal 215 may be equivalent to twelve times the frequency of the reference clock signal.

[0035] At step 430, the differential input signals (received at step 410) may be converted to a single-ended signal based on the oversampled clock signal. For example, referring to FIG. 3, the sample and hold unit 220 may sample and hold the differential signals input-p 201 and input-n 202 for some determined time period. Further, based on the oversampled clock signal 215, the differential-to-single conversion unit 230 may receive the differential signals 201, 202 from the sample and hold unit 220, and may convert the differential signals 201, 202 into the single-ended signal 235.

[0036] At step 440, the number of rising and falling edges may be counted for the single-ended signal. For example, referring to FIG. 3, the edge detector 240 may detect a rising edge in the single-ended signal 235, and may send a count-up indication in the edge signal 245 to the counter 260. Further, the edge detector 240 may detect a falling edge in the single-ended signal 235, and may send a count-down/reset indication in the edge signal 245 to the counter 260.

[0037] At step 450, a logical high or low value may be determined based on the edge count and the oversampled clock signal. For example, referring to FIG. 3, the counter 260 may increase or decrease a count based on the edge signal 245 during a time period of the oversampled clock signal 215. Further, the decision/data recovery unit 270 may determine a logical high bit value or a logical low bit value based on comparing the count signal 265 to a predefined threshold.

[0038] At step 460, data may be recovered based on the logical high or low value (determined at step 450). For example, referring to FIG. 3, the decision/data recovery unit 270 may recover a "1" data bit based on receiving a logical high value, or may recover a "0" data bit based on receiving a logical low value. Further, the decision/data recovery unit 270 may only recover a data bit if it is received during a time period of the processor clock signal 275. After step 460, the sequence 400 ends.

[0039] Referring now to FIG. 5, shown is a timing diagram of a system in accordance with one or more embodiments. Specifically, depicted is a series of square wave forms representative of the pulse-width modulated (PWM) signals involved in the previously-discussed systems and process (e.g., a MIPI M-PHY receiver architecture). In reference to the counter signal, the x-axis is time and the y-axis is a count value. In reference to all the other shown signals, the x-axis is also time but the y-axis is voltage.

[0040] The first waveform shown in FIG. 5 is a single-ended PWM signal. As discussed above, the single-ended PWM signal may be provided when the differential-to-single conversion unit 230 processes the differential signals 201, 202.

[0041] The second and third waveforms shown in FIG. 5 are count-down and count-up forms of the edge signal 245, respectively. As shown, the second waveform indicates count-down spikes corresponding to falling edges of the single-ended PWM signal. Similarly, the third waveform indicates count-up spikes corresponding to rising edges of the single-ended PWM signal.

[0042] The fourth and fifth waveforms shown in FIG. 5 are a processor clock signal and an oversampled clock signal, respectively. As shown, the oversampled clock signal has a greater pulse frequency than the processor clock signal.

[0043] The sixth and final waveform shown in FIG. 5 is a counter signal. In some embodiments, the count is incremented, decremented, or reset on the basis of count-up and count-down/reset signals generated by the edge detector 240. Accordingly, the present bit value maintained by the counter 260 at the end of each timing period marked by the processor clock signal is translated into a logical high or

low value for sending to the decision/data recovery unit 270. For example, the counter value is positive at the end of the first and third timing periods; as such, the bit value sent from the counter 260 to the decision/data recovery unit 270 is "1" or a high logical value. Conversely, the counter value is negative at the end of the second timing period; as such, the bit value sent from the counter 260 to the decision/data recovery unit 270 is "0" or a low logical value. As previously discussed, the decision/data recovery unit 270 performs data recovery based on the counter value received from the counter 260.

[0044] Referring now to FIG. 6, shown is a block diagram of a processor in accordance with one or more embodiments. As shown in FIG. 6, processor 600 may be a multicore processor including a plurality of cores 610a – 610n. Each core may be associated with a corresponding voltage regulator 612a – 612n. The various cores may be coupled via an interconnect 615 to an uncore logic that includes various components. As seen, the uncore logic may include a shared cache 630 which may be a last level cache. In addition, the uncore logic may include an integrated memory controller 640, various interfaces 650 and transmit/receive logic 655.

[0045] In one or more embodiments, transmit/receive logic 655 may include all or a portion of the receive logic 200 described above with reference to FIG. 3. Thus, the transmit/receive logic 655 may enable the cores 610a – 610n to synchronize or align data transfer with other components (e.g., components included in a mobile computing device).

[0046] With further reference to FIG. 6, processor 600 may communicate with a system memory 660, e.g., via a memory bus. In addition, by interfaces 650, connection can be made to various off-chip components such as peripheral devices, mass storage and so forth. While shown with this particular implementation in the embodiment of FIG. 6, the scope of the various embodiments discussed herein is not limited in this regard.

[0047] Embodiments may be used in many different environments. Referring now to FIG. 7, shown is a block diagram of a computer system 730 with which

embodiments can be used. The computer system 730 may include a hard drive 734 and a removable storage medium 736, coupled by a bus (shown as an arrow) to a chipset core logic 710. A keyboard and/or mouse 720, or other conventional components, may be coupled to the chipset core logic.

[0048] The core logic may couple to the graphics processor 712, and the applications processor 700 in one embodiment. The graphics processor 712 may also be coupled to a frame buffer 714. The frame buffer 714 may be coupled to a display device 718, such as a liquid crystal display (LCD) touch screen. In one embodiment, the graphics processor 712 may be a multi-threaded, multi-core parallel processor using single instruction multiple data (SIMD) architecture.

[0049] The chipset logic 710 may include a non-volatile memory port to couple to the main memory 732. Also coupled to the core logic 710 may be a radio transceiver and antenna(s) 721. Speakers 724 may also be coupled to core logic 710.

[0050] Referring now to FIG. 8, shown is a block diagram of an example system 800 with which embodiments can be used. As seen, system 800 may be a smartphone or other wireless communicator. As shown in the block diagram of FIG. 8, system 800 may include a baseband processor 810 which may be a multicore processor that can handle both baseband processing tasks as well as application processing. Thus baseband processor 810 can perform various signal processing with regard to communications, as well as perform computing operations for the device. In turn, baseband processor 810 can couple to a user interface/display 820 which can be realized, in some embodiments by a touch screen display. In addition, baseband processor 810 may couple to a memory system including, in the embodiment of FIG. 8 a non-volatile memory, namely a flash memory 830 and a system memory, namely a dynamic random access memory (DRAM) 835. As further seen, baseband processor 810 can further couple to a capture device 840 such as an image capture device that can record video and/or still images.

[0051] To enable communications to be transmitted and received, various circuitry may be coupled between baseband processor 810 and an antenna 880. Specifically, a radio frequency (RF) transceiver 870 and a wireless local area

network (WLAN) transceiver 875 may be present. In general, RF transceiver 870 may be used to receive and transmit wireless data and calls according to a given wireless communication protocol such as 3G or 4G wireless communication protocol such as in accordance with a code division multiple access (CDMA), global system for mobile communication (GSM), long term evolution (LTE) or other protocol. Other wireless communications such as receipt or transmission of radio signals, e.g., AM/FM, or global positioning satellite (GPS) signals may also be provided. In addition, via WLAN transceiver 875, local wireless signals, such as according to a Bluetooth™ standard or an IEEE 802.11 standard such as IEEE 802.11a/b/g/n can also be realized. Although shown at this high level in the embodiment of FIG. 8, understand the scope of the present invention is not limited in this regard.

[0052] Embodiments may be used in many different types of systems. For example, in one embodiment a communication device can be arranged to perform the various methods and techniques described herein. Of course, the scope of the present invention is not limited to a communication device, and instead other embodiments can be directed to other types of apparatus for processing instructions, or one or more machine readable media including instructions that in response to being executed on a computing device, cause the device to carry out one or more of the methods and techniques described herein.

[0053] Embodiments may be implemented in code and may be stored on a non-transitory storage medium having stored thereon instructions which can be used to program a system to perform the instructions. The storage medium may include, but is not limited to, any type of disk including floppy disks, optical disks, solid state drives (SSDs), compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[0054] The following clauses and/or examples pertain to further embodiments. One example embodiment may be an apparatus including: a pulse generator to generate an oversampled clock signal; a sample and hold unit to provide at least two differential input signals based on the oversampled clock signal; a conversion unit to generate a single-ended signal based on the at least two differential input signals; and a counter to determine a count of rising and falling edges of the single-ended signal based on the oversampled clock signal. The pulse generator may generate the oversampled clock signal based on rising edges and falling edges of an input clock signal. The apparatus may also include a clock generator to generate the input clock signal. The input clock signal may be a multiple of a processor clock signal. The apparatus may also include a decision/data recovery unit to recover data based on the count of rising and falling edges. The decision/data recovery unit may be to recover a logical high bit value if the count is greater than or equal to a threshold value. The decision/data recovery unit may also be to recover a logical low bit value if the count is less than the threshold value. The apparatus may also include an edge detector to detect the rising and falling edges of the single-ended signal. The sample and hold unit may be to sample each of the at least two differential input signals for a first time period. The sample and hold unit may be to hold each of the at least two differential input signals for a second time period. The sample and hold unit may also be to provide the at least two differential input signals based on a frequency of the oversampled clock signal. The counter may be to determine the count of rising and falling edges based on a time period of the oversampled clock signal. The at least two differential input signals may be Pulse Width Modulated (PWM) signals. The PWM signals may conform to the Mobile Industry Processor Interface (MIPI) M-PHY Specification.

[0055] Another example embodiment may be a system including: a system on a chip comprising at least one core having at least one execution unit and receiver logic, the receiver logic including a clock generator to generate an input clock signal, a pulse generator to generate an oversampled clock signal based on the input clock signal, a sample and hold unit to provide two or more differential input signals based on the oversampled clock signal, a conversion unit to generate a single-ended signal based on the two or more differential input signals, and a counter to determine a

count of rising and falling edges of the single-ended signal based on the oversampled clock signal. The system may also include a wireless device coupled to the system on the chip via an interconnect, where the interconnect is used to communicate data between the wireless device and the receiver logic of the system on the chip. The receiver logic may also include a decision/data recovery unit to recover data based on the count of rising and falling edges. The decision/data recovery unit may include an elastic buffer synchronized to a processor clock signal. The receiver logic may also include an edge detector to detect the rising and falling edges of the single-ended signal. The clock generator may include a delay locked loop (DLL). The clock generator may include a phase locked loop (PLL). The clock generator may be to generate the input clock signal based on a gear selection input and a reference clock signal. The pulse generator may be to generate the oversampled clock signal based on rising edges and falling edges of the input clock signal.

[0056] Yet another example embodiment may be a method including: generating, in a receiver logic of a first device, an oversampled clock signal based on an input clock signal; sampling and holding a plurality of differential input signals based on the oversampled clock signal; generating a single-ended signal based on the plurality of differential input signals; and determining a count of rising and falling edges of the single-ended signal based on the oversampled clock signal. The method may also include generating the input clock signal based on a gear selection input and a reference clock signal. The method may also include recovering data based on the count of rising and falling edges of the single-ended signal. Generating the oversampled clock signal may be based on rising edges and falling edges of the input clock signal. The plurality of differential input signals may be pulse width modulated (PWM) signals.

[0057] References throughout this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Thus, appearances of the phrase "one embodiment" or "in an embodiment" are not necessarily referring to the same

embodiment. Furthermore, the particular features, structures, or characteristics may be instituted in other suitable forms other than the particular embodiment illustrated and all such forms may be encompassed within the claims of the present application.

[0058] While the present invention has been described with respect to a limited number of embodiments for the sake of illustration, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

- 1 1. An apparatus comprising:  
2 a pulse generator to generate an oversampled clock signal;  
3 a sample and hold unit to provide at least two differential input signals based  
4 on the oversampled clock signal;  
5 a conversion unit to generate a single-ended signal based on the at least two  
6 differential input signals; and  
7 a counter to determine a count of rising and falling edges of the single-ended  
8 signal based on the oversampled clock signal.
  
- 1 2. The apparatus of claim 1, the pulse generator to generate the oversampled  
2 clock signal based on rising edges and falling edges of an input clock signal.
  
- 1 3. The apparatus of claim 2, further comprising a clock generator to generate the  
2 input clock signal.
  
- 1 4. The apparatus of claim 2, wherein the input clock signal is a multiple of a  
2 processor clock signal.
  
- 1 5. The apparatus of claim 1, further comprising a decision/data recovery unit to  
2 recover data based on the count of rising and falling edges.
  
- 1 6. The apparatus of claim 5, wherein the decision/data recovery unit is to  
2 recover a logical high bit value if the count is greater than or equal to a threshold  
3 value.
  
- 1 7. The apparatus of claim 6, wherein the decision/data recovery unit is to  
2 recover a logical low bit value if the count is less than the threshold value.
  
- 1 8. The apparatus of claim 1, further comprising an edge detector to detect the  
2 rising and falling edges of the single-ended signal.

- 1 9. The apparatus of claim 1, the sample and hold unit to sample each of the at  
2 least two differential input signals for a first time period.
- 1 10. The apparatus of claim 9, the sample and hold unit to hold each of the at least  
2 two differential input signals for a second time period.
- 1 11. The apparatus of claim 1, the sample and hold unit to provide the at least two  
2 differential input signals based on a frequency of the oversampled clock signal.
- 1 12. The apparatus of claim 1, the counter to determine the count of rising and  
2 falling edges based on a time period of the oversampled clock signal.
- 1 13. The apparatus of claim 1, wherein the at least two differential input signals are  
2 Pulse Width Modulated (PWM) signals.
- 1 14. The apparatus of claim 13, wherein the PWM signals are to conform to the  
2 Mobile Industry Processor Interface (MIPI) M-PHY Specification.
- 1 15. A system comprising:  
2 a system on a chip comprising at least one core having at least one execution  
3 unit and receiver logic, the receiver logic comprising:  
4 a clock generator to generate an input clock signal;  
5 a pulse generator to generate an oversampled clock signal based on the input  
6 clock signal;  
7 a sample and hold unit to provide two or more differential input signals based  
8 on the oversampled clock signal;  
9 a conversion unit to generate a single-ended signal based on the two or more  
10 differential input signals;  
11 a counter to determine a count of rising and falling edges of the single-ended  
12 signal based on the oversampled clock signal; and

13 a wireless device coupled to the system on the chip via an interconnect, the  
14 interconnect used to communicate data between the wireless device and the  
15 receiver logic of the system on the chip.

1 16. The system of claim 15, the receiver logic further comprising a decision/data  
2 recovery unit to recover data based on the count of rising and falling edges.

1 17. The system of claim 16, the decision/data recovery unit comprising an elastic  
2 buffer synchronized to a processor clock signal.

1 18. The system of claim 15, the receiver logic further comprising an edge detector  
2 to detect the rising and falling edges of the single-ended signal.

1 19. The system of claim 15, the clock generator comprising a delay locked loop  
2 (DLL).

1 20. The system of claim 15, the clock generator comprising a phase locked loop  
2 (PLL).

1 21. The system of claim 15, the clock generator to generate the input clock signal  
2 based on a gear selection input and a reference clock signal.

1 22. The system of claim 15, the pulse generator to generate the oversampled  
2 clock signal based on rising edges and falling edges of the input clock signal.

1 23. A method comprising:  
2 generating, in a receiver logic of a first device, an oversampled clock signal  
3 based on an input clock signal;  
4 sampling and holding a plurality of differential input signals based on the  
5 oversampled clock signal;  
6 generating a single-ended signal based on the plurality of differential input  
7 signals; and

8           determining a count of rising and falling edges of the single-ended signal  
9 based on the oversampled clock signal.

1   24.   The method of claim 23, further comprising generating the input clock signal  
2 based on a gear selection input and a reference clock signal.

1   25.   The method of claim 23, further comprising recovering data based on the  
2 count of rising and falling edges of the single-ended signal.

1   26.   The method of claim 23, wherein generating the oversampled clock signal is  
2 based on rising edges and falling edges of the input clock signal.

1   27.   The method of claim 23, wherein the plurality of differential input signals are  
2 pulse width modulated (PWM) signals.

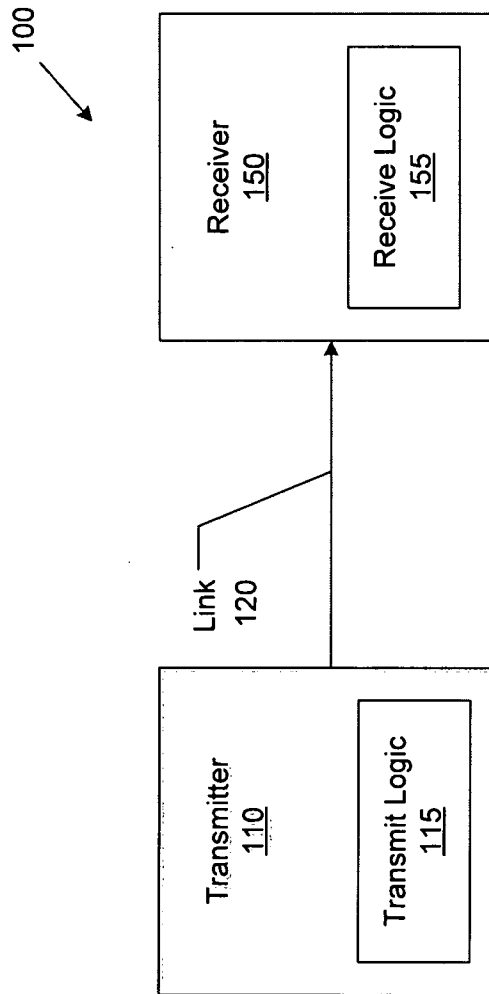


FIG. 1

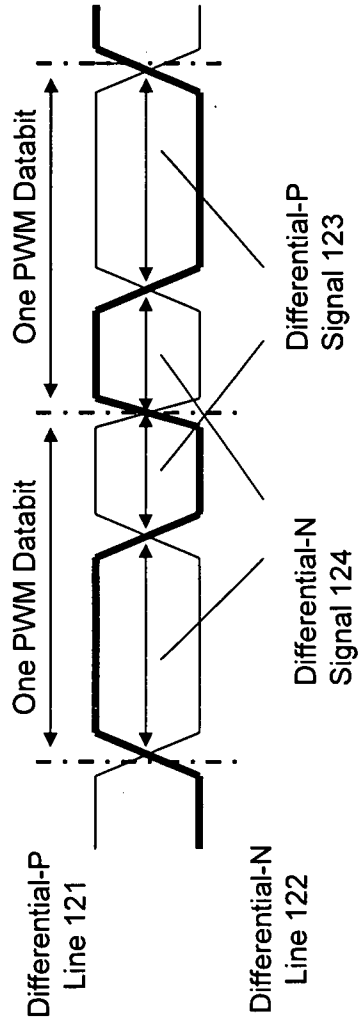


FIG. 2

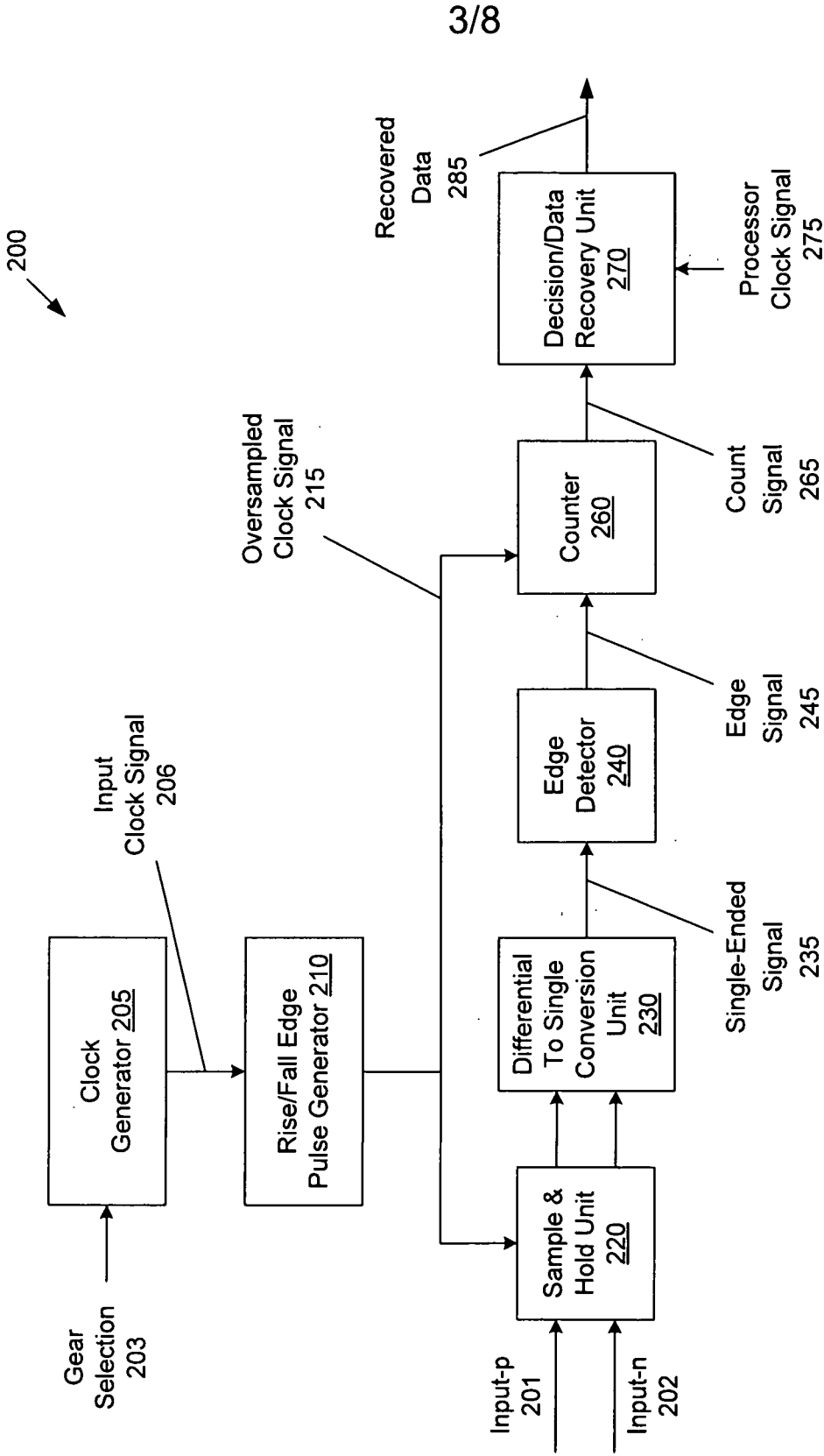


FIG. 3

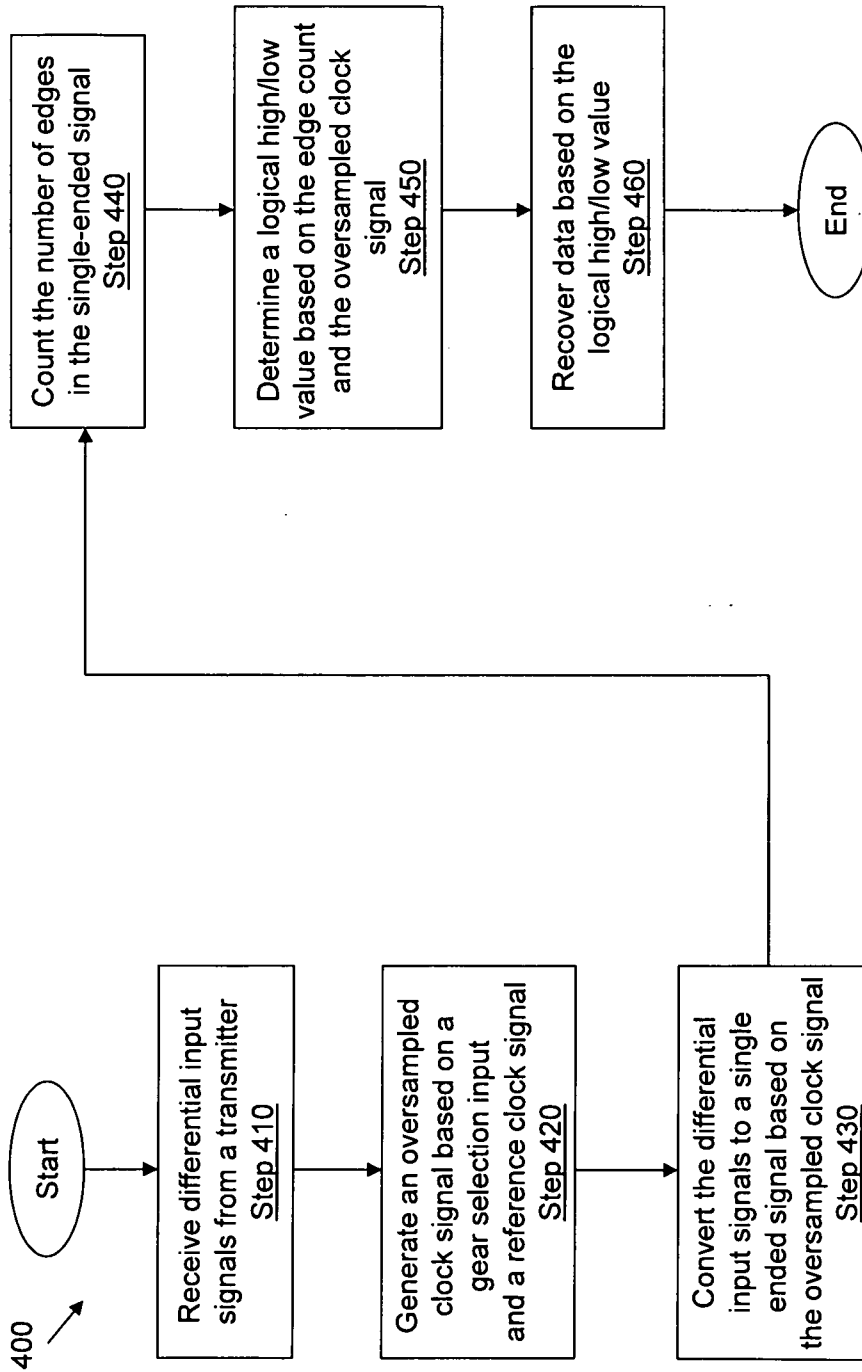


FIG. 4

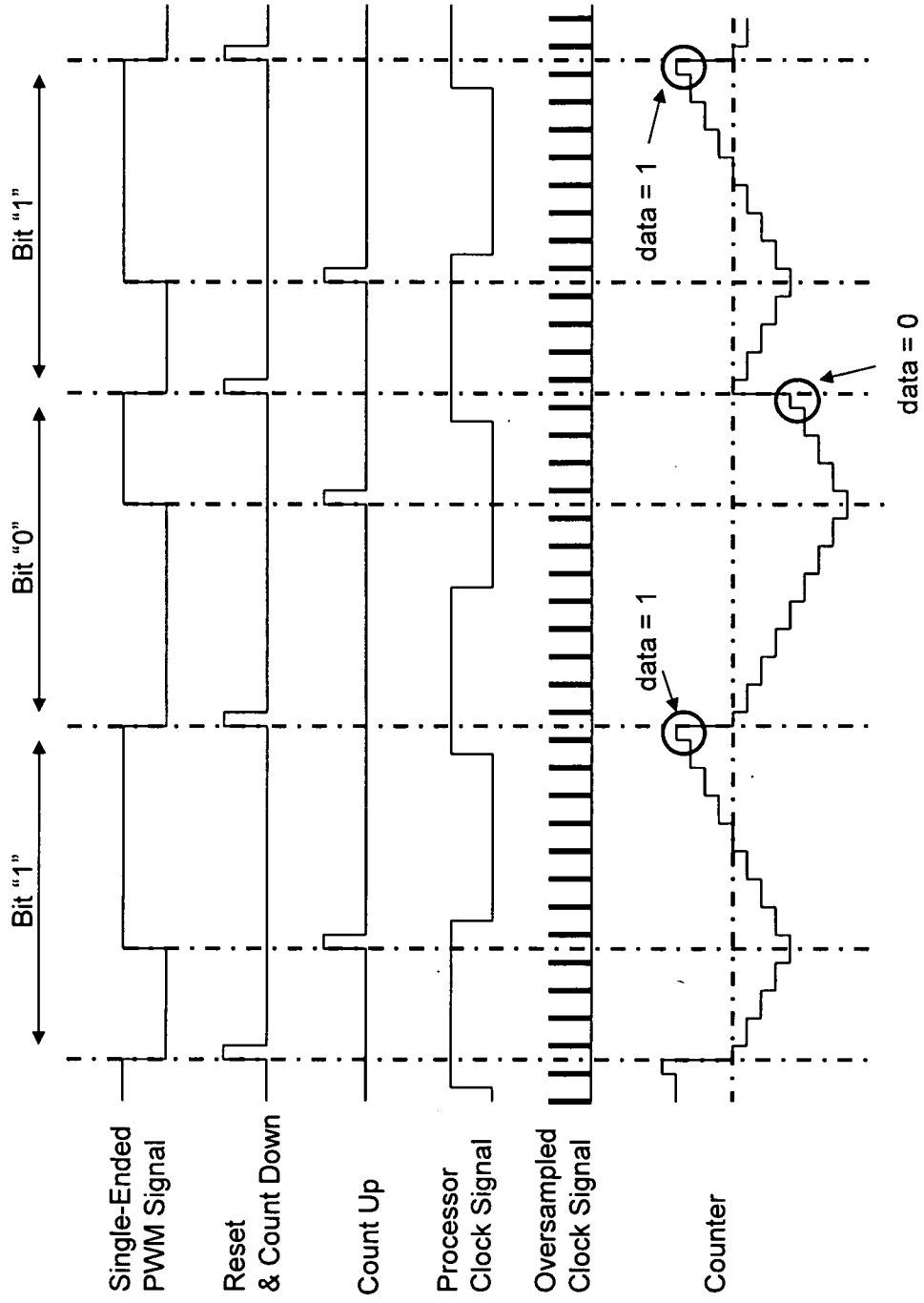


FIG. 5

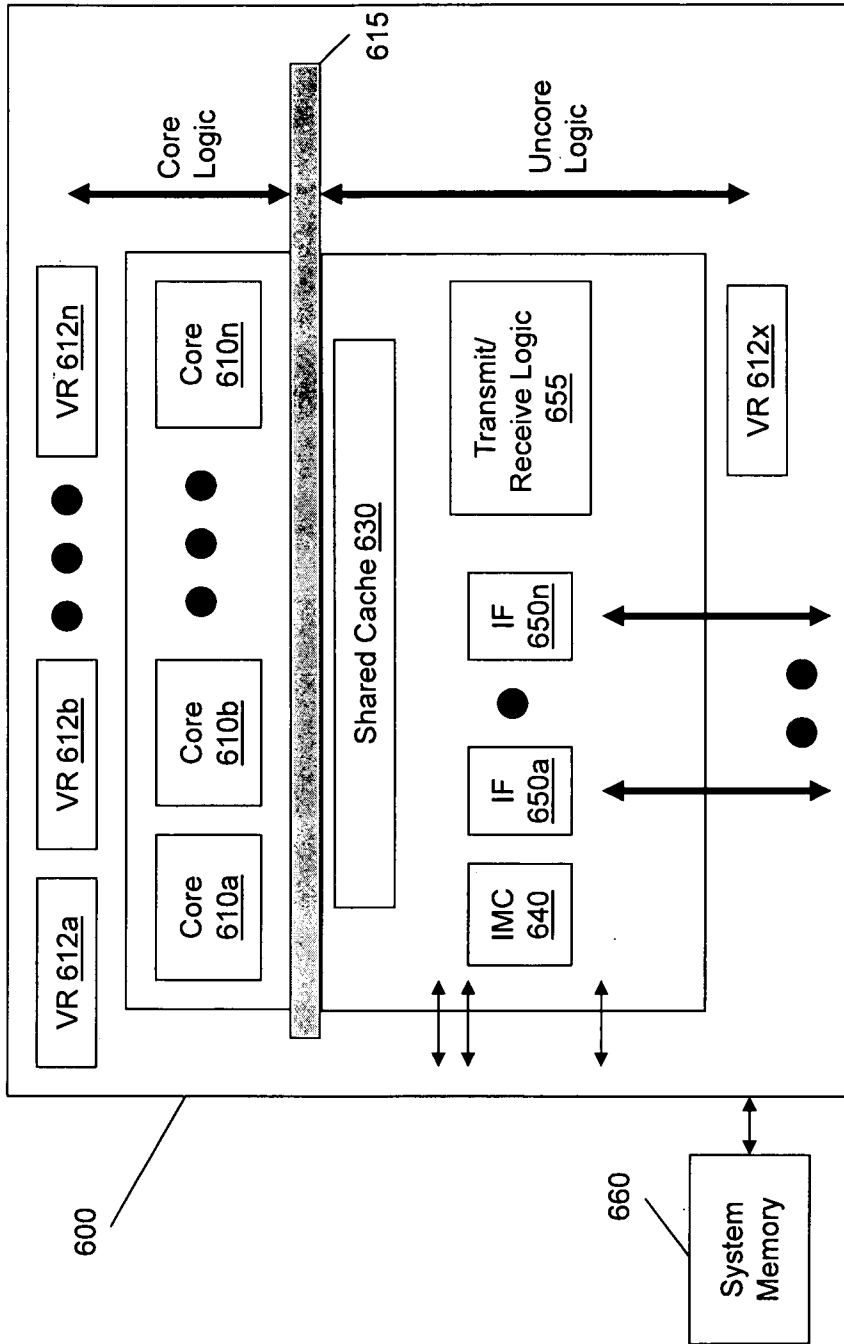


FIG. 6

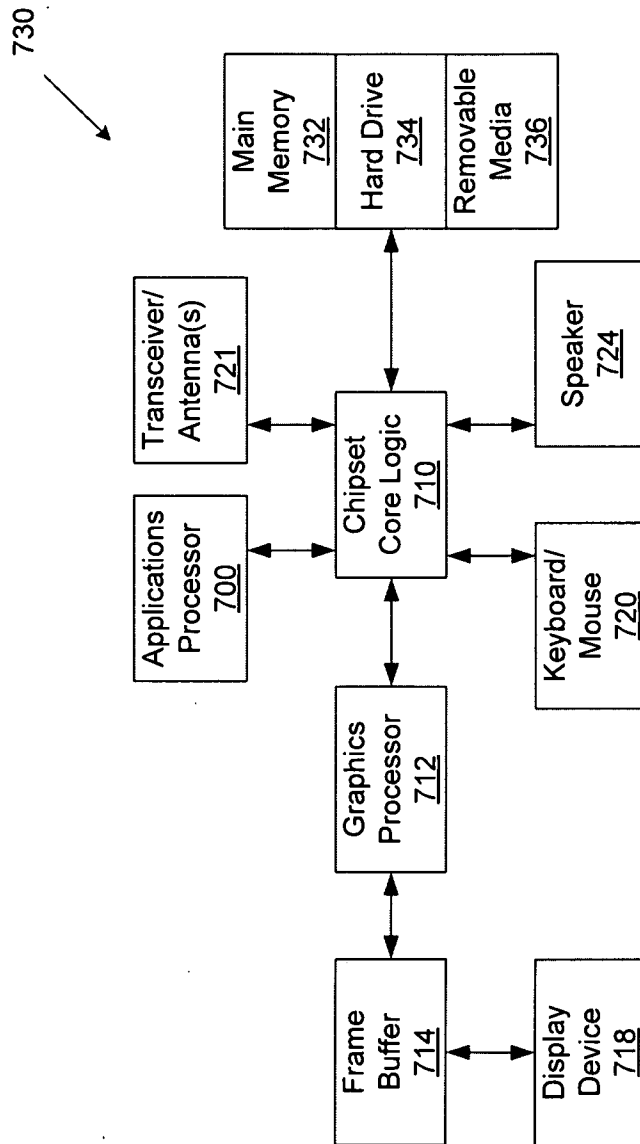


FIG. 7

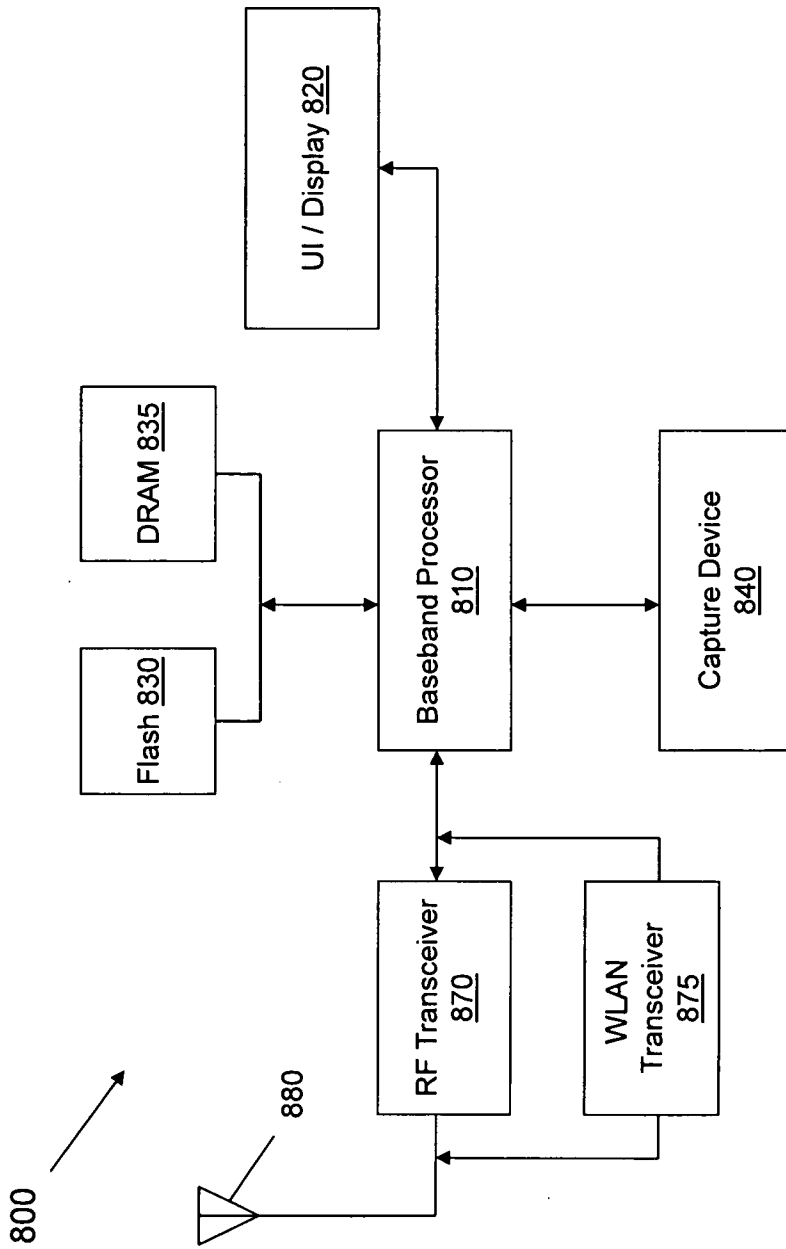


FIG. 8

**A. CLASSIFICATION OF SUBJECT MATTER****H04L 7/02(2006.01)i, H04L 25/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H04L 7/02; H04L 7/00; H03D 3/24; H03K 3/017; G06F 1/12; H04L 25/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: MIPI, MPHY, pluse, data, recovery, oversampled clock signal, counter, single-ended signal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004-0070436 A1 (MAKOTO KUDO et al.) 15 April 2004 See abstract, paragraphs [0035]-[0040], claims 1, 3, 5, and figures 2A-2B.	1-27
A	US 2008-0187080 A1 (TZUEN-HWAN LEE et al.) 07 August 2008 See abstract, paragraph [0027], claims 1, 8, and figure 7.	1-27
A	US 2006-0109942 A1 (VINCENT VALLET) 25 May 2006 See abstract, paragraphs [0025]-[0032], claims 1, 5, and figures 2-3.	1-27
A	US 2003-0190006 A1 (HIDEO NAGANO) 09 October 2003 See paragraphs [0011]-[0013], claims 1-2, and figure 1.	1-27
A	US 2006-0008040 A1 (VINCENT VALLET et al.) 12 January 2006 See paragraphs [0024]-[0029], claim 1, and figure 2.	1-27
A	US 6775345 B1 (HONGJIANG SONG) 10 August 2004 See abstract, column 4, lines 16-38, claims 1, 4, and figures 1-2.	1-27



Further documents are listed in the continuation of Box C.



See patent family annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family


Date of the actual completion of the international search

14 October 2013 (14.10.2013)

Date of mailing of the international search report

**16 October 2013 (16.10.2013)**

Name and mailing address of the ISA/KR


 Korean Intellectual Property Office  
 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City,  
 302-701, Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

CHOI Sang Won

Telephone No. +82-42-481-8291



**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.  
**PCT/US2013/046666**

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004-0070436 A1	15/04/2004	JP 2000-269816 A JP 3817958 B2 KR 10-0510333 B1 TW 469370 B US 6658583 B1 US 7017069 B2	29/09/2000 06/09/2006 25/08/2005 21/12/2001 02/12/2003 21/03/2006
US 2008-0187080 A1	07/08/2008	TW 200835178 A TW I342127 B US 7936855 B2	16/08/2008 11/05/2011 03/05/2011
US 2006-0109942 A1	25/05/2006	AT 421201 T DE 602004019040 D1 EP 1545046 A2 EP 1545046 A3 EP 1545046 B1 US 2008-0187079 A1 US 7406142 B2 US 7630467 B2	15/01/2009 05/03/2009 22/06/2005 22/11/2006 14/01/2009 07/08/2008 29/07/2008 08/12/2009
US 2003-0190006 A1	09/10/2003	JP 2003-304225 A	24/10/2003
US 2006-0008040 A1	12/01/2006	US 7474716 B2	06/01/2009
US 6775345 B1	10/08/2004	None	