(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 September 2006 (08.09.2006)

PCT

(10) International Publication Number
WO 2006/093460 A1

(51) International Patent Classification:
H04L 12/28 (2006.01) *H04L 7/00* (2006.01)

(21) International Application Number:
PCT/SE2006/000273

(22) International Filing Date: 2 March 2006 (02.03.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/657,406 2 March 2005 (02.03.2005) US

(71) Applicant *(for all designated States except US)*: **OMICRON CETI AB** [SE/SE]; Borgarfjordsgatan 7, S-164 40 Kista (SE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **WRIFE, Kenneth** [SE/SE]; Henrik Palmes Allé 18, S-182 69 Djursholm (SE).

(74) Agents: **ZACCO SWEDEN AB** et al.; Box 23101, S-104 35 Stockholm (SE).

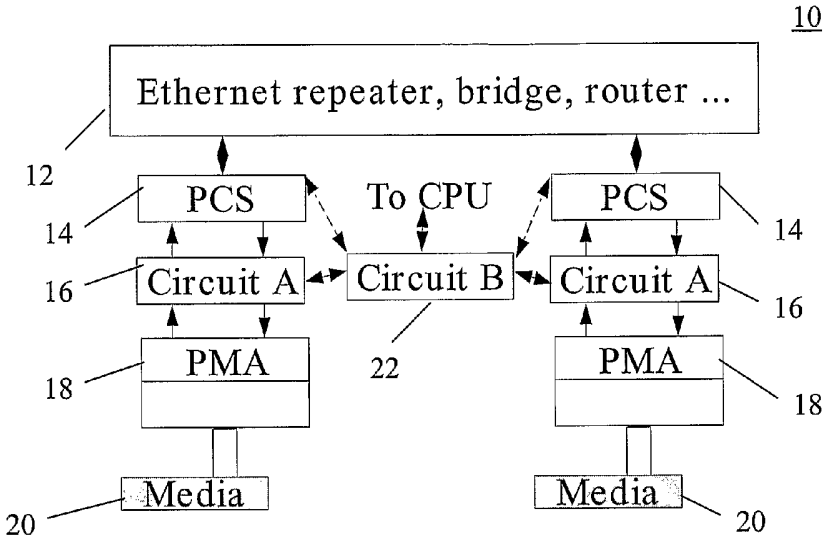
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** AN ACCURATE TIME DISTRIBUTION OVER ASYNCHRONOUS NETWORKS.



(57) **Abstract:** The invention relates to a system (10) and a method of adapting nodes (12) in an asynchronous Ethernet network to provide packages of at least one of data and telecommunication for accurate time distribution of messages, network synchronization and low latency messaging over asynchronous networks. Hence, it provides clock signal adaptin circuits (16) for every Ethernet connection to a node, each adapted to receive packages to the node, and to transmit packages from the node inserting delay, time and time critical real time information into a provided network protocol stack. Also introduced is a central circuit (22), a timer (23) connecting said clock signal adapting circuits with each other. Hereby, utilizing undefined codes (34) in packages sent in the network, by modifying the packages with the time information, thus the conventional traffic of packages, due to the utilization of undefined codes is affected to a minor degree.

WO 2006/093460 A1

Title

An accurate time distribution over asynchronous networks.

Technical field

The present invention pertains to a system and a method of adapting nodes in an asynchronous Ethernet, or Ethernet like network to provide packages of at least one of data and telecommunication for accurate time distribution of messages, network synchronization and low latency messaging over asynchronous networks.

Background art

There is a problem to transmit information in packets on an asynchronous network such as Ethernet or the like relating to time latency, i.e. the device that receives packages addressed to it has to wait until all packets have been received in order to perform for instance a control command or operation. Hence, a delay or latency is introduced for the intended control or operation.

Hence, it would be appreciated to solve problems related to time latency, delay time in asynchronous networks for transmission messages through packet technology.

Summary of the invention

An aim with the embodiments of the present invention is to synchronize information packets in an asynchronous network such as Ethernet in order to be able to control, regulate or the like, in real time applications. Such applications could be of an unlimited set of time demanding operations including for instance rocket launching, controlling robots, moving conveyer belts a minimum distance, emergency stops, alarm signals, determining positions of cellular phones in respect of base stations and an otherwise unlimited number of other applications that need to be time critically controlled.

Especially, the present invention is applicable in closed system networks, not necessarily limited to those, but to a person skilled in the art of networks such as Ethernet or the like.

The present invention thus sets forth an adapting system of nodes in an asynchronous Ethernet network to provide packages of at least one of data and telecommunication for accurate time distribution of messages, network synchronization and low latency messaging over asynchronous networks. The system thus comprises:

clock signal adapting circuits for every Ethernet connection to a node, providing delay information through a signal modifier, each adapted to receive packages to the node, and to transmit packages from the node inserting delay, time and time critical real time information into a provided network protocol stack utilizing undefined codes in packages sent in the network, by modifying the packages with the time information, thus the conventional traffic of packages, due to the utilization of undefined codes is affected to a minor degree;

a central circuit connecting the clock signal adapting circuits with each other, the central circuit distributing clock signals received from the circuit which receives packages and distributing clock signals to the circuit which transmits packages, and to other units in the node that rely on clock signals in order to provide the time information;

a physical medium attachment sub-layer standard in association with the clock signal adapting circuits, receiving and transmitting a data stream of packages to the node;

a physical coding sub-layer standard in association with the clock signal adapting circuits, forwarding a data stream of packages to and from the node; and

when the clock signal adapting circuit transmitting its downstream part reads incoming package data from the physical coding sub-layer to the physical medium attachment sub-layer, the clock signal adapting circuit checks if it is time to send a clock/time message, If not, the incoming data is written directly to the physical medium attachment sub-layer for transmission to a receiving node, and If a clock/time message should be sent incoming data is buffered in a buffer and the clock/time message is sent first to a receiving node.

In one embodiment of the present invention, if the buffer is getting overloaded, a wait signal is given to the physical coding sub-layer to halt transmission of packages, a release signal being given when to proceed with the transmission.

Another embodiment comprises the undefined codes utilized are codes in the 4B/5B and 8B/10B code set, inserted into the conventional bit stream.

A further embodiment comprises that the clock signal adapting circuit is connected directly to the physical code sub-layer and close to the node main device, when the sub-layer handles a transparent mode.

In a still further embodiment the clock signal adapting circuit is connected between the physical medium attachment sub-layer, and the physical code sub-layer, the physical code sub-layer being connected closest to the node main device.

Yet another embodiment comprises that the clock signal adapting circuit media delay time is calculated using a round trip calculation through the aid of a timer, whereby a time receiving clock signal adapting circuit receiving a time message from the central circuit, resending the message on the same Ethernet port as on which it was received, including internal delay information. The clock signal adapting circuit in the node connected to this port is setting a timer when the original message was sent, and when the returned message is received the timer is read and the media delay transmission time is calculated as round_trip_time / 2. Hereby, the time message transmission time is included in the next message of packages, as a separate part or as total delay time since the original origin of time. Thus the message sent includes the calculated delay to a receiving node.

A further embodiment comprises that the time message has the following structure:

<start>	Start of time message (an unused code)
<type>	Type of message, tells how to interpret the rest of the message
<delay>	Total delay since first node or delay in latest node.
<absolute>	Optional absolute time, sent from the origin
<end>	End of time message.

Set forth by the present invention is also an adaptation method of nodes in an asynchronous Ethernet network to provide packages of at least one of data and telecommunication for accurate time distribution of messages, network synchronization and low latency messaging over asynchronous networks. Thus it comprises:

connecting for every Ethernet connection to a node clock signal adapting circuits, providing delay information through a signal modifier,each adapted to receive packages to the node, and to transmit packages from the node inserting delay, time and time critical real time information into a provided network protocol stack utilizing undefined codes in packages sent in the network, by modifying the packages with the time information, thus the conventional traffic of packages, due to the utilization of undefined codes is affected to a minor degree;

connecting the clock signal adapting circuits, through a central circuit, with each other, the central circuit distributing clock signals received from the circuit which receives packages and distributing clock signals to the circuit which transmits packages, and to other units in the node that rely on clock signals in order to provide the time information;

associating a physical medium attachment sub-layer standard with the clock signal adapting circuits, receiving and transmitting a data stream of packages to the node;

associating a physical coding sub-layer standard with the clock signal adapting circuits, forwarding a data stream of packages to and from the node; and

when the clock signal adapting circuit transmitting its downstream part reads incoming package data from the physical coding sub-layer to the physical medium attachment sub-layer, the clock signal adapting circuit checks if it is time to send a clock/time message, If not, the incoming data is written directly to the physical medium attachment sub-layer for transmission to a receiving node, and If a clock/time message should be sent incoming data is buffered in a buffer and the clock/time message is sent first to a receiving node.

It is appreciated that the attached dependent method claims convey features described in context with the above system embodiments.

Brief description of the drawings

Henceforth reference is had to the attached drawings in the accompanying description for a better understanding of the present invention and its embodiments and given examples:

Fig. 1 schematically illustrates a special hardware device inserted in each node in a network distributing time/clock/real time messages with a very high accuracy in accordance with the present invention;

Fig. 2 schematically illustrates a device, which decides if a clock/time message should be sent, thus incoming data is buffered and the message is sent first in accordance with the present invention;

Fig. 3 schematically illustrates one embodiment of a message sent in accordance with the present invention;

Fig. 4 schematically illustrates an alternative embodiment to handle a transparent mode in accordance with the present invention; and

Fig. 5 schematically illustrates a message round trip calculation in accordance with the present invention.

Preferred embodiments of the invention

A circuit is built into nodes in an Ethernet, or Ethernet like network in accordance with the present invention. The device receives and transmits absolute time and delay information over asynchronous lines like Ethernet to a very high degree of accuracy, and inserts delay, time and other time critical real time information into a network protocol stack utilizing undefined codes in package messages. By this conventional traffic is affected to a very low degree. Moreover the time adapting system of the present invention distributes time/clock/real time messages on for instance an Ethernet 802.x based network with a very high accuracy. Delay time of each node is controlled and the result is a synchronized network. The system can also be used for very accurate absolute time distribution and other type of synchronous messaging

In accordance with the present invention a specific hardware circuit/device is inserted in each schematically depicted node 10, Fig. 1, in a network sending packages of messages/information. A node 10 might be constituted by a repeater, a dual and multi-port bridge, a router, a computer or any other device 12 that has an IEEE 802.x interface. This is depicted in Fig. 1, where the reference numeral 12 schematically shows the actual node device.

The device in each node, consist of a number of parts. For each Ethernet connection an inter connection circuit A 16, functioning as a clock signal adapting circuit, is inserted into the data stream between the IEEE 802 PCS, Physical Coding Sub-layer, 14 and the IEEE 802 PMA, Physical Medium Attachment sub-layer 18 in accordance with the present invention. In specific designs the Circuit A 16 is actually inserted between the PCS

14 and a connection/port to the main node device 12 utilizing a transparent PCS mode, if available. This is depicted in Fig. 4, and further elaborated below.

Every main node device 12 has multiple connections/ports for receiving and transmitting messages of packages in an Ethernet like network, which in Fig. 1 is depicted with two connections/ports, the two ports in Fig. 1 having similar features 14, 16, 18 for receiving and transmitting packages in different directions in the network, where the clock signal adapting circuit A 16 is inserted in accordance with the present invention.

A central circuit B 22, in accordance with the present invention, connects the circuits A 16, for the depicted two ports in Fig. 1, with each other. The circuit B 22 distributes clock signals received from one of the connection/port circuits A 16 circuit, named Ar (Areceiving), when acting as such, and distributes the signal to the other transmitting units called At (Atransmitting), when acting as such, and to other units in the node being dependent on accurate clock signals, like a CPU (not shown). The central circuit B 22 keeps track of/monitors delays and modifies signals, through a signal modifier 26 so that transmitted time signals include delay information.

Moreover, the central circuit B 22 is equipped with a timer 23, utilized for instance to calculate round trip time as further described below and depicted in Fig. 5.

The media 20 box of Fig. 1 schematically depicts any device receiving or transmitting information in a network of the present invention.

The interconnection clock signal adapting circuit A 16, as schematically depicted in Fig. 2, is inserted into the data-stream between PCS and the PMA sub-layer 14, 16, having two parts, an upstream part and a downstream part for receiving/transmitting packages of media 20 information, which is depicted by the arrows in Fig. 2.

If the circuit A 16 currently is of the At type the downstream part reads incoming 4B/5B or 8B/10B data from the PCS to the PMA 16, 18. It checks if it is time to send a clock/time message. If not, the incoming data is written directly to the PMA 18 for transmission. If a clock/time message should be sent incoming data is buffered and the message is sent first. The buffer 24 should be large enough to hold a number of times the size of the clock/timer message. If the buffer is getting full or overloaded, a wait signal is given to the PCS sub-layer 14. The central circuit B 22 receives timing information from the circuit A 16 modifier 26, which is passed on to other ports and timing dependent devices.

The conceptions, PMA, PCS and 4B/5B or 8B/10B data utilized throughout the present description are defined in the IEEE standard 802.3-2000:

> PMA Physical Medium Attachement Is the service layer that connects to the physical media. Input to this layer is either 5B or 10B coded. See 802.3-2000 1.4.212 and clause 36 and 40)

PCS Physical Coding Sub-layer: The PCS contains the functions to encode data bits into code-groups that can be transmitted over the physical medium. See 802.3-2000 1.4.210 and clause 36 and 40 in the standard.

4B/5B and 8B/10B coding is a way to translate a 4 bit word into a 5 bit word (8 bits into 10 bits). The conversion is described in 802.3-2000 Table 24-1 and Table 36-1d in the standard

See IEEE 802.3 Clauses 36 and 40.

The message sent as schematically depicted in Fig. 3, utilizes some of the undefined codes in the 4B/5B and 8B/10B code set to transmit timing information. This is inserted into the conventional bit stream 30, and in the embodiment shown in Fig. 3 a 4B/5B conversion is accomplished and the bit stream resembles the one shown as 32 in Fig. 3. Hence, the 4B/5B conversion 32 comprises undefined unused 5B codes, which can be utilized to transmit timing information to adapt time delay and latency in an asynchronous network throughout other nodes and internally in nodes 10.

It is appreciated if there is accomplished a 4B/5B coding, without making any changes an 8B/10B coding can be utilized, i.e., 5B can be replaced by 8B, and 5B can be replaced by 10B in accordance with the present invention.

As an alternative embodiment of the present invention, Fig. 4 schematically illustrates that the connection/insertion of the clock signal adapting circuit A 16 can be accomplished directly to the PCS 40 transparent mode. The transparent mode is utilized when the interface between PCS 40 and PMA 16 is not externally available. This may be the case when PCS and PMA is designed into the same electronic chip. In this case the PCS 40 circuit may be set into transparent mode and the 4B/5B or 8B/10B coding or decoding may be accomplished in the modifier circuit 26 itself.

A media delay time as schematically depicted in Fig. 5, is calculated through for instance the aid of the timer 23 in circuit B 22, using a round trip calculation 50. When a time receiving circuit At 16 receives a time message it also resends this message on the same Ethernet port as on which it was received, internal delay information included. The circuit A 16 in the node connected to this port sets a timer to when the original message was sent. When the returned message is received the timer is read and the media 20 delay transmission time is calculated as round_trip_time / 2. The media 20 transmission time is included in the next message, as a separate part or as total delay time since the original origin of time. Thus the message sent includes the calculated delay to the receiver.

Message structure:

<start>	Start of time message (an unsed code)
<type>	Type of message, tells how to interpret rest of message *
<delay>	Total delay since first node or delay in latest node.*,**
<absolute>	Optional absolute time, sent from the origin *,***
<end>	End of time message

Explanations to the message structure

*) Type, delay, absolute time are coded using a number of unsued codes in the /H/ code-group in the IEEE 802 standard. Binary coding is used where one 5 or ten bit code represent one binary number. E.g. 00011 represent the binay number 010 (2) and 10000 represent 100 (4). To represent a larger number the message contains several codes. E.g to sen the binary number 100010 (decimal 34) the code groups 10000 00011 are sent

**) The number indicates delay in a time unit like micro-, nano or pico-seconds.

***) The number indicates time in a time unit like micro-, nano or pico-seconds since a starting point in time like 2004-00-00, 00:00.0.

The following is in the scope of the present invention; a circuit for insertion of delay and time messages into a network link; a design of a device for bridging (switching) network traffic; a utilization of unused codes in the 4B5B or 8B10B code stream, for synchronous information and high priority messages; a media transmission time calculated utilizing a loop-back; a delay already set in messages transmitted; an internal delay in device circuits inserted into transmitted message; a synchronous transmission of high priority or isochrone real time messages; an un-effected or low impact of transmission of standard protocols; a variable size of messages; a special set of codes defining the delay in the node itself; a special set of codes defining the total delay since a transmission of the original time message; a code for start of clock/time/information messages; a code for end of transmission of messages; a set of codes defining the absolute time; the system and method of the present invention, utilizing a loop-back function to calculate the media 20 delay and the like.

The present invention attached set of claims conveys further embodiments to a person skilled in the art then those specifically exemplified in the present description.

Claims:

1. An adapting system (10) of nodes in an asynchronous Ethernet like network to provide packages of at least one of data and telecommunication for accurate time distribution of messages, network synchronization and low latency messaging over asynchronous networks, **characterized** in that it comprises:

clock signal adapting circuits (16) in each node (12), providing delay information through a signal modifier (26), each circuit (16) adapted to receive packages to said node (12), and to transmit packages from said node inserting delay, time and time critical real time information through said modifier (26) into a provided network protocol stack utilizing undefined codes (34) in packages sent in the network, by modifying said packages with said time information, thus the conventional traffic of packages, due to the utilization of undefined codes (34) is affected to a minor degree;

a central circuit (22), connecting said clock signal adapting circuits with each other, said central circuit (22) distributing clock signals received from the circuit (16) which receives packages and distributing clock signals to the circuit (16) which transmits packages, and to other units in the node that rely on clock signals in order to provide said time information;

a physical medium attachment sub-layer (18) standard in association with said clock signal adapting circuits (16), receiving and transmitting a data stream of packages to said node (12);

a physical coding sub-layer (14) standard in association with said clock signal adapting circuits (16), forwarding a data stream of packages to and from said node (12); and

when said clock signal adapting circuit (16) transmitting its downstream part, reads incoming package data from the physical coding sub-layer (14) to said physical medium attachment sub-layer (18), said clock signal adapting circuit (16) checks if it is time to send a clock/time message, If not, the incoming data is written directly to the physical medium attachment sub-layer (18) for transmission to a receiving node, and If a clock/time message should be sent incoming data is buffered in a buffer (24) and the clock/time message is firstly sent to a receiving node (12).

2. An adapting system according to claim 1, wherein said buffer is getting overloaded, a wait signal is given to the physical coding sub-layer to halt transmission of packages, a release signal being given when to proceed with said transmission.

3. An adapting system according to claim 1, wherein said undefined codes utilized are codes in the 4B/5B and 8B/10B code set, inserted into the conventional bit stream.

4. An adapting system according to claim 1, wherein said clock signal adapting circuit is connected directly to the physical code sub-layer and close to the node main device, when the sub-layer handles a transparent mode.

5. An adapting system according to claim 1, wherein said clock signal adapting circuit is connected between said physical medium attachment sub-layer, and said physical code sub-layer, said physical code sub-layer being connected closest to the node main device.

6. An adapting system according to claim 1, wherein said clock signal adapting circuit media delay time is calculated using a round trip calculation through the aid of a timer (23), whereby a time receiving clock signal adapting circuit receiving a time message from said central circuit, resending said message on the same Ethernet port as on which it was received, including internal delay information, said clock signal adapting circuit in the node connected to this port setting a timer when the original message was sent, and when the returned message is received the timer is read and the media delay transmission time is calculated as round_trip_time / 2, said time message transmission time being included in the next message of packages, as a separate part or as total delay time since the original origin of time, thus the message sent includes the calculated delay to a receiving node.

7. An adapting system according to claim 6, wherein said time message has the following structure:

<start>	Start of time message (an unsed code)
<type>	Type of message, tells how to interpret the rest of the message
<delay>	Total delay since first node or delay in latest node.
<absolute>	Optional absolute time, sent from the origin
<end>	End of time message.

8. An adaptation method of nodes in an asynchronous Ethernet like network to provide packages of at least one of data and telecommunication for accurate time distribution of messages, network synchronization and low latency messaging over asynchronous networks, **characterized** in that it comprises:

connecting for every Ethernet connection to a node (12) clock signal adapting circuits (16) in each node (12), providing delay information through a signal modifier (26), each circuit (16) adapted to receive packages to said node (12), and to transmit packages from said node (12) inserting delay, time and time critical real time information into a provided network protocol stack utilizing undefined codes (34) in packages sent in the network, by modifying said packages with said time information, thus the conventional traffic of packages, due to the utilization of undefined codes (34) is affected to a minor degree;

connecting said clock signal adapting circuits (16), through a central circuit (22), with each other, said central circuit (22) distributing clock signals received from the circuit (16) which receives packages and distributing clock signals to the circuit which transmits packages (16), and to other units in the node that rely on clock signals in order to provide said time information;

associating a physical medium attachment sub-layer (18) standard with said clock signal adapting circuits (16), receiving and transmitting a data stream of packages to said node;

associating a physical coding sub-layer (14) standard with said clock signal adapting circuits (16), forwarding a data stream of packages to and from said node (12); and

when said clock signal adapting circuit (16) transmitting its downstream part, reads incoming package data from the physical coding sub-layer (14) to said physical medium attachment sub-layer (18), said clock signal adapting circuit (16) checks if it is time to send a clock/time message, If not, the incoming data is written directly to the physical medium attachment sub-layer (18) for transmission to a receiving node, and If a clock/time message should be sent, incoming data is buffered in a buffer (24) and the clock/time message is firstly sent to a receiving node.

9. An adapting method according to claim 8, wherein said buffer is getting overloaded, a wait signal is given to the physical coding sub-layer to halt transmission of packages, a release signal being given when to proceed with said transmission.

10. An adapting method according to claim 8, wherein said undefined codes utilized are codes in the 4B/5B and 8B/10B code set, inserted into the conventional bit stream.

11. An adapting method according to claim 8, wherein said clock signal adapting circuit is connected directly to the physical code sub-layer and close to the node main device, when the sub-layer handles a transparent mode.

12. An adapting method according to claim 8, wherein said clock signal adapting circuit is connected between said physical medium attachment sub-layer, and said physical code sub-layer, said physical code sub-layer being connected closest to the node main device.

13. An adapting method according to claim 8, wherein said clock signal adapting circuit media delay time is calculated using a round trip calculation through the aid of a timer (23), whereby a time receiving clock signal adapting circuit receiving a time message from said central circuit, resending said message on the same Ethernet port as on which it was received, including internal delay information, said clock signal adapting circuit in the node connected to this port setting a timer when the original message was sent, and when the returned message is received the timer is read and the media delay transmission

time is calculated as round_trip_time / 2, said time message transmission time being included in the next message of packages, as a separate part or as total delay time since the original origin of time, thus the message sent includes the calculated delay to a receiving node.

14. An adapting method according to claim 13, wherein said time message has the following structure:

<start>	Start of time message (an unused code)
<type>	Type of message, tells how to interpret the rest of the message
<delay>	Total delay since first node or delay in latest node.
<absolute>	Optional absolute time, sent from the origin
<end>	End of time message.

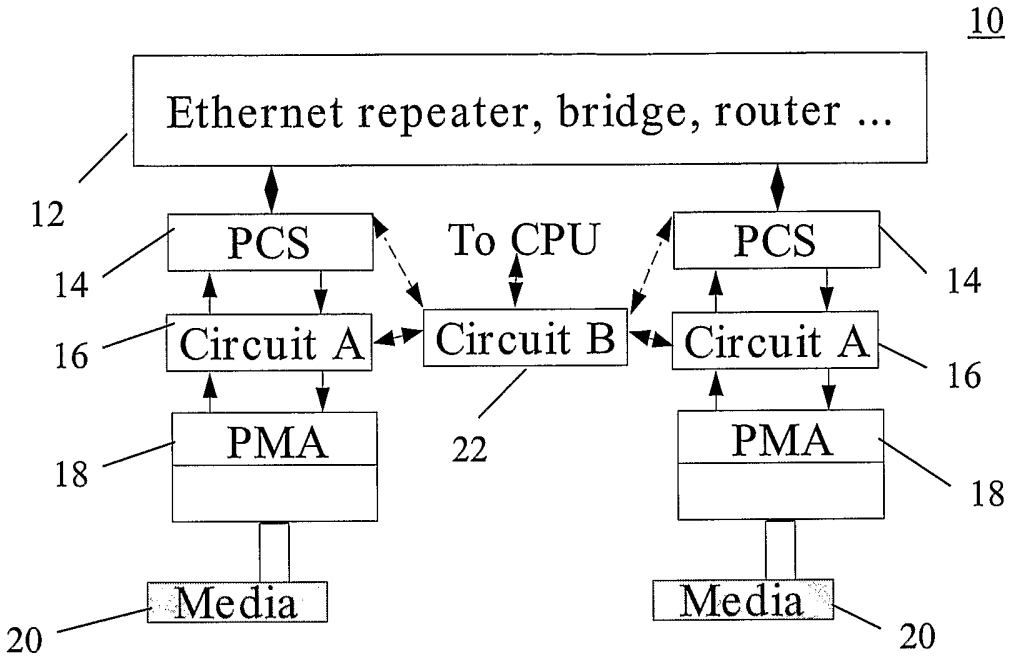

10
Ethernet repeater, bridge, router ...
12
PCS
To CPU
PCS
14
14
16
Circuit A
Circuit B
Circuit A
16
22
PMA
PMA
18
18
Media
Media
20
20

Fig. 1

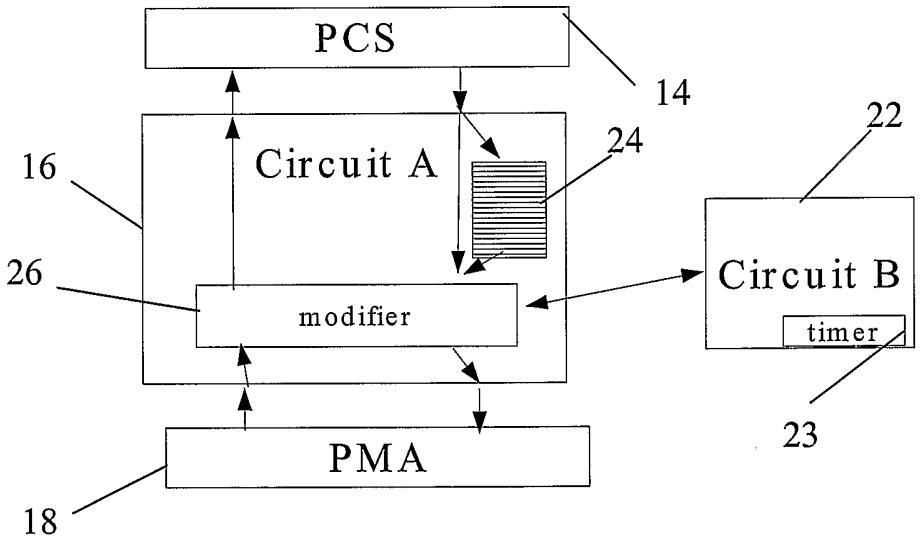

PCS
14
22
16
Circuit A
24
26
modifier
Circuit B
timer
23
PMA
18

Fig. 2

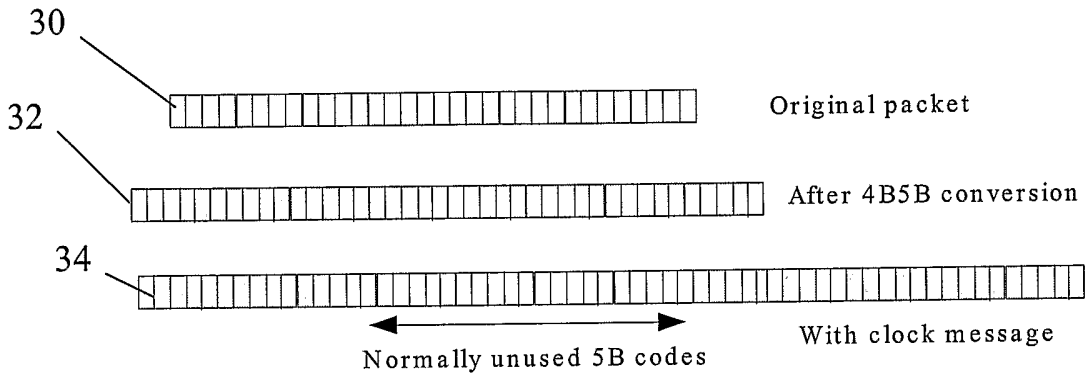


Fig. 3

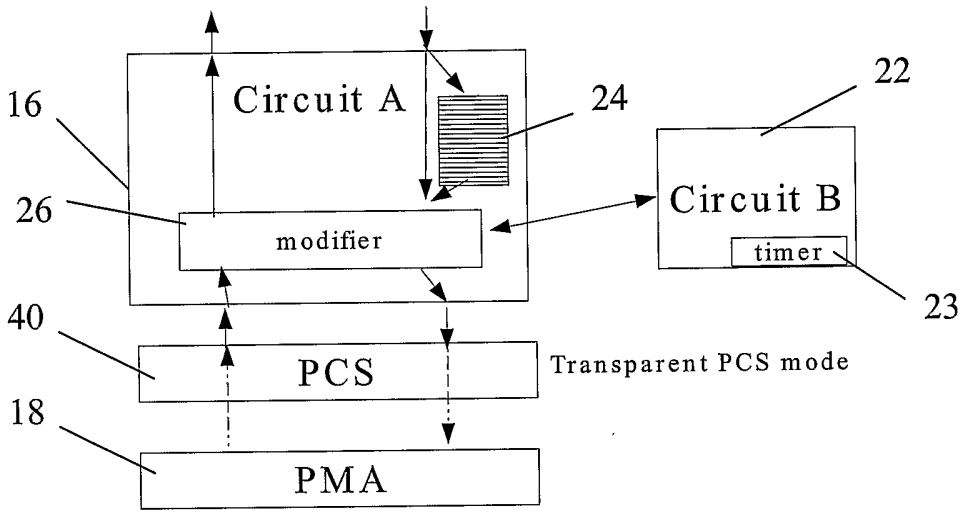


Fig. 4

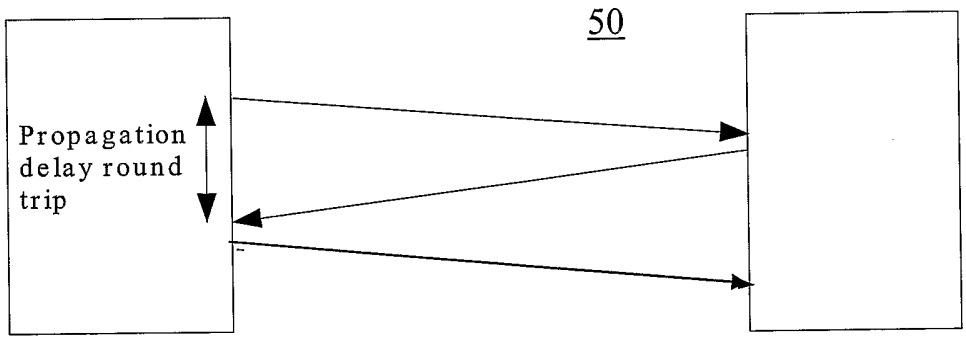


Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE2006/000273

A. CLASSIFICATION OF SUBJECT MATTER

IPC: see extra sheet
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1122931 A2 (SHARP KABUSHIKI KAISHA), 8 August 2001 (08.08.2001), paragraph [0044], abstract ---	1-14
A	WO 0120825 A1 (VOCALTEC COMMUNICATIONS LTD), 22 March 2001 (22.03.2001), page 2, line 22 - page 3, line 5, abstract ---	1-14
A	US 20030137997 A1 (KEATING), 24 July 2003 (24.07.2003), figure 1, abstract --- --------	1-14

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 June 2006	04 -07- 2006
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Ralf Boström/EK Telephone No. +46 8 782 25 00

International patent classification (IPC)
H04L 12/28 (2006.01)
H04L 7/00 (2006.01)

Download your patent documents at www.prv.se
The cited patent documents can be downloaded at www.prv.se by following the links:

- In English/Searches and advisory services/Cited documents (service in English) or
- e-tjänster/anförda dokument(service in Swedish).

Use the application number as username.
The password is **KMKIVPJJLF**.

Paper copies can be ordered at a cost of 50 SEK per copy from PRV InterPat (telephone number 08-782 28 85).

Cited literature, if any, will be enclosed in paper form.

EP	1122931	A2	08/08/2001	DE	60118269 D	00/00/0000
				JP	2001251360 A	14/09/2001
				US	6778493 B	17/08/2004
WO	0120825	A1	22/03/2001	AU	7310000 A	17/04/2001
				EP	1212859 A	12/06/2002
				IL	148682 D	00/00/0000
				US	6445681 B	03/09/2002
US	20030137997	A1	24/07/2003	NONE		