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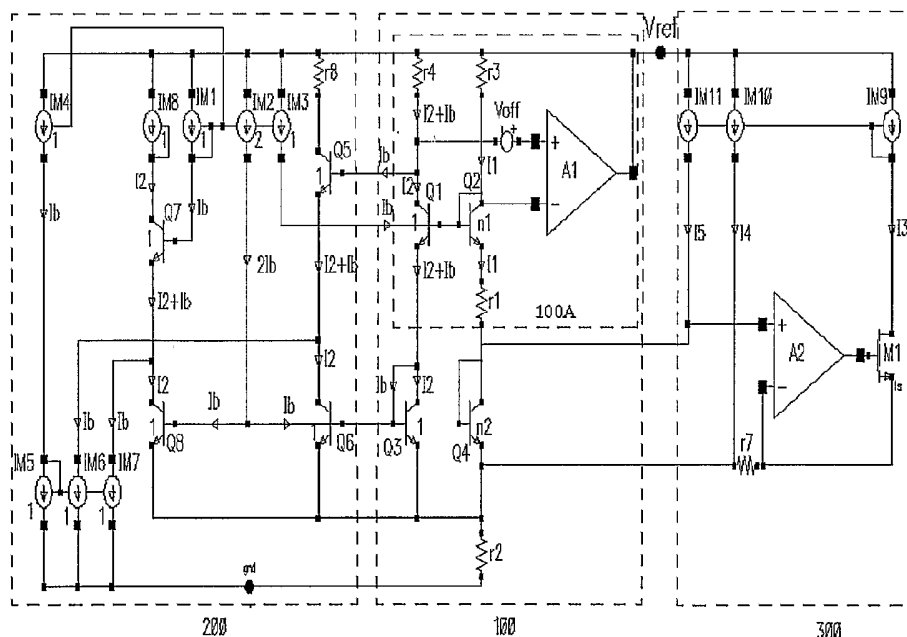
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(54) Title: IMPROVED BANDGAP VOLTAGE REFERENCE



(57) Abstract: A bandgap voltage reference is described which has reduced sensitivity to noise and amplifier offset. By configuring the circuitry such that the base width of the component transistors is not varied on application of a bias, it is possible to obviate the Early effect.

WO 2005/057313 A1

Improved bandgap voltage reference

Field of the Invention

The present invention relates to voltage reference circuits and in particular to a voltage reference circuit implemented using bandgap techniques. More particularly the present invention relates to a method and circuit that provide a voltage reference with very low temperature coefficient (TC) and reduced sensitivity to amplifier noise and offset.

10 Background Of The Invention

A bandgap voltage reference circuit is based on addition of two voltages having equal and opposite temperature coefficient. The first voltage is a base-emitter voltage of a forward biased bipolar transistor. This voltage has a negative TC of about $-2.2\text{mV}/\text{C}$ and is usually denoted as a Complementary to Absolute Temperature or CTAT voltage. The second voltage which is Proportional to Absolute Temperature, or a PTAT voltage, is formed by amplifying the voltage difference (ΔV_{be}) of two forward biased base emitter junctions of bipolar transistors operating at different current densities. These type of circuits are well known and further details of their operation is given in Chapter 4 of "Analysis and Design of Analog Integrated Circuits", 4th Edition by Gray et al, the contents of which are incorporated herein by reference.

A classical configuration of such a voltage reference circuit is known as a "Brokaw Cell", an example of which is shown in Figure 1. First and second transistors Q1, Q2 have their respective collectors coupled to the non-inverting

and inverting inputs of an amplifier A1. The bases of each transistor are commonly coupled, and this common node is coupled via a resistor, r5, to the output of the amplifier. This common node of the coupled bases and resistor r5 is coupled via another resistor, r6, to ground. The emitter of Q2 is coupled via a resistor, r1, to a common node with the emitter of transistor Q1. This common node is then coupled via a second resistor, r2, to ground. A feedback loop from the output node of A1 is provided via a resistor, r3, to the collector of Q2, and via a resistor r4 to the collector of Q1.

10 In Fig.1, the transistor Q2 is provided with a larger emitter area relative to that of transistor Q1 and as such, the two bipolar transistors Q1 and Q2 operate at different current densities. Across resistor r1 a voltage, ΔV_{be} , is developed of the form:

$$15 \quad \Delta V_{be} = \frac{KT}{q} \ln(n) \quad (1)$$

where

k is the Boltzmann constant,

q is the charge on the electron,

T is the operating temperature in Kelvin,

20 n is the collector current density ratio of the two bipolar transistors.

Usually the two resistors r3 and r4 are equal and the collector current density ratio is given by the ratio of emitter area of Q2 to Q1. In order to reduce the reference voltage variation due to the process variation Q2 may be provided as an array of n transistors, each transistor being of the same area as Q1.

The voltage ΔV_{be} generates a current, I_1 , which is also a PTAT current.

The voltage of the common base node of Q1 and Q2 will be:

$$V_b = 2 \Delta V_{be} * \frac{r_2}{r_1} + V_{be1} \quad (2)$$

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By properly scaling the resistor's ratio and current density the voltage "Vb" is temperature insensitive by the first order, and apart from the curvature which is effected by the base-emitter voltage can be considered as remaining compensated. The voltage "Vb" is scaled to the amplifier's output as a reference voltage, V_{ref} , by the ratio of r_5 to r_6 :

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$$V_{ref} = (2 \Delta V_{be} * \frac{r_2}{r_1} + V_{be1}) (1 + \frac{r_5}{r_6}) + (I_b(Q_1) + I_b(Q_2)) r_5 \quad (3)$$

Here $I_b(Q_1)$ and $I_b(Q_2)$ are the base currents of Q1 and Q2.

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Although a "Brokaw Cell" is widely used, it still has some drawbacks. The second term in equation 3 represents the error due to the base currents. In order to reduce this error r_5 has to be as low as possible. As r_5 is reduced, the current extracted from supply voltage via reference voltage increases and this is a drawback. Another drawback is related to the fact that as operating temperature changes the collector-base voltage of the two transistors also changes. As a result of the Early effect (the effect on transistor operation of varying the effective base width due to the application of bias), the currents into the two transistors are affected. Further information on the Early effect may be found on page 15 of the aforementioned 4th Edition of the Analysis and Design

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of Analog Integrated Circuits, the content of which is incorporated herein by reference.

If the second order effects in the circuit of Figure 1 are neglected the amplifier's input offset voltage V_{off} is reflected into the reference voltage node as:

$$V_{ref-off} = V_{off} * \frac{r2}{r4} (1 + \frac{r5}{r6}) \quad (4)$$

The amplifier's noise is also reflected from input to reference node with the same gain:

$$G = \frac{r2}{r4} (1 + \frac{r5}{r6}) \quad (5)$$

From equation 4 and Figure 1 it is clear that the easy way to reduce offset and noise sensitivity in "Brokaw Cell" is to make $r4$ larger compared to $r2$. But as $r4$ is larger, the collector-base voltages of Q1 and Q2 are also larger and Early effect is exaggerated.

The "Brokaw Cell" also suffers, in the same way as all uncompensated reference voltages do, in that it is affected by "curvature" of base-emitter voltage.

The base-emitter voltage of a bipolar transistor, used as a CTAT voltage in bandgap voltage references, and as biased by a PTAT collector current is temperature related as equation 6 shows :

$$V_{be}(T) = V_{G0} \left(1 - \frac{T}{T_0} \right) + V_{be0} \frac{T}{T_0} - (\sigma - 1) \frac{kT}{q} \ln \left(\frac{T}{T_0} \right) \quad (6)$$

where:

$V_{be}(T)$ is the temperature dependence of the base-emitter voltage for the bipolar transistor at operating temperature,

5 V_{BE0} is the base-emitter voltage for the bipolar transistor at a reference temperature,

V_{G0} is the bandgap voltage or base-emitter voltage at 0K temperature,

T_0 is the reference temperature,

σ is the saturation current temperature exponent (sometimes referred as
10 XTI in the computer added simulators).

The PTAT voltage developed across r_2 in Figure 1 only compensates for the first two terms in equation 6. The last term, which provides the "curvature" of the order of about 2.5mV for the industrial temperature range (-40C to 85C)
15 remains uncompensated and this is gained into the reference voltage by the gain factor G (equation 5).

As the "Brokaw Cell" is well balanced, it is not easy to compensate internally for the "curvature" error. One attempt to compensate this error is
20 presented in US patent No. 5,352,973 co-assigned to the assignee of the present invention, the disclosure of which is incorporated herein by way of reference. In this US patent, although the "curvature" error is compensated, in this methodology by use of a separate circuit which biases an extra bipolar transistor with constant current, it does require the use of an additional circuit.

Other known examples of band gap reference circuits include those described in US 4,399, 398 assigned to the RCA Corporation which describes a voltage reference circuit with feedback which is adapted to control the current flowing between first and second output terminals in response to the reference potential departing from a predetermined value. This circuit is a simple implementation that achieves a reduction of the Early effect. The circuit serves to reduce the base current effect, but at the cost of high power. As a result, this circuit is only suited for relatively high current applications. This can be traced to the fact that the compensation for the base current is effected by operating transistor T1 at a higher current than transistor T2, and as the power is increased the dissipation across RS is also increased. Also, it will be appreciated from an examination of the circuitry that the power supply rejection achieved is relatively modest.

It will be appreciated therefore that although the circuitry described in Figure 1 has very low offset and noise sensitivity, there is still a need to provide for further reduction in sensitivity to offset and noise.

Summary Of The Invention

Accordingly, a first embodiment of the invention provides an improved voltage reference circuit adapted to overcome these and other disadvantages of the prior art. The invention provides a bandgap reference circuit which by scaling the voltage difference between two transistors operating at different current densities can provide at an output of an amplifier a voltage reference. The circuit of the present invention is further adapted to reduce voltage differences between the collector-bases regions of the two transistors thereby minimising the Early effect.

In accordance with a preferred embodiment, a bandgap reference voltage circuit including a first amplifier having a first and second input and providing a voltage reference at the output thereof is provided. The amplifier is coupled at
5 its first input to a first transistor and at the second input to a second transistor, the second transistor having an emitter area larger than that of the first transistor. The second transistor is coupled at its emitter to a load resistor, the load resistor providing, in use, a measure of the difference in base emitter voltages between the first and second transistors, ΔV_{be} , for use in the
10 formation of the bandgap reference voltage. In accordance with the invention, the bases of each transistor are commonly coupled such that the base of the first and second transistor is at the same potential, one of the first and second transistors is provided in a diode connected configuration, and the base collector voltage of the other of the first and second transistors is maintained at
15 zero by the amplifier which is coupled in a feedback loop to the collector of each of the transistors, thereby reducing the Early effect.

The circuit desirably further includes a third and fourth transistor, the third transistor being coupled to the emitter of the first transistor and the fourth
20 transistor being coupled via the load resistor to the emitter of the second transistor, the emitter area of the fourth transistor being greater than that of the first or third transistor, such that the first and third transistors operate at a higher current density than the second and fourth transistors and wherein a PTAT voltage is provided via a resistor, in the feedback loop, at the second
25 input to the amplifier such that the voltage provided at the output of the amplifier is a combination of the base emitter voltages of the first and third transistors plus the PTAT voltage.

Each of the third and fourth transistors are desirably provided in a diode connected configuration. The emitter of the third transistor is preferably coupled via a second resistor to ground, the value of the resistor effecting a shifting of
5 the reference voltage from twice the natural bandgap voltage to a desired voltage, thereby enabling an offset adjustment to the circuit.

A third and fourth resistor are typically provided in each of the feedback loop paths between the output of the amplifier and the collectors of the first and
10 second transistors respectively.

The resistors provided in each of the feedback loops are either substantially the same value, or may be chosen to be of different values.

15 The circuit may additionally include circuitry adapted to provide the base current for the non-diode connected transistor and to extract that same current from the collector of the same transistor, thereby maintaining the collector current of each of the first and second transistors at the same value.

20 Such circuitry may be adapted to compensate for base current variation between the non-diode connected transistor and the other transistor, thereby reducing errors in the circuit due to the base current.

Typically, the non-diode connected transistor is the first transistor and the
25 circuitry adapted to extract the current from the collector of the first transistor includes a replication of the leg of the circuit defined by the first and third transistors, the replicated leg including a fifth and sixth transistor of the circuit,

the base of the fifth transistor being coupled to the collector of the first transistor, the emitter of the fifth transistor being coupled to the collector of the sixth transistor, the base of the sixth transistor being coupled to the diode connected base of the third transistor thereby providing a current mirror, such
5 that a base current is extracted from the collector of the first transistor by the fifth transistor.

The base current of the first and second transistors may be further mirrored via seventh and eight transistors and a bipolar mirror, the base
10 currents of the sixth and eight transistors being supplied by a double current mirror from the output of the amplifier such that the collector currents of each of the third, sixth and eight transistors are the same.

The collector of the fifth transistor is typically coupled via a resistor to the
15 output of the amplifier, the value of the resistor being substantially equivalent to that of the fourth resistor such that the base current of the fifth transistor tracks the base current of the first transistor.

The base current of the first and second transistors may be further
20 mirrored via a series of mirrors coupled to the fifth and seventh transistors such that the mirrored current may be extracted from the emitters of the fifth and seventh transistors thereby ensuring that the collector currents of the fifth and seventh transistors are substantially the same value, this current being further mirrored via a current mirror coupled between the collector of the seventh
25 transistor and the output of the amplifier, thereby providing a PTAT current.

Certain embodiments may further include circuitry adapted to provide a correction voltage adapted to compensate for the curvature of the voltage of the first and third transistors, the incorporation of the correction voltage effecting a cancelling of the curvature.

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Such circuitry is typically adapted to provide a mixture of PTAT and CTAT voltages at the load resistor.

The correction voltage is typically provided by mirroring the base-emitter
10 voltage of the fourth transistor across a resistor and effecting the generation of a complimentary to absolute temperature (CTAT) current using a MOSFET device and amplifier, the CTAT current being provided back into the fourth transistor via at least one current mirror thereby replicating across the load resistor a voltage having an inverse curvature, the combination of this
15 replicated voltage and the previously present voltage (ΔV_{be}) effecting a cancellation of the curvature.

The size of the voltage having an inverse curvature may be modified by changing the slope of the current provided by the current mirror and fourth
20 transistor.

Modifications to the circuit of the invention may include a plurality of additional transistors coupled to the third and fourth transistors, the plurality of additional transistors being provided in a stack arrangement, thereby enabling a
25 use of the reference circuit with higher reference voltages.

The invention also provides a method of providing a bandgap reference voltage circuit adapted to compensate for the Early effect, the method comprising the steps of:

5 providing first and second transistors, each transistor adapted to operate at different current densities, the first transistor being provided in a diode connected configuration, the transistors being additionally coupled to the inputs of an amplifier,

10 scaling the voltage difference between two transistors operating at different current densities so as to provide a reference voltage at an output of the amplifier,

15 providing a feedback loop, the feedback loop coupling each of the first and second transistors to the output of the amplifier so as to provide at an output of an amplifier a voltage reference, such that the collector base voltage of each of the first and second transistors is reduced to zero.

Brief Description Of The Drawings

The present invention will now be described with reference to the accompanying drawings in which:

20 Figure 1 is an example of a typical "Brokaw" cell in accordance with the prior art;

Figure 2 is an example of a circuit according to a preferred embodiment of the present invention;

Figure 3 is a simulation of the performance of a circuit in accordance with the prior art;

25 Figure 4 is a simulation of the currents through the output divider (r5, r6) and their difference (base currents) for the circuit of Figure1;

Figure 5 is a simulation of the reference voltage in accordance with the circuit of Figure 2;

Figure 6 is a simulation of the base current (Q1), the correction base current (Q5) and their difference in accordance with the circuit of Figure 2;

5 Figure 7 is a simulation of the base current, the compensation base current and their difference for the circuit of Figure 2;

Figure 8 highlights how the offset voltage influence the collector currents of Q1 and Q2 into the circuit of Figure 2;

Figure 9 is modification to the circuit of claim 1 including additional
10 transistors provided in a stack arrangement;

Figure 10 is a simulation of the performance of the circuit of Figure 9.

Detailed Description Of The Drawings

15 The prior art has been described with reference to Figure 1.

Figure 2 is an example of a bandgap voltage reference in accordance with the present invention. The circuit of Figure 2 may be sub-divided into three blocks: a main reference block 100; a bias current compensation block 200,
20 and a curvature correction block 300, each block adapted to obviate specific problems associated with the prior art. As was detailed in the section "background to the invention" there are a number of problems associated with the prior art implementations of the classic Brokaw cell. These can be summarised as problems due to the Early effect, sensitivity due to base
25 current, sensitivity due to offsets, power requirements arising from the coupling of the output from the voltage reference output across one or more resistors

and the fact that there is no possibility to internally correct for curvature. The configuration shown in Figure 2 is adapted to overcome these and other problems and the solution to each of the problems can be traced to specific components or functionality within the circuit.

5

As can be seen from Figure 2, this circuit is based on generating a voltage reference using bandgap techniques. As is known, by using the scaled difference between two transistors operating at different current densities it is possible to combine these at an amplifier and provide a voltage reference at that amplifier output. In accordance with the circuit of the present invention, the main block 100 includes an amplifier A1 which has an inverting and non-inverting input. A first transistor Q1 is provided with a first emitter area and a second transistor Q2 is provided with a second emitter area, n_1 times that of Q1. Q2 is provided in a diode connected configuration such that the collector is tied to the base. In accordance with standard operation, the amplifier A1 keeps its two inputs at substantially the same voltage level and as a result Q1 also operates at zero base-collector voltage. The bases of both Q1 and Q2 are coupled at the same potential, in a similar fashion to that described in Figure 1. However, in accordance with the present invention the output of the amplifier is provided in a feedback configuration to the common base of Q1 and Q2 and to the collectors of Q1 and Q2. Desirably this feedback is provided such that the collector of Q2 is coupled via a resistor r_3 and the collector of Q1 via a resistor r_4 . It can be seen that Q1 and Q2 have zero collector-base voltages, Q1 being a diode connected transistor and Q2 has also zero collector-base voltage due to the amplifier A1 and therefore the "Early" effect is eliminated. This set of circuitry is shown within the dashed block 100A of Figure 2. It will be appreciated that although the arrangement within block 100A illustrates the

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base-collector voltage of Q1 being controlled by the amplifier and that of the Q2 by virtue of the diode connection arrangement, that equivalently Q1 may be diode connected and Q2 controlled by the amplifier. It will be further appreciated that, if the base current can be neglected, such as in the case of applications having high β , that no additional circuitry is required to compensate for the base current.

The emitters of each of transistors Q1 and Q2 are typically coupled to the collectors of two further transistors Q3 and Q4 respectively, also diode connected. In the case of Q1, this is a direct connection whereas with Q2 it is via a resistor r1. Q3 is provided with the same emitter area as Q1 and Q4 has an emitter area of "n2" times larger that of Q1 and Q3. Q1 and Q3 therefore operate at a higher current density as compared to Q2 and Q4 and across r1, a ΔV_{be} voltage, which is a PTAT voltage, is developed. This results in a PTAT current flowing from the amplifier's output through Q1 to Q3 and Q2 to Q4 via r1. The common emitter of Q3 and Q6 are connected to the ground node via a resistor r2. This resistor has a role of shifting the reference voltage from twice the natural bandgap voltage ($\sim 2.3V$), for $r2=0$, to a desired value, for example a typical 2.5V.

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The bias current compensation block, 200, has the role of supplying the base current for Q1, I_b , and for extracting the same current from its collector. If this is the case, the currents passing r1 and r3 are substantially the same and they are not affected by the base currents. The current passing r4 is the same current as the emitter current of Q1. As a result the voltage drop over r3 and r4 is a scaled replica of ΔV_{be} voltage. The circuitry of this block is useful in applications having low or moderate β , where the contribution of the base

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current may introduce errors, and is specifically provided to reduce these errors. It will be appreciated that although r_1 and r_3 are typically chosen to have the same values, that they could for certain applications be specifically chosen to have different values. The advantage of using the bias current compensation
5 block is that the base currents will be compensated by the subtraction and subsequent re-introduction of a base current into the main block 100, regardless of the value of the chosen r_1 and r_3 .

The base current I_b is extracted from collector of Q1 by mirroring the
10 current I_2 via Q5 and Q6. These transistors form an equivalent leg to that provided by Q1 and Q3. As Q3 in the block 100 and Q6 in the block 200 have the same base-emitter voltage, their collector currents will be substantially the same, I_2 . The base current, I_b , is also mirrored via Q8, Q7 and a typical bipolar mirror IM1, usually a bipolar pnp diode connected transistor. The base currents
15 of Q8 and Q6 ($2I_b$) are supplied back via a double current mirror IM2. In this way Q3, Q6 and Q8 will have exactly the same collector currents as they operate at the same base current. In order to minimise the base current difference from Q1 to Q5 an extra resistor r_8 is provided, with substantially the same value as r_4 , thereby ensuring that Q1 and Q5 operate in similar
20 conditions, having the same collector current and substantially zero base-collector voltage. As a result the base current of Q5 will track the base current of Q1. Due to the similarities between the two legs provided by Q1/Q3 and Q5/Q6, the tracking performance of the base current achieved is very accurate.

25 The base current, I_b , is also mirrored from the current mirror IM4 to a "master" mirror IM5, usually a bipolar npn diode connected transistor. This current is extracted via mirrors IM5 and IM7 from the emitters of Q5 and Q7 to

ensure that the collector currents of Q5 and Q7 are substantially the same current as the collector of Q3, which is I_2 . The PTAT current I_2 is mirrored via a "master" mirror IM8 connected between the reference voltage and the collector of Q7. In this way the cell according to Fig.2 can also generate a PTAT current.

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It will be further appreciated from an examination of the components of the circuitry of the block 200, that one set of circuitry is used to pull the base current and another set of circuitry is used to generate and provide the base current back into block 100. By using two different sets of circuit components it is possible to more accurately extract the base current. This is because this extraction circuitry has no additional functionality, specifically that associated with the generation of the base current to be re-introduced. The second set of circuitry has the specific purpose of re-provide that base current. The first set of components, that extracting the base current, is provided by the replicated leg, that leg having Q5 and Q6. The other components generate a base current that may be fed back to the coupled bases of Q1 and Q2.

Although the extraction and re-introduction of the base current to the block 100 could be achieved using a simpler configuration wherein the circuitry used to extract the base current from the collector of Q1 had the additional functionality of re-providing that base current to the base of Q1 and Q2, such circuitry would not achieve the accuracy of extraction that is possible using the arrangement described above.

25 The second order effect, or "curvature" of a typical bandgap voltage is compensated via the block 300. The circuitry of the block 300 is adapted to develop a negative "curvature" voltage in a manner similar to that described in

co-pending and co-assigned US application Serial Number 10/375,359 filed on 27 February 2003, the content of which is incorporated herein by way of reference. The "curvature" correction is performed by mirroring the base-emitter voltage of Q4 across a resistor, r7, and by generating a CTAT current via MOSFET device M1, and current mirrors IM9 and IM11. The CTAT current is fed back into the diode-connected transistor Q4 in order to exaggerate its curvature and thereby replicating across r1 a negative voltage "curvature". This negative voltage "curvature" depends by the slope of the collector current of Q4, and is gained by the ratio r3/r1 to compensate for the positive voltage "curvature" of Q3 and Q1.

The current passing r2 is a combination of PTAT currents, flowing from Q3, Q4, Q6, Q8, and CTAT currents flowing from r7 and IM11. An extra CTAT current, I4, generated from a current mirror IM10 ensures that the voltage drop over r2 is the required shifting voltage and the reference voltage is the desired compensated reference voltage. It will be understood that the slope of the CTAT current generated can be varied by choice of current mirror IM11 and transistor Q4. The CTAT current and the PTAT current already across the load resistor r1 are then gained by the choice of the ratio of the load resistor r1 to the feedback resistor r3.

If we consider that the emitter areas of Q2 and Q4 are identical then $n_1=n_2=n$ and $r_3=r_4$, then the PTAT voltage, ΔV_{be} , is:

$$\Delta V_{be} = 2 \frac{KT}{q} \ln(n) \quad (7)$$

The reference voltage V_{ref} is:

$$V_{ref} = V_{shift} + V_{be,Q3} + V_{be,Q1} + I_1 * r_3 = V_{shift} + 2(V_{be1} + \Delta V_{be} \frac{r_3}{r_1}) \quad (8)$$

where V_{shift} is a combination of PTAT and CTAT voltages:

$$V_{shift} = (4I_1 + I_3 + I_4 + I_5)r_2 \quad (9)$$

Here V_{be1} is the base-emitter voltage of Q1 and Q3.

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In order to see the amplifier's offset voltage influence into the reference voltage let us consider that the base currents are neglected, $r_3=r_4$, $n_1=n_2=n$, and the amplifier A has a input offset voltage V_{off} as Figure 2 shows. If the offset voltage is zero the two currents, I_1 and I_2 , are balanced.

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For a given offset voltage, V_{off} , the currents become unbalanced as equation 10 shows:

$$I_1 r_3 = I_2 r_3 + V_{off} \quad (10)$$

As equation 10 shows, for a positive offset voltage $I_1 > I_2$. As the current I_2 into the high current density side (Q1, Q3) decreases and the current I_1 into the low current density side (Q2, Q4) increases ΔV_{be} decreases. This tends to decrease the current I_1 and this inherent negative feedback play the role of rebalance the voltage drop over r_3 which is the main PTAT voltage. For a negative offset voltage $I_1 < I_2$, ΔV_{be} increases and PTAT voltage decreases.

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In order to see the improvements from the circuit according to Figure 1 to the circuit according to Figure 2, two appropriate circuits were simulated.

Into the simulated circuit according to Figure 1 the resistors values are:
r1=20k; r2=56.5k; r3=r4=100k; r5=10.1k; r5=10k. Q1 is a unity 5x5 microns
emitter transistor. Q2 is an area of 50 unity transistors of the same emitter area.
The collector currents I1 and I2 are PTAT currents of about 5 uA at room
5 temperature. The simulated reference voltage is presented in Figure 3. The
reference voltage variation is about 3mV for the temperature range from -40C
to 85C. This corresponds to a TC of about 10ppm/C.

Figure 4 shows the currents through the gain resistors (r5, r6) and their
10 difference, being the sum of two base currents. The current difference can be
considered as an error because the factor "beta", or the ratio of the collector
current to the base current has a large spread due to the process variation. As
is seen this error current develop across r5=10k a error voltage of about 1.6mV.

15 In order to quantify the type of improvement that is possible using the
circuitry and methodology of the present invention, a circuit according to Figure
2 was designed and simulated. In this exemplary simulated circuit, the resistors
values are: r1=30k; r2=5k; r3=r4=r8=190k; r7=142k. Q1, Q3, Q5, Q6, Q7, Q8
are unity area bipolar transistors; Q2 and Q4 are each on an area of 25 parallel
20 unity area bipolar transistors. From the area point of view the two circuits
(Figure 1 and Figure 2) are comparable as the total number of unity bipolar
transistors are close: Q2 in Fig.1 is 50 units, Q2 and Q4 in Fig.2 are each 25
units. The current passing r3, Q2, r1 and Q4 is a PTAT current of about 5uA at
room temperature, the same as it was for the circuit according to Figure1. Also,
25 the amplifiers are the same in both circuits.

A simulated reference voltage according to Figure 2 is presented in Figure 5. The total voltage variation according to Figure 4 is about 40uV, for the same temperature range, -40C to 85C. This correspond to a TC of about 0.15ppm/C and this is a reduction of TC of $10/0.15=68$.

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If the slope of the voltage reference into the circuit of Figure 2 is compensated by fine tuning remains only the residual voltage curvature and this is displayed in Figure 6. As Fig.5 shows the residual "curvature " voltage corresponds to a TC of about 0.025ppm/C.

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Figure 7 shows how the base currents of Q1 and Q5 track each other. As we can see these currents are about 63nA at room temperature and their difference is less than 30pA for the entire temperature range. The voltage drop of this current across r4 in Figure 2 is less than 6uV compared to 1.6mV voltage error due to the base current into the circuit of Figure 1.

15

The amplifier input offset voltage influence into the reference voltage was simulated for both circuits. For the circuit according to Figure 1, 1mV offset voltage into the amplifier's input is reflected as 1.88mV error into the reference voltage. For the circuit according to Figure 2, a 1mV offset voltage is reflected as 0.57mV. This corresponds to a reduction of more than three times in offset and noise sensitivity from the circuit of Figure 1 to the circuit of Figure 2.

20

Figure 8 highlights how the offset voltage influence the collector currents of Q1 and Q2 into the circuit of Figure 2. The first diagram shows the alteration of the collector currents of Q1 and Q3 due to a offset voltage of 1mV. The lower diagram shows the alteration of collector currents of Q2 and Q4 for the same

25

offset voltage. As it seen the offset voltage is reflected mainly into the high density current side (Q1 and Q3) and this is due to the inherent feedback against offset voltage which was mentioned before.

5 The offset voltage of the second amplifier A2 in Figure 2 has very low influence into the reference voltage. 1mV offset voltage for A2 translates as an error of less than 30uV into the reference voltage of the circuit according to Figure 2.

10 The reference voltage according to Figure 2 can be adapted for a higher reference voltage value by stacking more bipolar transistors. One such example aimed to generate a 5V reference voltage is presented in Figure 9. Figure 9 is very similar to that of Figure 2 with the only difference being the addition of components to the main reference block 100 and the subsequent
15 changing of the coupling arrangement between the main reference block 100 and the other two blocks 200, 300.

In Figure 9 additional transistors Q9, Q10, Q11 and Q12 are provided in a stack arrangement coupled to the transistors Q3 and Q4. All four of the new
20 transistors are provided in a diode connection configuration with the collector of Q9 being coupled to the emitter of Q3, the collector of Q10 being coupled to the emitter of Q9. Similarly, the collector of Q11 is coupled to the emitter of Q4, the collector of Q12 being coupled to the emitter of Q10. Q11 and Q12 are provided between the resistor r2 and the transistor Q4. The coupling of the first
25 block 100 to the third block 300 is provided through the common node of Q11 and Q12, and Q12 and r2. In a similar fashion, the coupling of the block 100 to the block 200 is effected through connections coupled to the common node of

Q10, Q12 and r2. The effect of the stacking of the transistors is to enable operation of the circuit at higher voltages as will be appreciated by those skilled in the art. As such the number of transistors shown is for exemplary purposes only and any number of stacked transistors of varying properties could
5 equivalently be used.

Figure 9 also shows an alternative way in which the curvature can be corrected. In this embodiment, the amplifier and MOSFET arrangement that was present in the equivalent block 300 of Figure 2 is replaced by a transistor
10 qn17 and resistor r9 arrangement. The base of qn17 is coupled to the emitter of Q4, the collector to current source IM9 and the emitter to resistor r9. The second terminal of r9 is coupled to the emitter of Q12. The curvature correction is provided in a similar fashion to that described earlier. The base-emitter voltage of Q4 is coupled via Q12 across resistor, r9, and a CTAT current is
15 generated using current mirrors IM9 and IM11. The CTAT current is fed back into the diode-connected transistor Q11 in order to exaggerate its curvature and thereby replicating across r1 a negative voltage "curvature". This arrangement is possible due to the greater number of stacked transistors available in the embodiment of Figure 9 and it will be appreciated that any number of different
20 schema may be used to provide the block functionality of the curvature correction block 300, and that although two exemplary embodiments have been illustrated in Figures 9 and 2, that these are illustrative of the type that may be used with the other blocks of the present invention and as such modifications may be made without departing from the spirit and scope of the present
25 invention.

A circuit according to Figure 9 was simulated, the simulation results being shown in Figure 10. For this circuit the resistors values are: $r_1=30k$, $r_2=5k$, $r_3=r_4=r_8=200k$, $r_7=60k$; the bipolar transistors Q1, Q3, Q5, Q7, Q8, Q9, Q10 are unity emitter area of $5\mu\times 5\mu$ each; the bipolar transistors Q2, Q4, Q11 and Q12 are each an area of 12 unity emitter area of $5\mu\times 5\mu$. A MONTE CARLO analysis of 1000 iteration at 25C temperature were performed for the circuit according to Figure 9 to see the reference voltage spread due to process variation. As Figure 10 shows, the parameter " σ " in the distribution is 1.25mV in 5V reference voltage. For 3σ , the deviation in reference voltage is about 0.075%.

The bandgap voltage reference in accordance with the circuit of the present invention is also advantageous in that it generates the inherently PTAT and CTAT currents required if extra trimming is to be performed.

It will be understood that the present invention has been described with reference to specific NPN configurations of bipolar transistors and that it is not intended that the application of the invention be limited to such configurations. As will be understood by the person skilled in the art many modifications and variations in configurations may be achieved by implementation in PNP architectures or the like. It will be appreciated that what has been described herein is an exemplary embodiment of a bandgap voltage reference in accordance with the present invention. Specific components, features and values have been used to describe the circuit in detail, but it is not intended that the present invention be limited in any way whatsoever except as may be deemed necessary in the light of the appended claims. It will be further appreciated that some of the components of the present invention have been

described using their conventional symbols and the actual functional description of how for example an amplifier is constructed has been omitted. Such functionality will be well known to the person skilled in the art and where additional details is required, it will be understood that it can be found in any
5 number of standard text books.

Similarly, the words comprises/comprising when used in this specification are to specify the presence of stated features, integers, steps or components but does not preclude the presence or addition of one or more other features,
10 integers , steps, components or groups thereof.

Claims

1. A bandgap reference voltage circuit including a first amplifier having a first and second input and providing a voltage reference at the output thereof, the amplifier being coupled at its first input to a first transistor and at the second input to a second transistor, the second transistor having an emitter area larger than that of the first transistor, and wherein:

the second transistor is coupled at its emitter to a load resistor, the load resistor providing, in use, a measure of the difference in base emitter voltages between the first and second transistors, ΔV_{be} , for use in the formation of the bandgap reference voltage,

the bases of each transistor are commonly coupled such that the base of the first and second transistor is at the same potential,

one of the first and second transistors is provided in a diode connected configuration,

the base collector voltage of the other of the first and second transistors is maintained at zero by the amplifier which is coupled in a feedback loop to the collector of each of the transistors, thereby reducing the Early effect.

2 The circuit as claimed in claim 1 further including a third and fourth transistor, the third transistor being coupled to the emitter of the first transistor and the fourth transistor being coupled via the load resistor to the emitter of the second transistor, the emitter area of the fourth transistor being greater than that of the first or third transistor, such that the first and third transistors operate at a higher current density than the second and fourth transistors and wherein a PTAT voltage is provided via a resistor, in the feedback loop, at the second input to the amplifier such that the voltage provided at the output of the

amplifier is a combination of the base emitter voltages of the first and third transistors plus the PTAT voltage.

3. The circuit as claimed in claim 2 wherein each of the third and
5 fourth transistors are provided in a diode connected configuration.

4. The circuit as claimed in claim 2 wherein the emitter of the third
transistor is coupled via a second resistor to ground, the value of the resistor
effecting a shifting of the reference voltage from twice the natural bandgap
10 voltage to a desired voltage, thereby enabling an offset adjustment to the
circuit.

5. The circuit as claimed in claim 3 further including a third and
fourth resistor provided in each of the feedback loop paths between the output
15 of the amplifier and the collectors of the first and second transistors
respectively.

6. The circuit as claimed in claim 5 wherein the resistors provided in
each of the feedback loops are substantially the same value..
20

7. The circuit as claimed in claim 5 wherein the resistors provided in
each of the feedback loops are of different values.

8. The circuit as claimed in claim 5 further including circuitry adapted
25 to provide the base current for the non-diode connected transistor and to
extract that same current from the collector of the same transistor, thereby

maintaining the collector current of each of the first and second transistors at the same value.

9. The circuit as claimed in claim 5 further including circuitry adapted to provide the base current for the non-diode connected transistor and to extract that same current from the collector of the same transistor, the circuitry adapted to compensate for base current variation between the non-diode connected transistor and the other transistor, thereby reducing errors in the circuit due to the base current.

10

10. The circuit as claimed in claim 8 wherein the non-diode connected transistor is the first transistor and the circuitry adapted to extract the current from the collector of the first transistor includes a replication of the leg of the circuit defined by the first and third transistors, the replicated leg including a fifth and sixth transistor of the circuit, the base of the fifth transistor being coupled to the collector of the first transistor, the emitter of the fifth transistor being coupled to the collector of the sixth transistor, the base of the sixth transistor being coupled to the diode connected base of the third transistor thereby providing a current mirror, such that a base current is extracted from the collector of the first transistor by the fifth transistor.

11. The circuit as claimed in claim 10 wherein the base current of the first and second transistors is further mirrored via seventh and eight transistors and a bipolar mirror, the base currents of the sixth and eight transistors being supplied by a double current mirror from the output of the amplifier such that the collector currents of each of the third, sixth and eight transistors are the same.

12. The circuit as claimed in claim 11 wherein the collector of the fifth transistor is coupled via a resistor to the output of the amplifier, the value of the resistor being substantially equivalent to that of the fourth resistor such that the
5 base current of the fifth transistor tracks the base current of the first transistor.

13. The circuit as claimed in claim 11 wherein the base current of the first and second transistors is further mirrored via a series of mirrors coupled to the fifth and seventh transistors such that the mirrored current may be extracted
10 from the emitters of the fifth and seventh transistors thereby ensuring that the collector currents of the fifth and seventh transistors are substantially the same value, this current being further mirrored via a current mirror coupled between the collector of the seventh transistor and the output of the amplifier, thereby providing a PTAT current.

15

14. The circuit as claimed in claim 3 further including circuitry adapted to provide a correction voltage adapted to compensate for the curvature of the voltage of the first and third transistors, the incorporation of the correction voltage effecting a cancelling of the curvature.

20

15. The circuit as claimed in claim 14 wherein the circuitry adapted to provide a correction voltage is adapted to provide a mixture of PTAT and CTAT voltages at the load resistor.

25

16. The circuit as claimed in claim 14 wherein the correction voltage is provided by mirroring the base-emitter voltage of the fourth transistor across a resistor and effecting the generation of a complimentary to absolute

temperature (CTAT) current using a MOSFET device and amplifier, the CTAT current being provided back into the fourth transistor via at least one current mirror thereby replicating across the load resistor a voltage having an inverse curvature, the combination of this replicated voltage and the previously present
5 voltage (ΔV_{be}) effecting a cancellation of the curvature.

17. The circuit as claimed in claim 15 wherein the size of the voltage having an inverse curvature may be modified by changing the slope of the current provided by the current mirror and fourth transistor.

10

18. The circuit as claimed in claim 1 further including a plurality of additional transistors coupled to the third and fourth transistors, the plurality of additional transistors being provided in a stack arrangement, thereby enabling a use of the reference circuit with higher reference voltages.

15

19. A bandgap reference voltage circuit including a first amplifier having a first and second input and providing a voltage reference at the output thereof, the amplifier being coupled at its first input to a first transistor and at the second input to a second transistor, the amplifier being coupled in a
20 feedback loop to the collector of each of the transistors, the second transistor having an emitter area larger than that of the first transistor, the circuit additionally including a third and fourth transistor, each being provided in a diode connected configuration, and wherein:

the second transistor is coupled at its emitter to a load resistor, the load
25 resistor providing, in use, a measure of the difference in base emitter voltages between the first and second transistors, ΔV_{be} , for use in the formation of the bandgap reference voltage,

the bases of each transistor are commonly coupled such that the base of the first and second transistor is at the same potential,

one of the first and second transistors is provided in a diode connected configuration,

5 the third transistor is coupled to the emitter of the first transistor and the fourth transistor is coupled via the load resistor to the emitter of the second transistor, the emitter area of the fourth transistor being greater than that of the first or third transistor, such that the first and third transistors operate at a higher current density than the second and fourth transistors and wherein a
10 PTAT voltage is provided via a resistor, in a feedback loop of the amplifier, at the second input to the amplifier such that the voltage provided at the output of the amplifier is a combination of the base emitter voltages of the first and third transistors plus the PTAT voltage, and

the base-collector voltage of the other of the first and second transistors is
15 minimized by the amplifier which is coupled in a feedback loop to the collector of each of the transistors, thereby reducing the Early effect.

20. A method of providing a bandgap reference voltage circuit adapted to compensate for the Early effect, the method comprising the steps of:
20 providing first and second transistors, each transistor adapted to operate at different current densities, the first transistor being provided in a diode connected configuration, the transistors being additionally coupled to the inputs of an amplifier,

scaling the voltage difference between two transistors operating at
25 different current densities so as to provide a reference voltage at an output of the amplifier,

providing a feedback loop, the feedback loop coupling each of the first and second transistors to the output of the amplifier so as to provide at an output of an amplifier a voltage reference, such that the collector base voltage of each of the first and second transistors is reduced to zero.

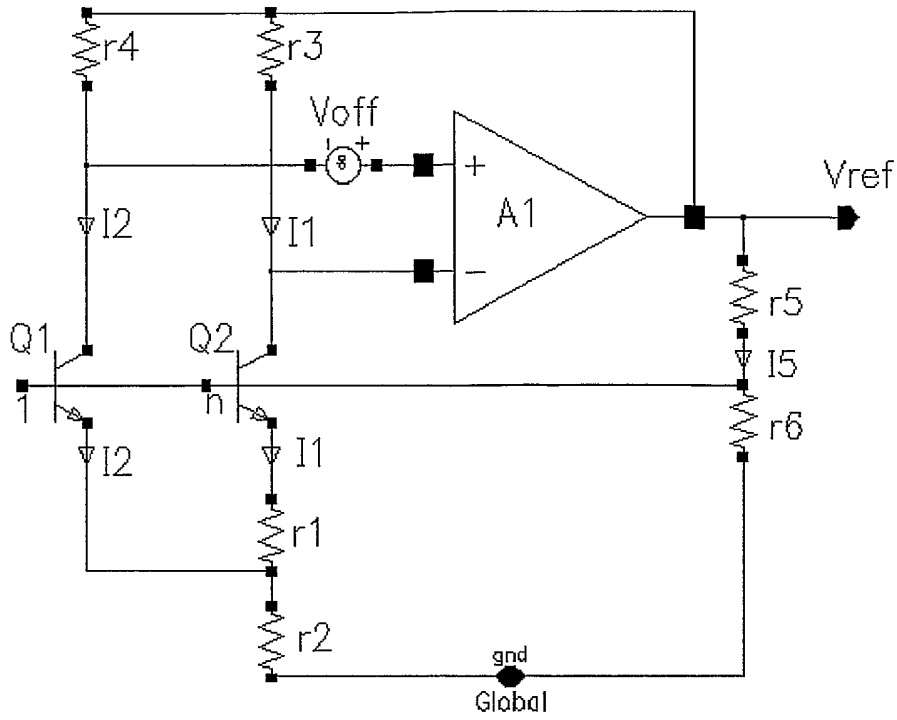


Fig.1. Prior Art

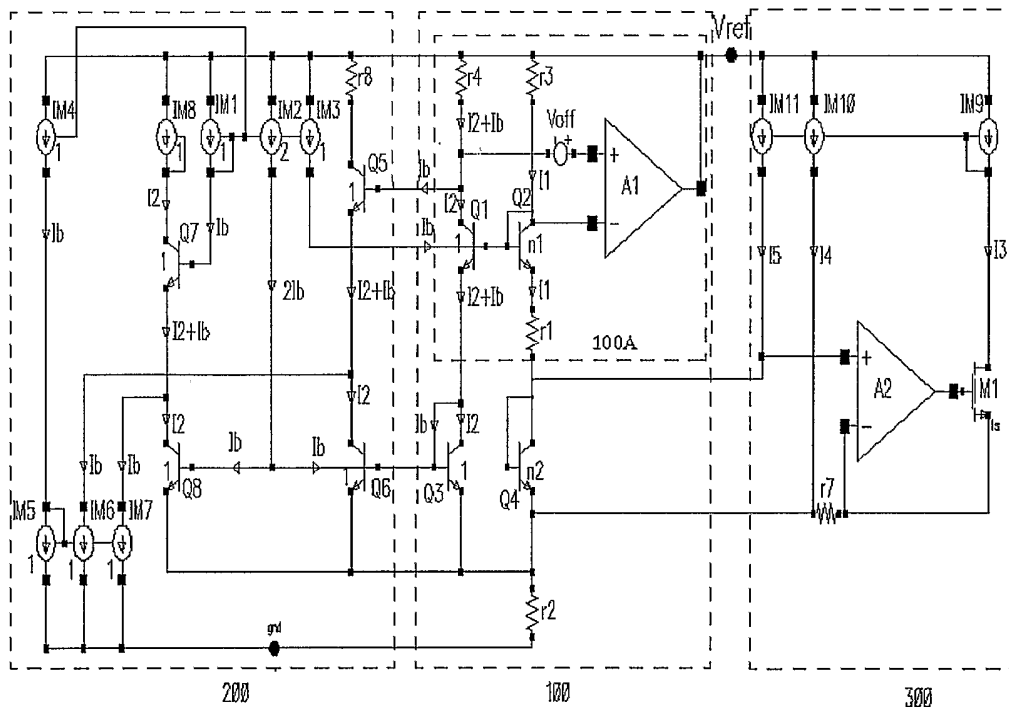


Fig.2

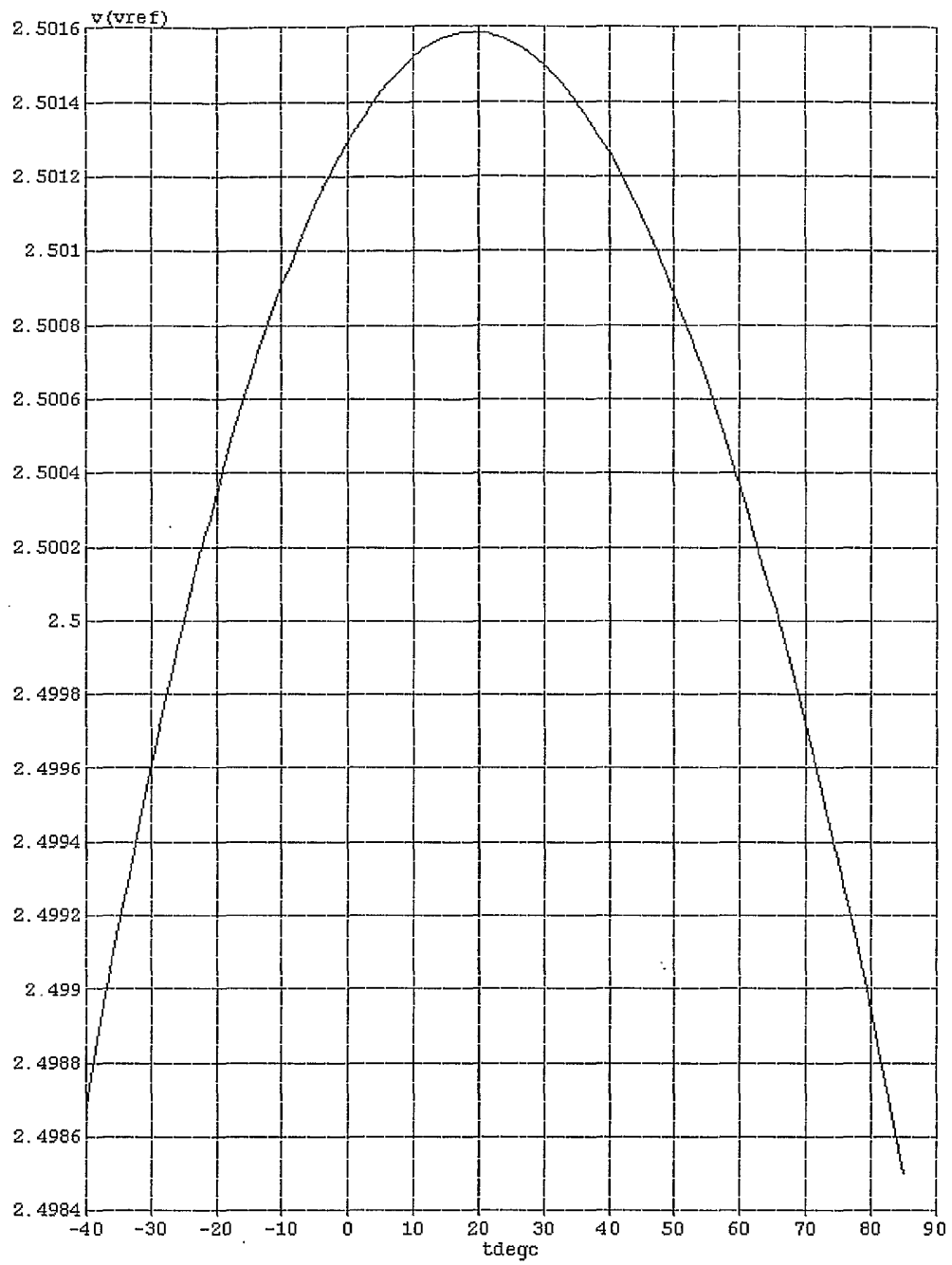


Fig.3

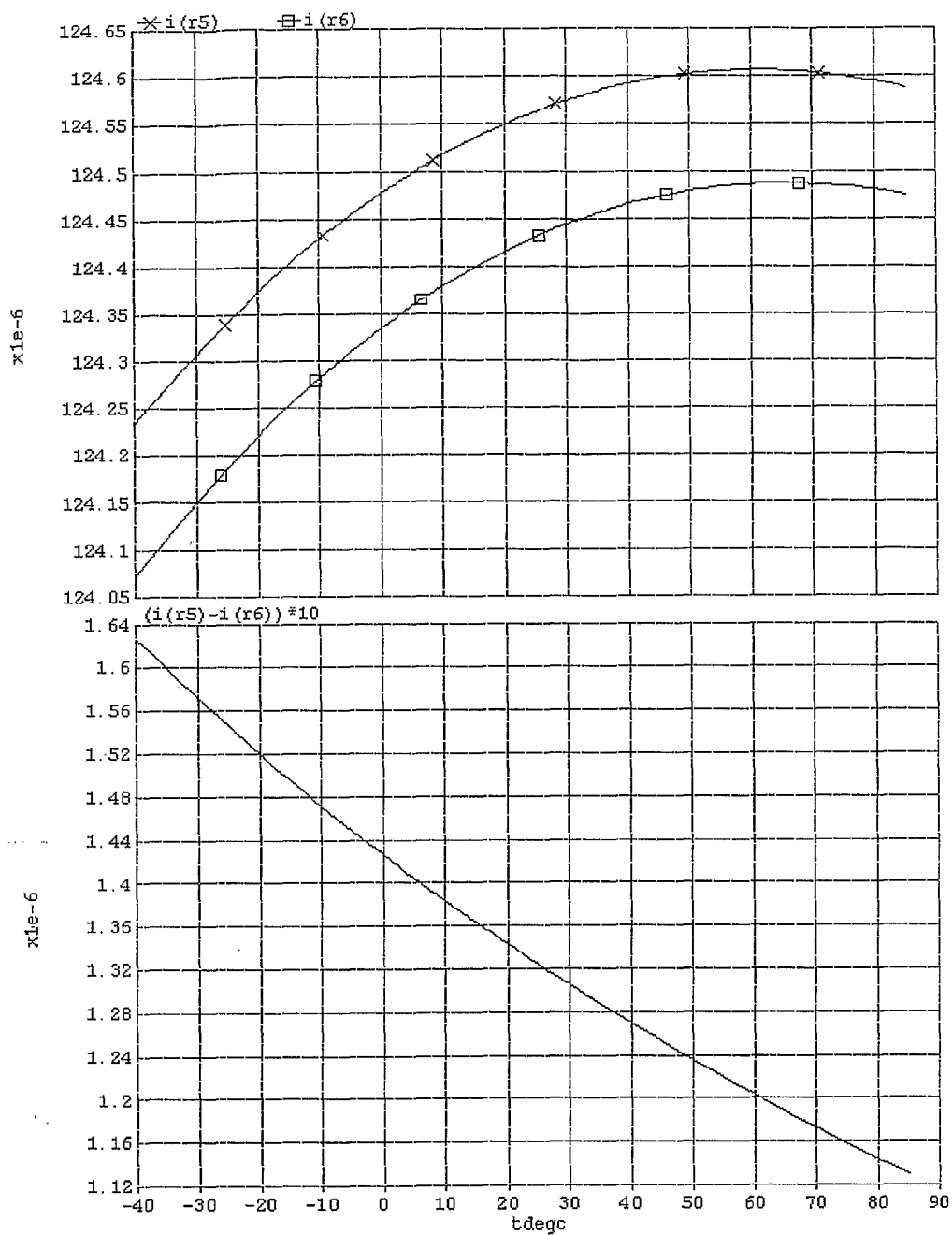


Fig.4

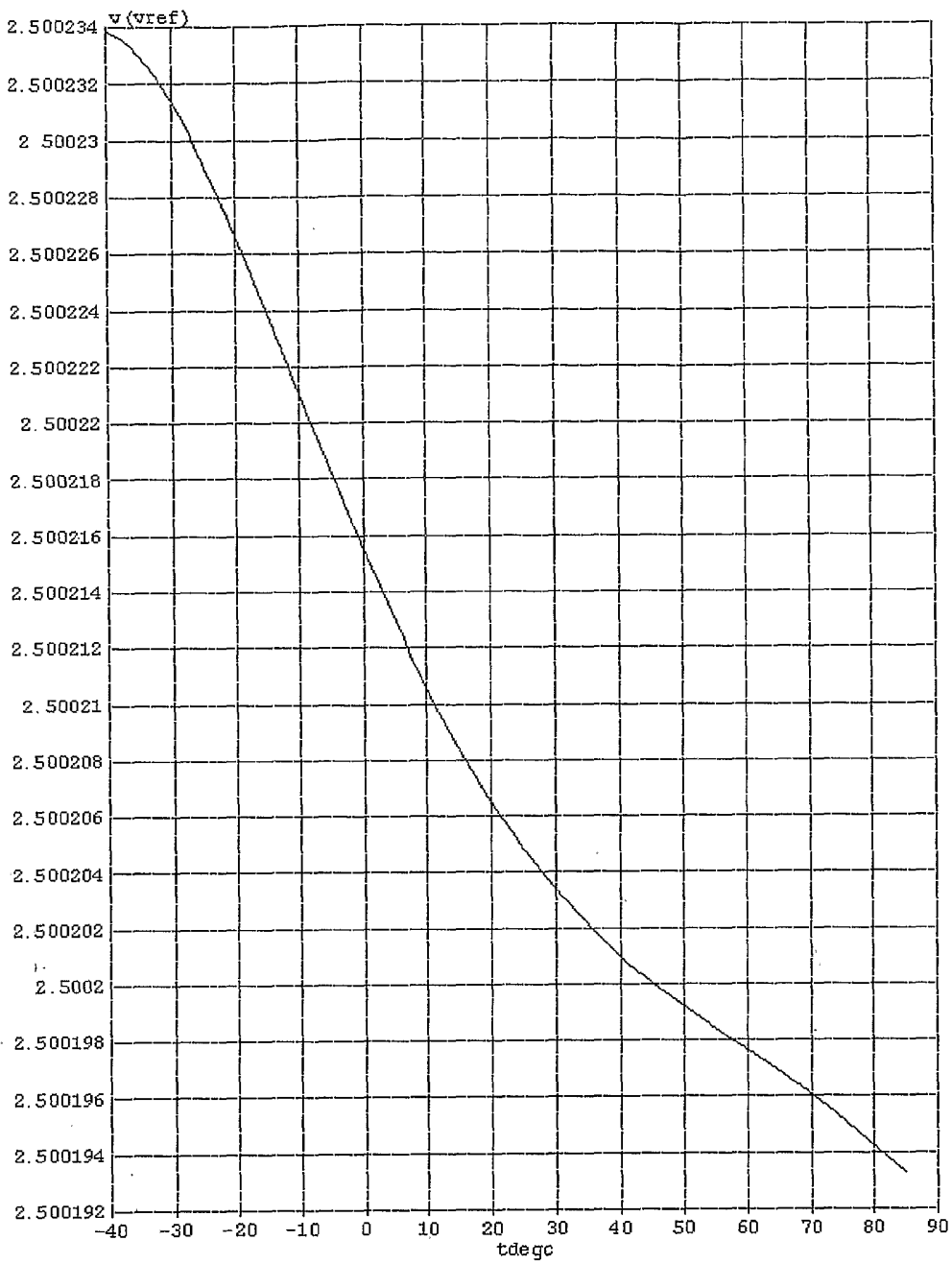


Fig.5

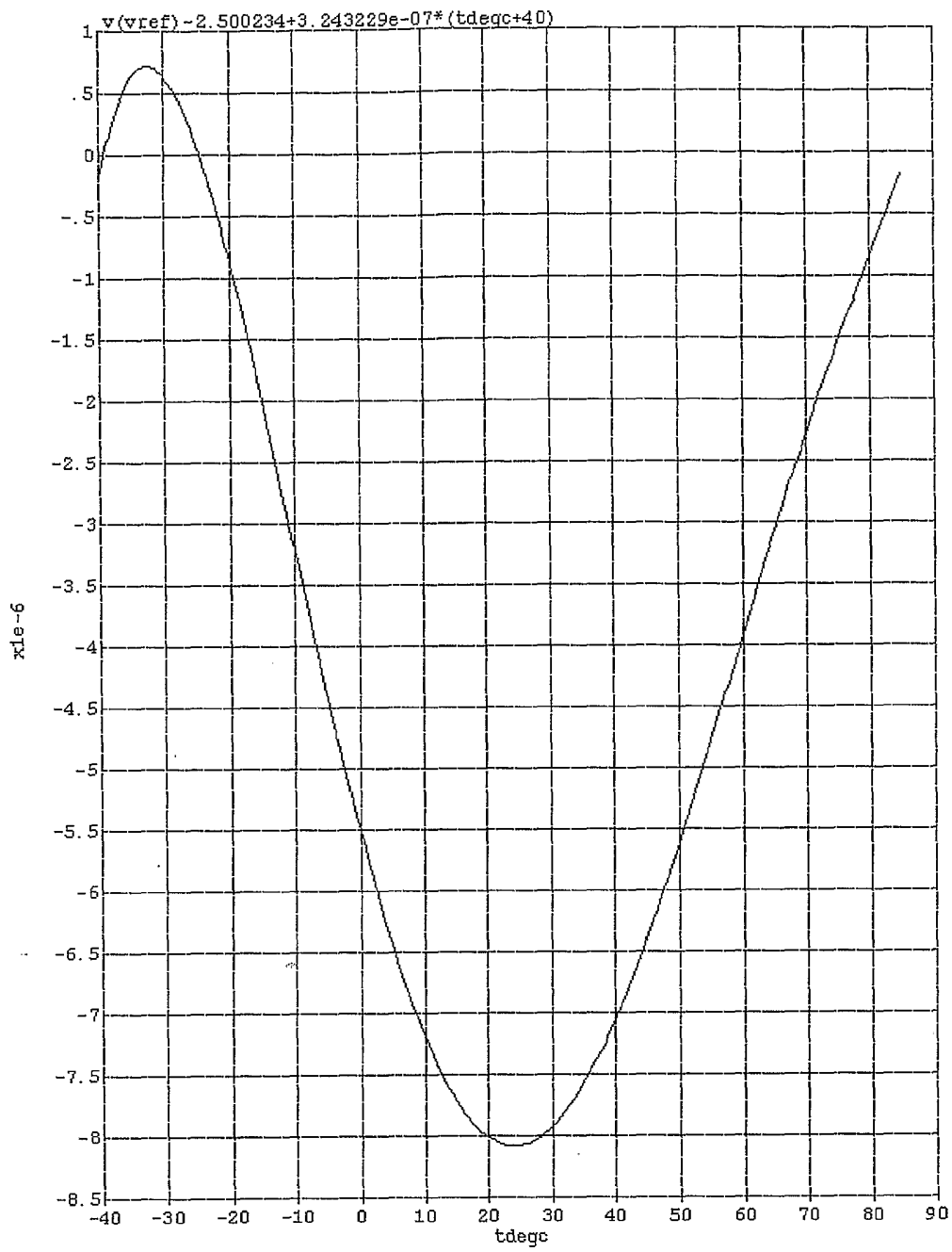


Fig.6

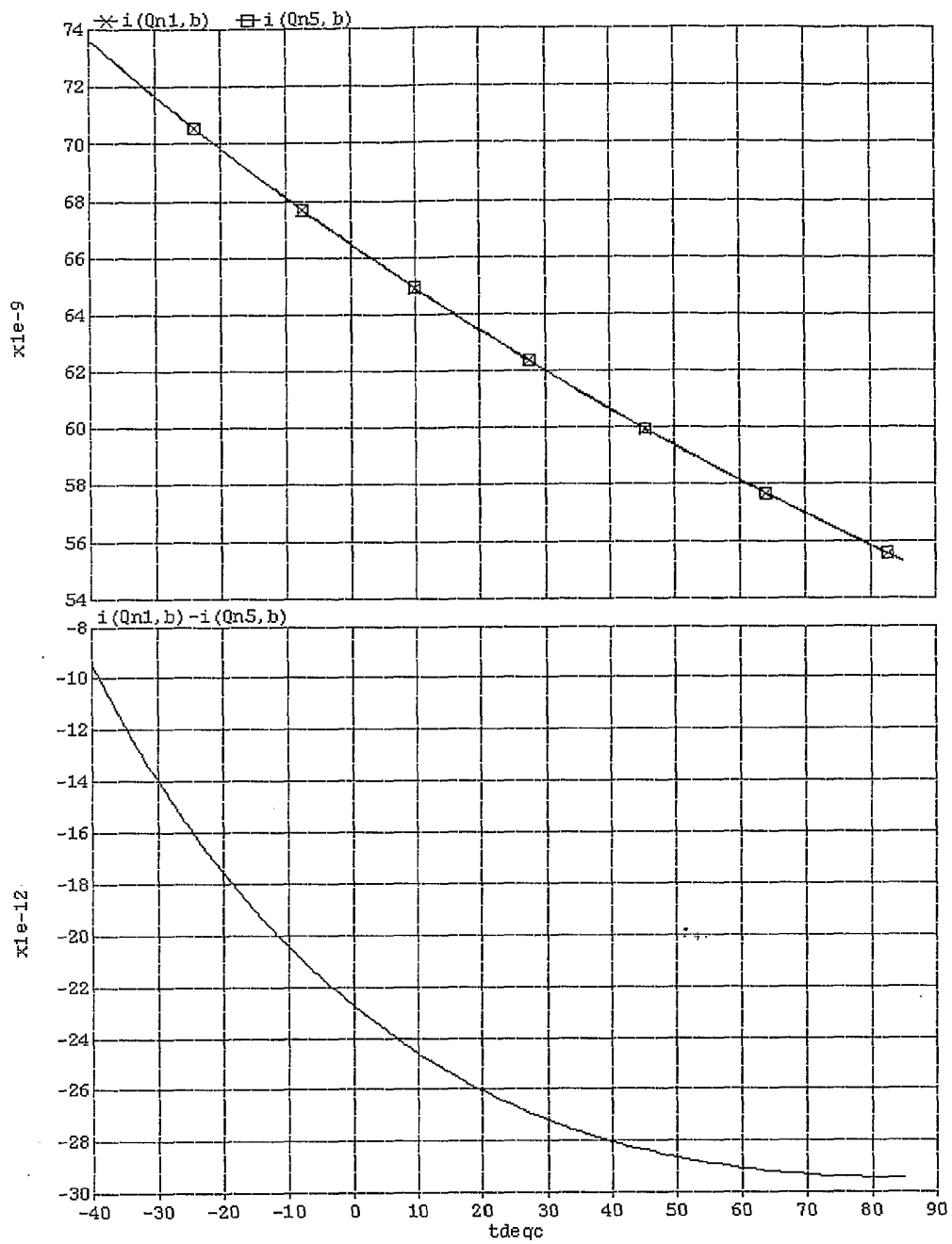


Fig.7

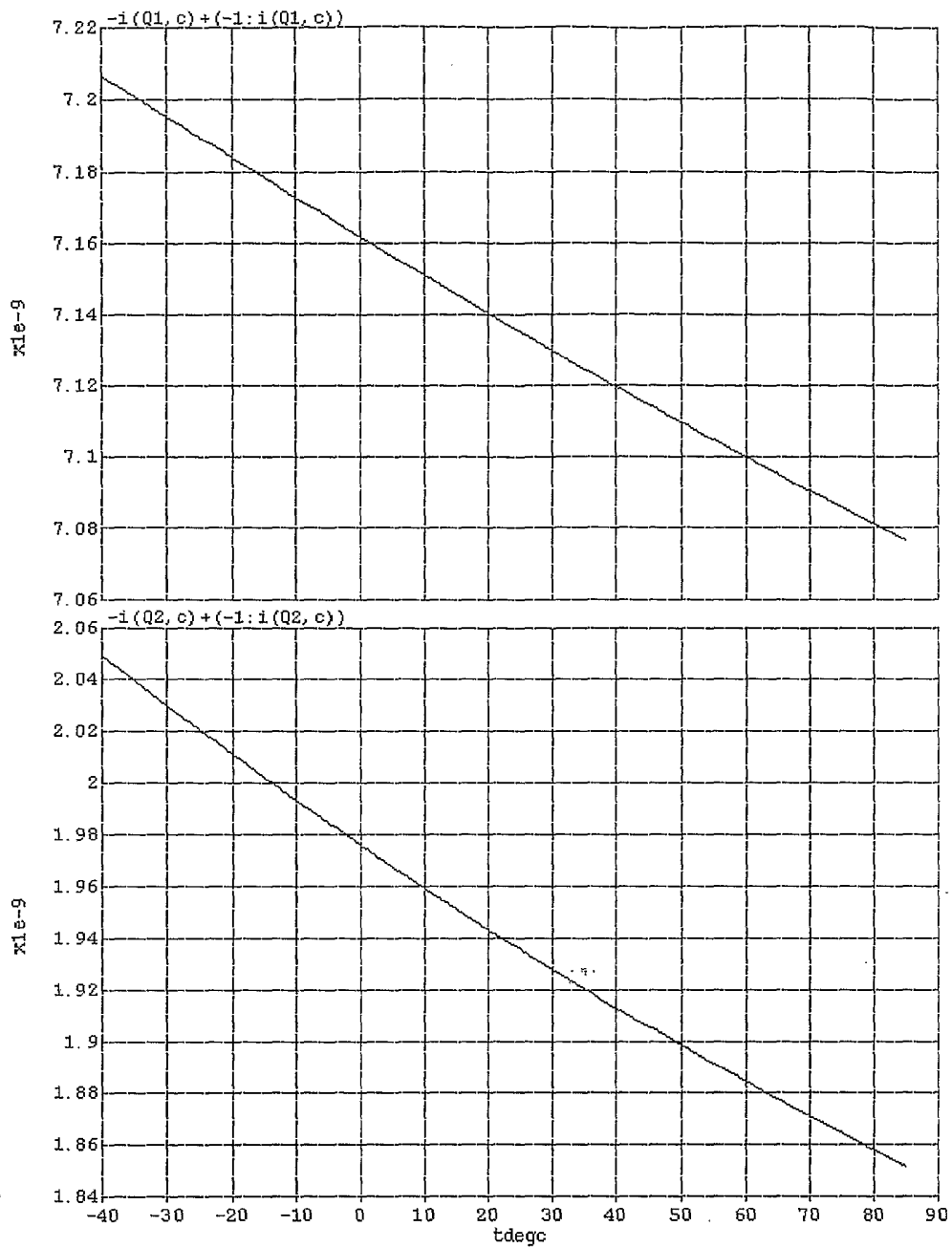


Fig.8

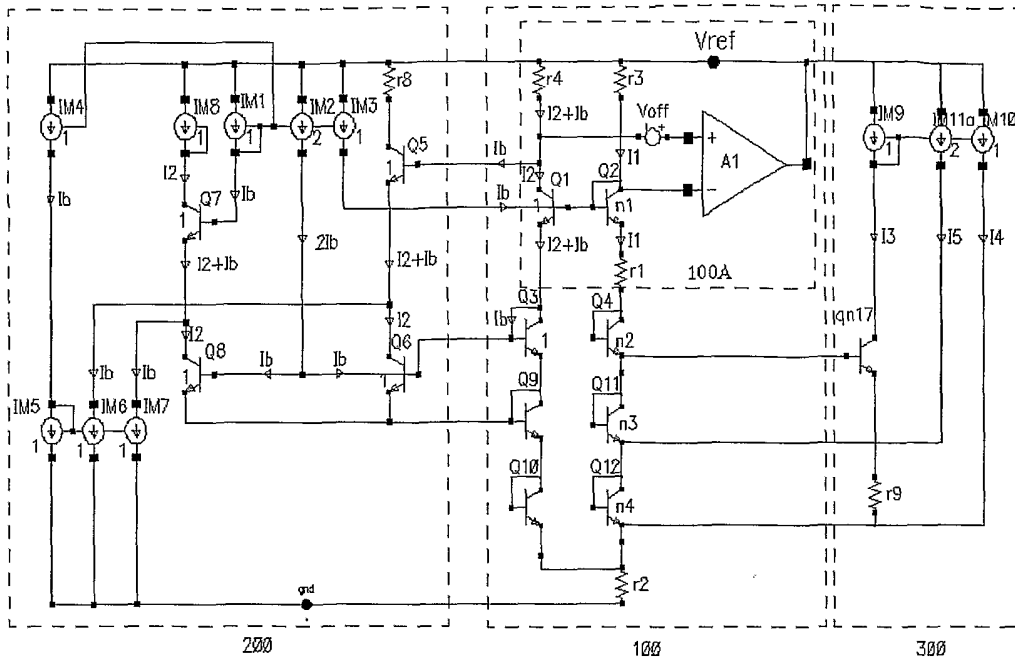


Fig.9

Mean = 5.0005431 V
 Standard Deviation = 0.9580 mV

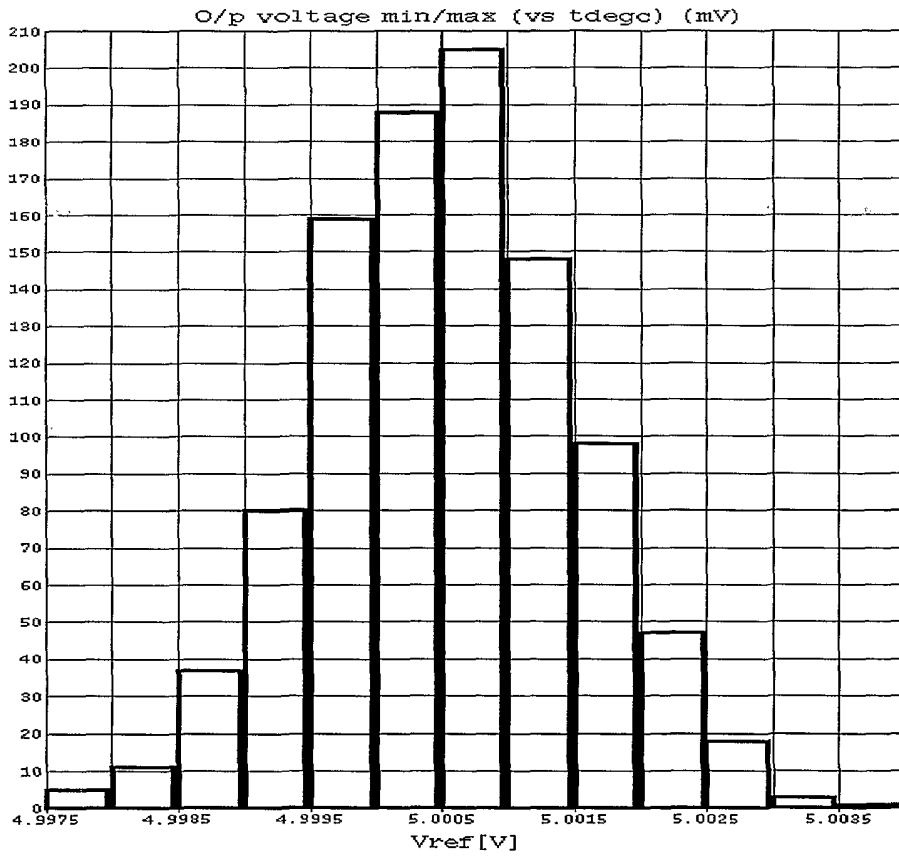


Fig.10

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/053306A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G05F1/46 G05F3/22

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 132 795 A (INFINEON TECHNOLOGIES AG) 12 September 2001 (2001-09-12) paragraphs '0003! - '0008!; figure 2	1, 18, 20
A	US 3 914 684 A (LEIDICH ET AL) 21 October 1975 (1975-10-21) column 3, lines 1-39; figure 2	18

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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Date of the actual completion of the international search

17 March 2005

Date of mailing of the international search report

29/03/2005

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/EP2004/053306

Patent document cited in search report	Publication date	Publication date	Patent family member(s)	Publication date
EP 1132795	A	12-09-2001	DE 10011669 A1 EP 1132795 A1	20-09-2001 12-09-2001
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US 3914684	A	21-10-1975	CA 1018616 A1 DE 2447517 A1 FR 2247006 A1 GB 1477224 A JP 977844 C JP 50066139 A JP 54012305 B US B403990 I5	04-10-1977 17-04-1975 02-05-1975 22-06-1977 29-11-1979 04-06-1975 22-05-1979 28-01-1975
<hr style="border-top: 1px dashed black;"/>				