

(51) International Patent Classification:  
*H01L 21/027* (2006.01)

(21) International Application Number:

PCT/US2009/048873

(22) International Filing Date:

26 June 2009 (26.06.2009)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

12/164,977 30 June 2008 (30.06.2008) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR),

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(54) Title: METHODS FOR FABRICATING LINE/SPACE ROUTING BETWEEN C4 PADS

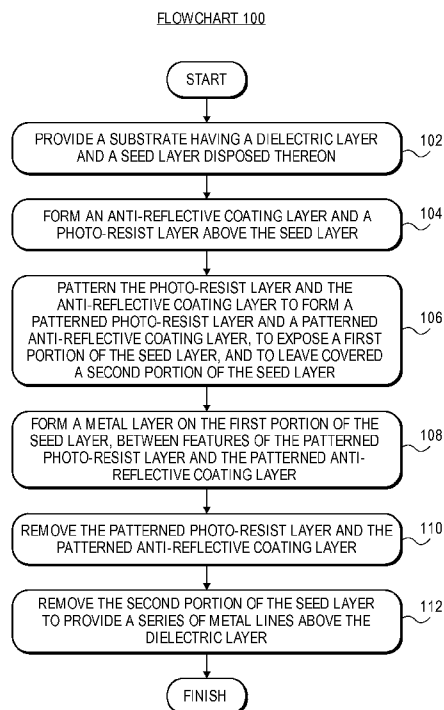


FIG. 1

(57) Abstract: A method for fabricating fine line and space routing described. The method includes providing a substrate having a dielectric layer and a seed layer disposed thereon. An anti-reflective coating layer and a photo-resist layer are then formed above the seed layer. The photo-resist layer and the anti-reflective coating layer are patterned to form a patterned photo-resist layer and a patterned anti-reflective coating layer, to expose a first portion of the seed layer, and to leave covered a second portion of the seed layer. A metal layer is then formed on the first portion of the seed layer, between features of the patterned photo-resist layer and the patterned anti-reflective coating layer. The patterned photo-resist layer and the patterned anti-reflective coating layer are subsequently removed. Then, the second portion of the seed layer is removed to provide a series of metal lines above the dielectric layer.



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OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**  
— *without international search report and to be republished  
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**METHODS FOR FABRICATING LINE/SPACE ROUTING BETWEEN C4 PADS****TECHNICAL FIELD**

Embodiments of the invention are in the field of semiconductor structures and, in particular, methods for fabricating fine line and space (FLS) routing for high density  
5 interconnect (HDI) substrates.

**BACKGROUND**

A flip chip or Controlled Collapse Chip Connection (C4) is a type of mounting used for semiconductor devices, such as integrated circuit (IC) chips, MEMS or components, which utilizes solder bumps instead of wire bonds. The solder bumps are  
10 deposited on the C4 pads, located on the top side of the substrate package. In order to mount the semiconductor device to the substrate, it is flipped over – the active side facing down on the mounting area. The solder bumps are used to connect the semiconductor device directly to the substrate.

C4 solder ball connections have been used for many years to provide flip chip  
15 interconnections between semiconductor devices and substrates. Hemispherical C4 solder bumps are formed above an insulation layer and above the exposed surfaces of connector pads (also known as bump pads), each of which is exposed through a via hole in the insulation layer or layers. Subsequently, the solder bumps are heated above their melting point until they reflow and form a connection with the Cu stud bumps of the die. The  
20 actual C4 solder bumps may be fabricated using a number of different processing techniques, including evaporation, screen printing, and electroplating. Fabrication by electroplating requires a series of basic operations which typically include the deposition of a metallic seed layer, the application of an imaged photo-resist (in the pattern of C4 solder bumps), the electro-deposition of solder, the stripping of the photo-resist, and the  
25 sub-etching of the metallic seed layer to isolate the C4 bumps.

As semiconductor structures become more advanced, the need for higher I/O density leads to a tighter C4 bump pitch. This, in turn, puts stringent requirements on the fabrication and dimensions of the line and spacing..

**BRIEF DESCRIPTION OF THE DRAWINGS**

30 Figure 1 is a Flowchart representing operations in a method for fabricating fine line and space routing in an organic substrate package, in accordance with an embodiment of the present invention.

Figures 2A-2H illustrate cross-sectional views representing operations in a method for fabricating fine line and space routing in an organic substrate package, in accordance with an embodiment of the present invention.

### **DETAILED DESCRIPTION**

5 Methods for fabricating fine line and space routing in an organic substrate package are described. In the following description, numerous specific details are set forth, such as integration schemes and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that  
10 other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Disclosed herein are methods for fabricating fine line and space routing. A  
15 substrate may be provided having a dielectric layer and a seed layer disposed thereon. In an embodiment, an anti-reflective coating layer and a photo-resist layer are formed above the seed layer. The photo-resist layer and the anti-reflective coating layer are then patterned to form a patterned photo-resist layer and a patterned anti-reflective coating layer, to expose a first portion of the seed layer, and to leave covered a second portion of  
20 the seed layer. A metal layer is formed on the first portion of the seed layer, between features of the patterned photo-resist layer and the patterned anti-reflective coating layer. The patterned photo-resist layer and the patterned anti-reflective coating layer are subsequently removed. In one embodiment, the second portion of the seed layer is then removed to provide a series of metal lines above the dielectric layer.

25 In accordance with an embodiment of the present invention, the application of an anti-reflective coating layer is used to control the amount of reflection from a seed layer, by absorbing the reflected light during a lithographic process. By absorbing the reflected light, the exposure of regions of a photo-resist layer undergoing a patterning process may be better controlled. For example, in one embodiment, the undesirable exposure of  
30 regions of the photo-resist layer is substantially reduced, if not eliminated, by using an anti-reflective coating layer between the seed layer and the photo-resist layer for the lithographic process. Accordingly, line-width variation among the features in a patterned photo-resist layer may be mitigated as compared with line-width variation resulting from

scattering in the absence of an anti-reflective coating layer. In one embodiment, by incorporating an anti-reflective coating layer into an integration scheme for fabricating fine lines and spaces, the density of such routing can be increased, while the line-widths of individual lines in such routing can be decreased, to enable the scaling of such routing to accommodate ever the increasing I/O density. In accordance with an embodiment of the present invention, the use of an anti-reflective coating layer between a seed layer and a photo-resist layer for a lithographic process reduces the extent of line-edge roughness (e.g. reflective notching) common to processes that do not use an anti-reflective coating layer.

In an embodiment of the present invention, an anti-reflective coating layer is used in a method for fabricating fine line and space routing. Figure 1 is a Flowchart 100 representing operations in a method for fabricating fine line and space routing in an organic substrate package, in accordance with an embodiment of the present invention. Figures 2A-2H illustrate cross-sectional views representing operations in a method for fabricating fine line and space routing in an organic substrate package, in accordance with an embodiment of the present invention.

Referring to operation 102 from Flowchart 100 and corresponding Figure 2A, a build-up layer 202 is provided having a dielectric layer 204 disposed thereon. In accordance with an embodiment of the present invention, build-up layer 202 and dielectric layer 204 form a stack of layers 200 included in an organic substrate package. For example, in one embodiment, the stack of layers 200 can include any build-up layer that requires fine line and space routing. In an embodiment, dielectric layer 204 has a roughened surface 206, e.g. dielectric layer 204 is subjected to a desmear process, as depicted in Figure 2A.

Dielectric layer 204 may be a layer suitable for electrically isolating devices and interconnects on the face of build-up layer 202 from subsequently formed fine line/space routing disposed above or below the dielectric layer 204. In an embodiment, dielectric layer 204 is composed of an epoxy-based material with silica fillers. In one embodiment, dielectric layer 204 has a roughened surface 206 with an average surface roughness approximately in the range of 0.5 – 0.6 microns, i.e. the average depth of the V-grooves in roughened surface 206 is approximately in the range of 0.5 – 0.6 microns. In an embodiment, dielectric layer 204 is roughened to have roughened surface 206 in order to better adhere with a subsequently deposited metal layer, such as an electro-less deposited metal layer, as described below. In an embodiment, roughened surface 206 of dielectric

layer 204 is formed by desmear process following laser via drilling. In an embodiment, the surface of dielectric layer 204 is not roughened.

Build-up layer 202 may be composed of a material suitable for semi-additive process (SAP) fabrication. In one embodiment, build-up layer 202 is an epoxy based dielectric material with silica fillers. In another embodiment, build-up layer 202 includes a copper plane.

Referring again to operation 102 from Flowchart 100 and corresponding Figure 2B, a seed layer 208 is disposed on dielectric layer 204. In accordance with an embodiment of the present invention, seed layer 208 is formed to be conformal with dielectric layer 204, e.g. seed layer 208 has the same or a similar topography as roughened surface 206, as depicted in Figure 2B. In an embodiment, seed layer 208 partially or completely fills any top surface roughness of dielectric layer 204 to provide a substantially flat top surface for seed layer 208. In an embodiment, seed layer 208 has a thickness approximately in the range of 0.5 – 1 microns. In an embodiment, seed layer 208 has a thickness of approximately 0.7 microns. Seed layer 208 may be a layer suitable for subsequent electrolytic plating of a metal film onto its surface. In an embodiment, seed layer 208 is composed of a metal or metal-containing alloy such as, but not limited to, copper, silver, nickel, aluminum. In an embodiment, seed layer 208 is formed on dielectric layer 204 by an electro-less deposition process. Metal sputtering is an alternative metal deposition process that could be used.

Referring to operation 104 from Flowchart 100 and corresponding Figure 2C, an anti-reflective coating layer 210 is formed above seed layer 208. In accordance with an embodiment of the present embodiment, anti-reflective coating layer 210 is formed above seed layer 208 to absorb light reflected from the metal surface and from the roughened topography of seed layer 208, as depicted in Figure 2C, during a subsequent lithographic process. Also, in one embodiment and as depicted in Figure 2C, anti-reflective coating layer 210 fills in the surface roughness of seed layer 208 in order to provide a flat surface for anti-reflective coating layer 210, upon which a photo-resist layer is subsequently deposited. In an embodiment, anti-reflective coating layer 210 has a thickness, as measured from the top surface of seed layer 208, approximately in the range of 1 – 2 microns. In an embodiment, anti-reflective coating layer 210 has a thickness, as measured from the top surface of seed layer 208, of approximately 1.5 microns.

Anti-reflective coating layer 210 may be composed of a material that substantially absorbs scattered light produced during a lithographic process. In accordance with an embodiment of the present invention, anti-reflective coating layer 210 is composed of an organic compound and a dye. In one embodiment, anti-reflective coating layer 210 is composed of material such as, but not limited to, a water-soluble polymer Aquazol, organosiloxane based film. In an embodiment, the composition of anti-reflective coating layer 210 is selected to be chemically compatible with a photo-resist layer subsequently formed on the surface of anti-reflective coating layer 210.

Anti-reflective coating layer 210 may be formed on seed layer 208 by a technique suitable to uniformly cover seed layer 208 and to provide a flat surface upon which a photo-resist layer may subsequently be deposited. In one embodiment, anti-reflective coating layer 210 is formed by a process such as, but not limited to, spray-coating or roll-coating. In another embodiment, anti-reflective coating layer 210 is formed by a spin-on process. In an embodiment, a solvent is used to aid in the coating of anti-reflective coating layer 210 onto the surface of dielectric layer 204, and, in order to remove the solvent following its formation, anti-reflective coating layer 210 is subsequently exposed to a bake process at a temperature of approximately, but not limited to, 150 degrees Celsius.

Referring again to operation 104 from Flowchart 100 and corresponding Figure 2D, a photo-resist layer 212 is formed above anti-reflective coating layer 210. Photo-resist layer 212 may be composed of a material suitable for undergoing a lithographic process. In accordance with an embodiment of the present invention, photo-resist layer 212 is composed of a dry film resist or a liquid resist. In an embodiment, photo-resist layer 212 is composed of a negative tone liquid photo-resist. In one embodiment, photo-resist layer 212 is composed of a two-component DQN resist including a photoactive diazoquinone ester (DQ) and a phenolic novolak resin (N). Photo-resist layer 212 may be formed on anti-reflective coating layer 210 by a technique suitable to uniformly cover anti-reflective coating layer 210 and to provide a flat top surface to which a lithographic process is applied. In one embodiment, photo-resist layer 212 is a liquid photo-resist layer formed by a process such as, but not limited to, spray-coating or roll-coating onto the surface of anti-reflective coating layer 210. In another embodiment, photo-resist layer 212 is formed by a lamination process and is a dry film photo-resist layer. In one embodiment, the dry film photo-resist layer is cyclized poly(cis-isoprene) resin-based. In an

embodiment, photo-resist layer 212 has a thickness approximately in the range of 10 – 15 microns. In an embodiment, photo-resist layer 212 is a negative tone or a positive tone photo-resist layer. In an embodiment, the composition of photo-resist layer 212 is selected to be chemically compatible with anti-reflective coating layer 210.

5 Referring to operation 106 from Flowchart 100 and corresponding Figure 2E, photo-resist layer 212 and anti-reflective coating layer 210 are patterned to form a patterned photo-resist layer 214 and a patterned anti-reflective coating layer 216, respectively, to expose a first portion of seed layer 208, and to leave covered a second portion of seed layer 208. In accordance with an embodiment of the present invention, 10 photo-resist layer 212 and anti-reflective coating layer 210 are patterned to form patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 by a masked lithographic process. In that embodiment, photo-resist layer 212 and anti-reflective coating layer 210 are exposed to a light source via masked lithography which changes portions of photo-resist layer 212 and anti-reflective coating layer 210. In an embodiment, 15 anti-reflective coating layer 210 absorbs light scattered by seed layer 208 during the lithographic exposure operation. In one embodiment, anti-reflective coating layer 210 is patterned to form patterned anti-reflective coating layer 216 in the same development process step used to pattern photo-resist layer 212. In that embodiment, photo-resist layer 212 is first exposed to a masked lithographic process. Next, in the same process step, 20 photo-resist layer 212 and anti-reflective coating layer 210 are developed to form patterned photo-resist layer 214 and patterned anti-reflective coating layer 216, respectively. In an embodiment, photo-resist layer 212 and anti-reflective coating layer 210 are developed by a solution such as, but not limited to, 1 weight %  $\text{Na}_2\text{CO}_3$  or tetramethylammonium hydroxide (TMAH). In another embodiment, anti-reflective coating layer 210 is patterned to form patterned anti-reflective coating layer 216 in a 25 different process step than the process step used to pattern photo-resist layer 212. In an embodiment, photo-resist layer 212 is first exposed to a masked lithographic and development process to form patterned photo-resist layer 214. Next, using patterned photo-resist layer 214 as a mask, anti-reflective coating layer 210 is dry or wet etched to 30 form patterned anti-reflective coating layer 216.

Referring to operation 108 from Flowchart 100 and corresponding Figure 2F, a metal layer 218 is formed on the exposed portion of seed layer 208, between features of patterned photo-resist layer 214 and patterned anti-reflective coating layer 216. In

accordance with an embodiment of the present invention, metal layer 218 is formed on the exposed portion of seed layer 208 by an electrolytic deposition process. Metal layer 218 may be composed of a metal suitable for strong adhesion with seed layer 208 and suitably conductive for forming a conductive line. In an embodiment, both seed layer 208 and  
5 metal layer 218 are composed of copper.

Referring to operation 110 from Flowchart 100 and corresponding Figure 2G, patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 are removed. In accordance with an embodiment of the present invention, patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 are removed by a  
10 photoresist stripping solution. In an embodiment, patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 are removed by an amine-based stripping solution. In one embodiment, patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 are removed in the same process step. In an embodiment, patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 are  
15 removed in separate process steps.

Referring to operation 112 from Flowchart 100 and corresponding Figure 2H, the portion of seed layer 208 previously covered by patterned photo-resist layer 214 and patterned anti-reflective coating layer 216 is removed. In accordance with an embodiment of the present invention, this portion of seed layer 208 is removed to provide a series of  
20 metal lines 220 above dielectric layer 204. In one embodiment, the width of each line of the series of lines 220 is less than approximately 5 microns and the spacing between each line in the series of lines 220 is less than approximately 5 microns. The portion of seed layer 208 removed may be removed by a global dry or wet etch process. In an embodiment, the portion of seed layer 208 is removed in an  $H_2O_2/H_2SO_4$  based etching  
25 solution. In one embodiment, the global etch process also reduces the height of each line in the series of lines 220, as depicted in Figure 2G and 2H.

Thus, a method for fabricating fine line and space routing has been disclosed. In accordance with an embodiment of the present invention, the method includes first providing a substrate having a dielectric layer and a seed layer disposed thereon. An anti-reflective coating layer and a photo-resist layer are then formed above the seed layer. The  
30 photo-resist layer and the anti-reflective coating layer are patterned to form a patterned photo-resist layer and a patterned anti-reflective coating layer, to expose a first portion of the seed layer, and to leave covered a second portion of the seed layer. A metal layer is

then formed on the first portion of the seed layer, between features of the patterned photo-resist layer and the patterned anti-reflective coating layer. The patterned photo-resist layer and the patterned anti-reflective coating layer are then removed. Finally, the second portion of the seed layer is removed to provide a series of metal lines above or below the dielectric layer. In one embodiment, the photo-resist layer and the anti-reflective coating layer are patterned in separate process steps. First, the photo-resist layer is exposed to a masked lithographic and development process to form the patterned photo-resist layer. Next, the anti-reflective coating layer is etched to form the patterned anti-reflective coating layer. In another embodiment, the photo-resist layer and the anti-reflective coating layer are patterned in the same process step. First, the photo-resist layer and anti-reflective coating layer are exposed to a masked lithographic process. Next, both the photo-resist layer and the anti-reflective coating layer are developed to form the patterned photo-resist layer and the patterned anti-reflective coating layer.

## CLAIMS

What is claimed is:

1. A method for fabricating fine line and space routing, comprising:
  - forming a seed layer on a substrate having a dielectric layer;
  - 5 forming an anti-reflective coating layer and a photo-resist layer above said seed layer;
  - patterning said photo-resist layer and said anti-reflective coating layer to form a
    - patterned photo-resist layer and a patterned anti-reflective coating layer, to expose
    - a first portion of said seed layer, and to leave covered a second portion of said seed
    - layer;
  - 10 forming a metal layer on said first portion of said seed layer, between features of said
    - patterned photo-resist layer and said patterned anti-reflective coating layer;
    - removing said patterned photo-resist layer and said patterned anti-reflective coating
    - layer; and
    - removing said second portion of said seed layer to provide a series of metal lines
  - 15 above said dielectric layer.
2. The method of claim 1, wherein forming said anti-reflective coating layer comprises spray-coating or roll-coating said anti-reflective coating layer on said seed layer.
3. The method of claim 2, wherein said photo-resist layer is a liquid photo-resist layer, and wherein forming said photo-resist layer comprises spray-coating or roll-coating said
- 20 photo-resist layer on said anti-reflective coating layer.
4. The method of claim 2, wherein forming said anti-reflective coating layer comprises using an organic compound and a dye.
5. The method of claim 1, wherein forming both said seed layer and said metal layer comprises using copper.
- 25 6. The method of claim 1, wherein removing said second portion of said seed layer to provide said series of metal lines comprises forming each line of said series of lines with a width less than approximately 5 microns and a spacing between each line of less than approximately 5 microns.
7. A method for fabricating fine line and space routing, comprising:
  - 30 forming a seed layer on a substrate having a dielectric layer;
  - forming an anti-reflective coating layer and a photo-resist layer above said seed layer;
  - exposing said photo-resist layer to a masked lithographic and development process to
  - form a patterned photo-resist layer;

etching said anti-reflective coating layer to form a patterned anti-reflective coating layer, to expose a first portion of said seed layer, and to leave covered a second portion of said seed layer;

- 5 forming a metal layer on said first portion of said seed layer, between features of said patterned photo-resist layer and said patterned anti-reflective coating layer;
- removing said patterned photo-resist layer and said patterned anti-reflective coating layer; and
- removing said second portion of said seed layer to provide a series of metal lines above said dielectric layer.

10 8. The method of claim 7, wherein removing said patterned photo-resist layer and said patterned anti-reflective coating layer is performed in the same process step.

9. The method of claim 7, wherein forming said anti-reflective coating layer comprises spray-coating or roll-coating said anti-reflective coating layer on said seed layer.

10. The method of claim 9, wherein said photo-resist layer is a liquid photo-resist layer,  
15 and wherein forming said photo-resist layer comprises spray-coating or roll-coating said photo-resist layer on said anti-reflective coating layer.

11. The method of claim 9, wherein forming said anti-reflective coating layer comprises using an organic compound and a dye.

12. The method of claim 7, wherein forming both said seed layer and said metal layer  
20 comprises using copper.

13. The method of claim 7, wherein removing said second portion of said seed layer to provide said series of metal lines comprises forming each line of said series of lines with a width less than approximately 5 microns and a spacing between each line of less than approximately 5 microns.

25 14. A method for fabricating fine line and space routing, comprising:

forming a seed layer on a substrate having a dielectric layer;  
forming an anti-reflective coating layer and a photo-resist layer above said seed layer;  
exposing said photo-resist layer and said anti-reflective coating layer to a masked lithographic process;

30 developing, in the same process operation, said photo-resist layer and said anti-reflective coating layer to form a patterned photo-resist layer and a patterned anti-reflective coating layer, to expose a first portion of said seed layer, and to leave covered a second portion of said seed layer;

forming a metal layer on said first portion of said seed layer, between features of said patterned photo-resist layer and said patterned anti-reflective coating layer; removing said patterned photo-resist layer and said patterned anti-reflective coating layer; and

5 removing said second portion of said seed layer to provide a series of metal lines above said dielectric layer.

15. The method of claim 14, wherein removing said patterned photo-resist layer and said patterned anti-reflective coating layer is performed in the same process step.

16. The method of claim 14, wherein forming said anti-reflective coating layer comprises 10 spray-coating or roll-coating said anti-reflective coating layer on said seed layer.

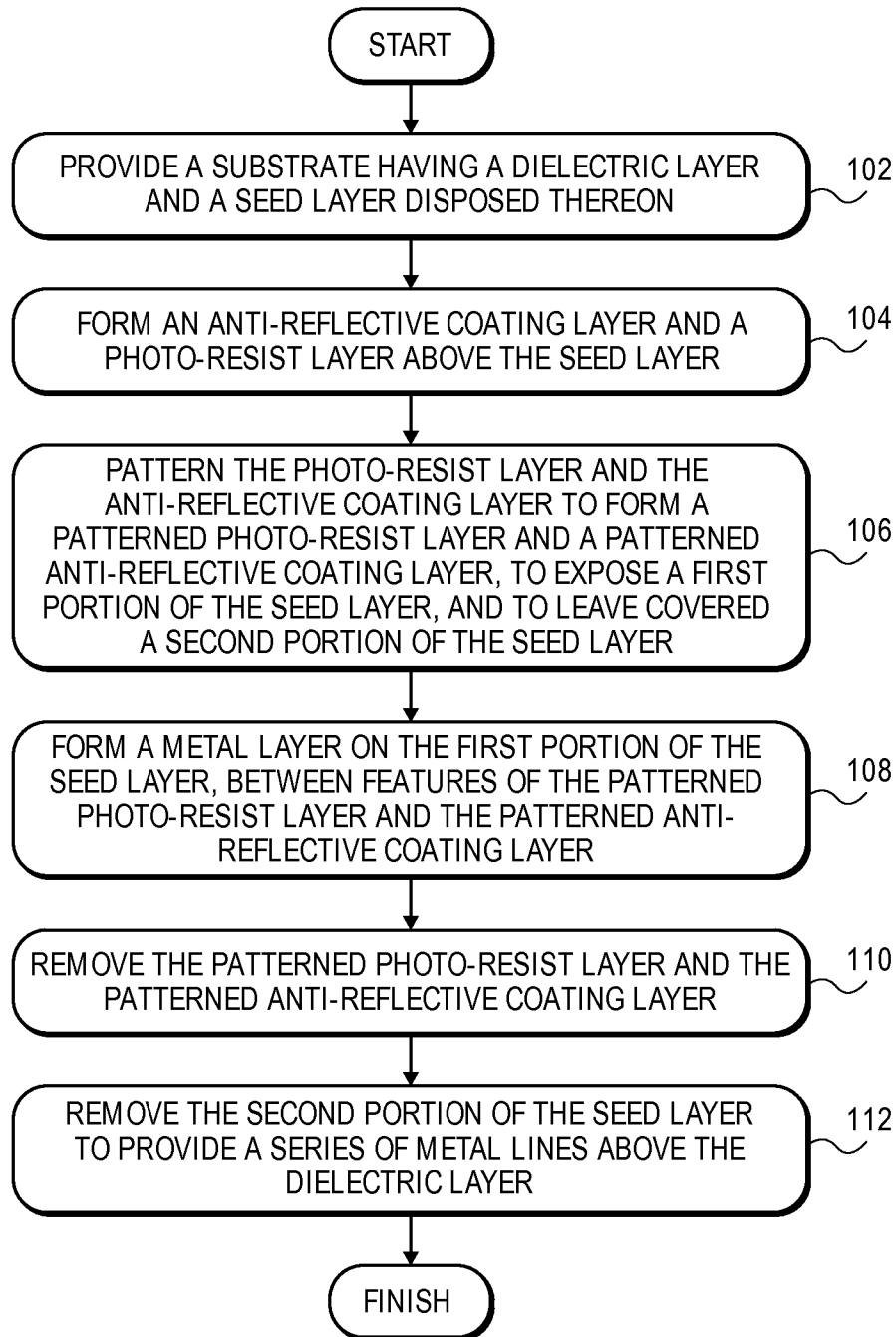
17. The method of claim 16, wherein said photo-resist layer is a liquid photo-resist layer, and wherein forming said photo-resist layer comprises spray-coating or roll-coating said photo-resist layer on said anti-reflective coating layer.

18. The method of claim 16, wherein forming said anti-reflective coating layer comprises 15 using an organic compound and a dye.

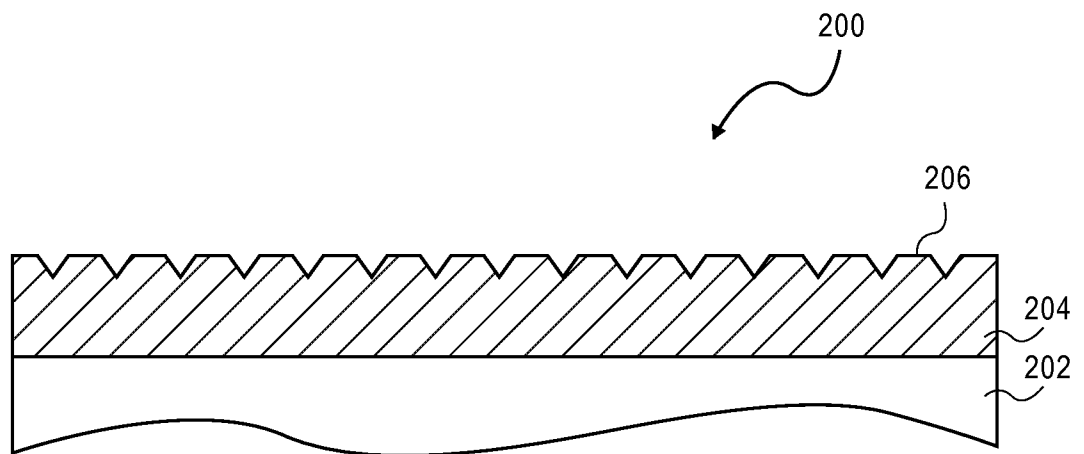
19. The method of claim 14, wherein forming both said seed layer and said metal layer comprises using copper.

20. The method of claim 14, wherein removing said second portion of said seed layer to provide said series of metal lines comprises forming each line of said series of lines with a 20 width less than approximately 5 microns and a spacing between each line of less than approximately 5 microns.

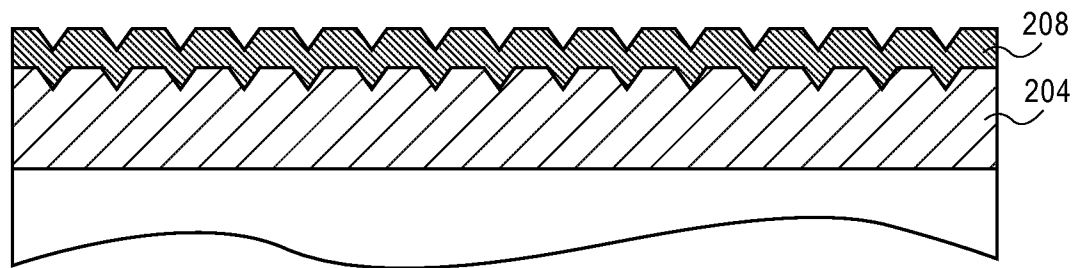
## FLOWCHART 100

**FIG. 1**

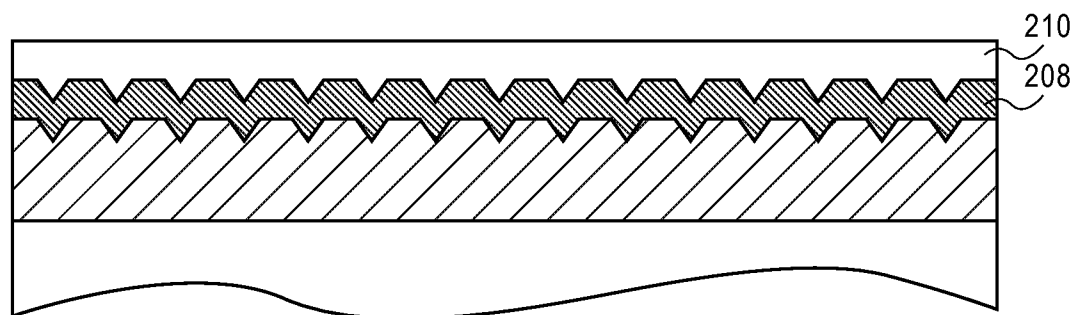
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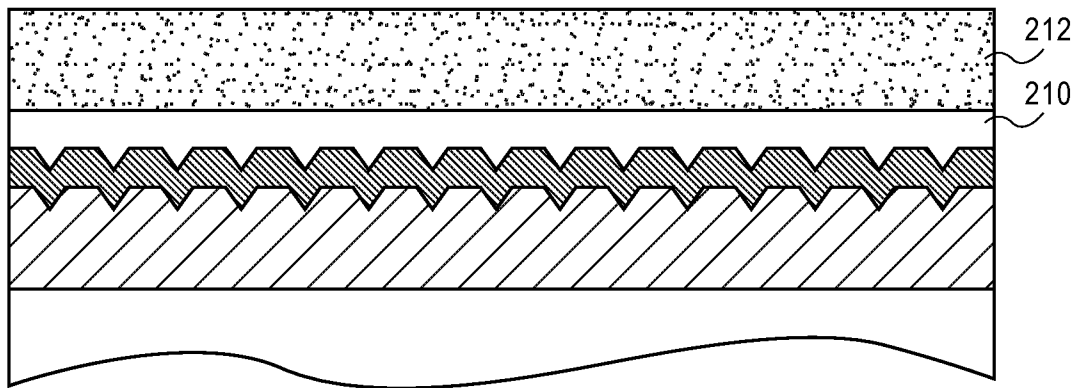
**FIG. 2A**



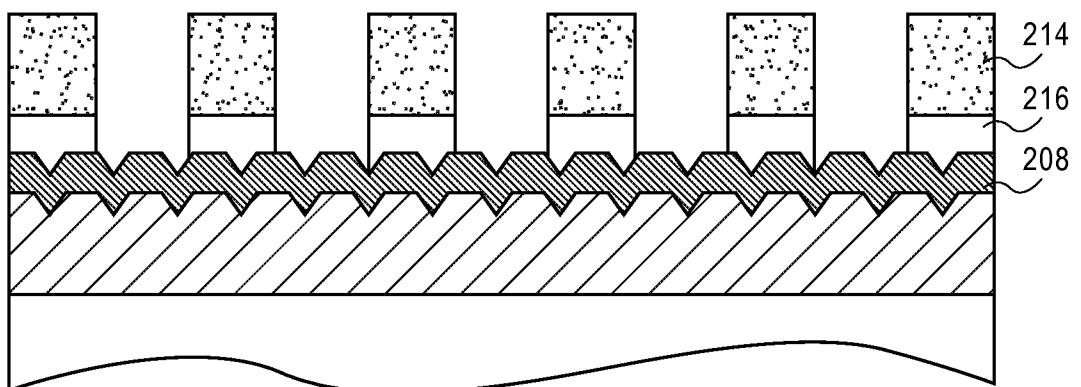
**FIG. 2B**



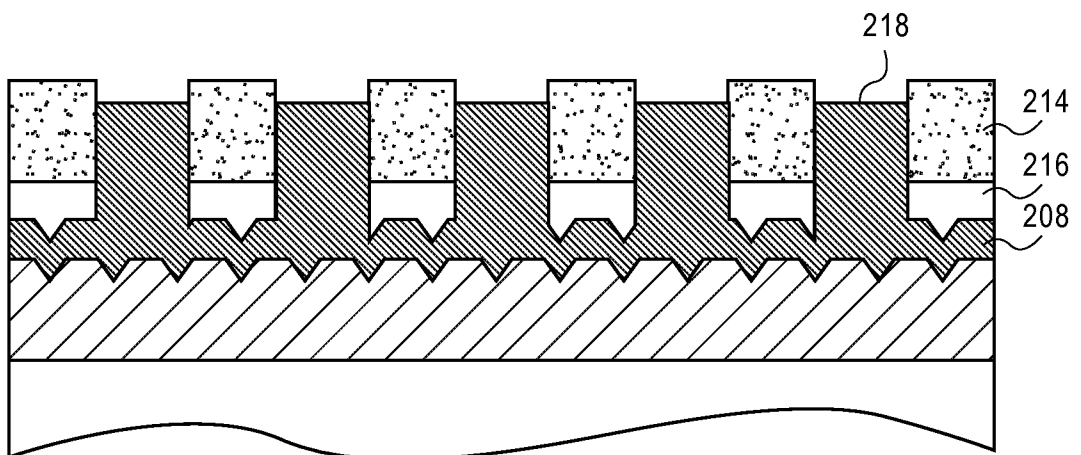
**FIG. 2C**



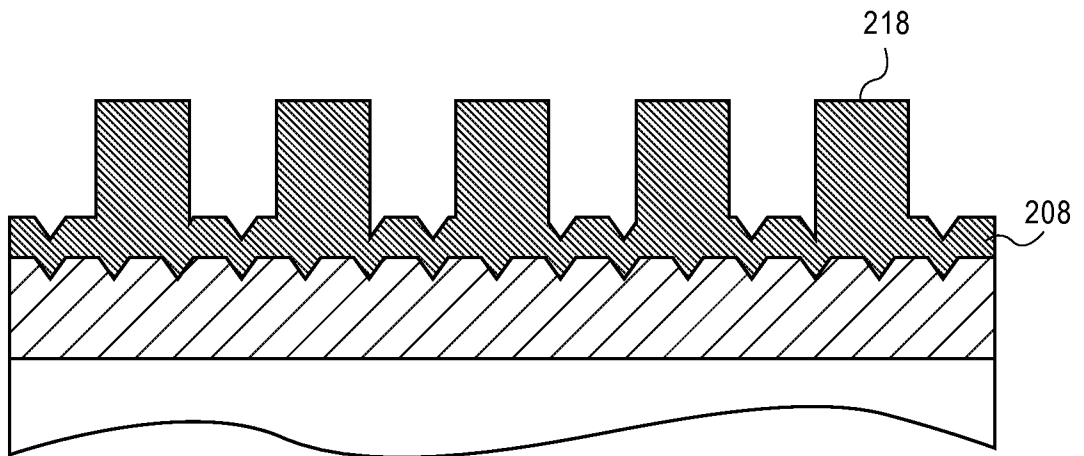
**FIG. 2D**



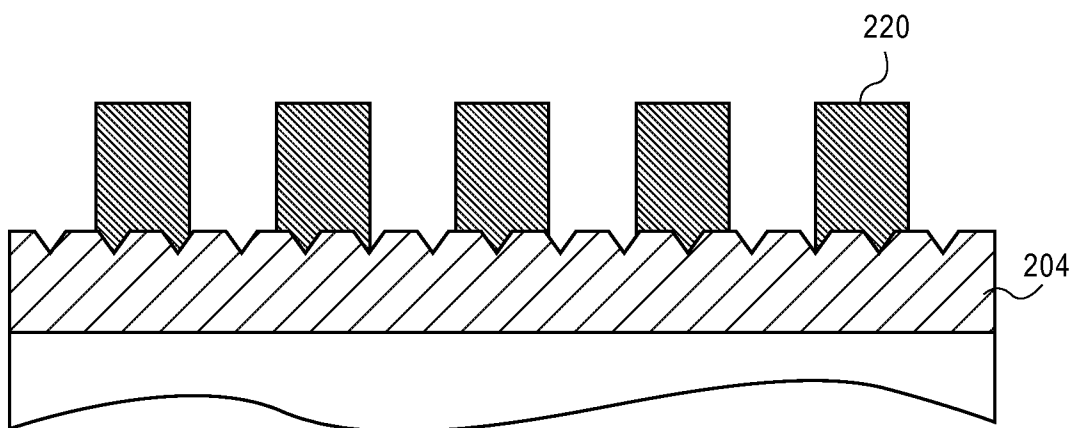
**FIG. 2E**



**FIG. 2F**



**FIG. 2G**



**FIG. 2H**