PARALLEL ANALOG-DIGITAL CONVERTER WITH DUAL STATIC LADDER

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ABSTRACT

The invention relates to fast, high resolution, analog digital converters, and more particularly those which possess at least one conversion stage of “flash” type. The converter according to the invention uses N differential amplifiers with four inputs. The amplifier of rank j receives the input voltage to be converted V_in−V_ref on two first inputs, and a reference potential difference on two other inputs. The reference potential difference is obtained between two taps of networks of resistors that are identical operating in parallel and supplied between a high voltage source and a low current source; the taps for an amplifier are respectively among a tap P_j of first network and a tap P_{j+1} of rank N−j−1 of a second network. This reduces the first and second order non-linearity effects due to the fact that the differential amplifiers consume an input current tapped off from the networks of resistors.

14 Claims, 3 Drawing Sheets
PARALLEL ANALOG-DIGITAL CONVERTER
WITH DUAL STATIC LADDER

CROSS-REFERENCE TO RELATED APPLICATIONS

The present Application is based on International Application No. PCT/EP2008/052989, filed on Mar. 13, 2008, which in turn corresponds to French Application No. Mar. 16, 2007, and priority is hereby claimed under 35 USC §119 based on these applications. Each of these applications are hereby incorporated by reference in their entirety into the present application.

FIELD OF THE INVENTION

The invention relates to fast analog digital converters, and more particularly those which possess at least one conversion stage of "flash" type, that is to say a parallel-structure stage in which the voltage to be converted is simultaneously compared with a series of reference voltages $V_j$ where $j$ is an index varying from 0 to N, all the potential differences $V_{j+1}-V_j$ being assumed identical and equal to a fixed elementary reference voltage $V_{ref}$.

BACKGROUND OF THE INVENTION

Such converters generally use a network of identical resistors $R$ in series supplied with a constant current $I_0$ so as to produce the reference voltages distributed at regular intervals of value $V_{ref}=R I_0$ and N differential amplifiers each associated with a respective reference voltage so as to determine whether the input voltage is greater or less than this reference voltage or to linearly amplify the disparity between the input voltage and this reference voltage. The junction points of the resistors constitute intermediate taps connected to the inputs of the amplifiers.

The simplest structure is that which is represented in FIG. 1 depicting a network of resistors in series $R_1$ to $R_N$, traversed by a fixed current $I_0$ and a set of differential amplifiers or comparators $A_1$ to $A_N$, the amplifier $A_j$ of rank $j$ receiving on the one hand the voltage $V_{in}$ to be converted, and on the other hand the voltage at the junction point of resistor $R_{j+1}$ and resistor $R_j$.

This structure can be used for a final analog-digital conversion stage, the amplifiers toggling in one direction or the other depending on the direction of the difference between the input voltage and the reference voltage. It can also be used as input stage or intermediate analog-digital conversion stage, followed by other conversion stages, and in this case each amplifier must provide, destined for the following stage, a voltage or a current varying linearly as a function of the difference between the input voltage $V_{in}$ and the reference voltage associated with this amplifier.

It is desired to be able to make converters having even greater linearity so as to be able to perform precise conversions with ever higher resolution. It is sought for example to make converters with 12 or 14 bit resolution. The linearity errors are due to the imperfections of the resistors which may have values that are not entirely identical; they are due also to the fact that even if the resistors are identical, the inputs of the amplifiers divert a part of the current which crosses the resistors so that the currents traversing the resistors on the top of the series are higher than the currents traversing the resistors on the bottom of the series. FIG. 1 schematically represents an input current $I_0$ diverted onto each amplifier input connected to the network of resistors. This current $I_0$ is in practice the base current of a bipolar input transistor of the amplifier. It follows from this that the potentials of the intermediate taps of the series network of resistors are not regularly distributed with voltage intervals $R I_0$ between two successive intermediate taps of the series of resistors. It may be reckoned that the overall non-linearity error is proportional to the square of the number of amplifiers, to the value of the elementary resistance $R$, and to the value of the input current $I_0$ consumed by each amplifier.

It is not possible to decrease R beyond certain limits for reasons of manufacturing precision and current consumption. The number N depends on the resolution desired for the stage, for example for 6-8 bits, for example N=64 for 6 bits. A minimum current $I_0$ is imposed by the dynamic performance of the differential amplifiers which must be able to work at high speed. It would be possible to use MOS technologies with low input current consumption but with these technologies it is difficult to achieve sufficient manufacturing precision to obtain the performance afforded by bipolar technologies.

Solutions involving current compensation have already been devised, wherein currents of value $I_{bc}$ are injected into the intermediate taps of the ladder of resistors so as to neutralize the loss of current $I_0$ to the amplifiers. These solutions are complex and very sensitive to temperature variations or to dispersion in the technological manufacturing parameters; this is because the problem is to compensate a base current which is directly related to the gain in current of the input transistor of the differential stage, but the value of the gain is highly dispersed and variable with temperature.

Inspiration could possibly be drawn from the differential structure described in patent application WO 2005/055431, which was devised for increasing the speed performance of converters. This structure, recalled in FIG. 2, uses differential amplifiers $A_1$ to $A_N$, with four inputs each; the amplifier $A_j$ of rank $j$ receives on the one hand on two first inputs the differential voltage to be converted $V_{ref}-V_{ref}$, and on the other hand on two other inputs the voltages sampled from two symmetric taps, of rank $j$ and $N-j+1$ respectively, of the network of resistors in series. Thus, the first amplifier $A_1$ is linked to the first intermediate tap $P_1$ and to the last $P_N$, the second is linked to the second tap $P_2$ and to the penultimate $P_{N-2}$, etc. With this structure, it would be possible to solve the problem engendered by this current $I_0$ diverted from each tap of the network of resistors, on account of the symmetry of the structure which establishes a natural compensation for this current. Indeed, what counts in this structure is not the linearity of distribution of the potentials of the taps $P_1$ to $P_N$, it is the linearity of the succession of potential differences between taps $P_j$ and $P_{N-j}$ when $j$ increases from 1 to N. Now, whatever $j$, the voltage drop between the taps $P_j$ and $P_{N-j}$ results from the addition of voltage drops in the resistors at the top of the set, traversed by bigger currents, and of voltage drops in the resistors at the bottom, traversed by smaller currents, so that on average the distribution of the voltage drops remains regular, even if the mean current in the resistors is not $I_0$, but would be desired in any case $I_0+N H I_0$.

Nevertheless, this compensation takes place only on condition that the current $I_0$ is independent of the input voltage $V_{ref}-V_{ref}$ to be converted. But this is not the case. It would be possible to correct matters so that this is the case by inserting a follower stage between each tap of the network and the input of the corresponding differential amplifier; but this would introduce additional problems of matching of circuits, of dispersion as a function of temperature, of additional current consumption, of noise introduced by the follower stage, and
of additional base-emitter voltage drop which is harmful if it is desired to work with a power supply at very low voltage such as 3.3 volts.

By way of example, a linearity error calculation simulation in the configuration of FIG. 2, for a 14-bit converter whose first stage comprises 80 differential amplifiers, leads to the conclusion that the integral non-linearity error over the conversion ladder may attain 7.5 LSB (least significant bit) in an example where the supply current to the network of resistors is 30 milliamperes, the differential pairs of the amplifiers have current supplies of 200 microamperes, and the mean base current is 1.7 microamperes. The integral non-linearity error INL is the aggregate sum of the differences between the theoretical values of the reference voltages and their actual values. These 7.5 least significant bits represent too big an error, which it is desired to reduce.

It has been noted that if the network of resistors of FIG. 2 was supplied between two reference voltage sources rather than between a high voltage source and a low current source, the integral non-linearity error was divided in a ratio of almost 2:5, which is considerable. Under the same measurement conditions, this leads to an integral non-linearity error of 3 LSB peak-to-peak for a 14-bit converter, which is much more satisfactory. Power supply through two reference voltages therefore improves performance.

Attempts have also been made to verify whether it was possible to further improve the integral non-linearity of the structure by using a double ladder of resistors in series supplied between two reference voltages, instead of a simple ladder supplied between two reference voltages; one of the inputs of the amplifier is then tapped on a tap of rank j of one of the ladders while the other input is tapped on a tap of rank N-j+1 of the other ladder. But the result is not conclusive since the same conditions as above lead to an integral non-linearity of 4.7 LSB. The double ladder of resistors is therefore useless from the point of view of the integral non-linearity since it impairs performance.

SUMMARY OF THE INVENTION

To improve the linearity of high-resolution analog digital conversion, notably conversion on more than 12 bits, the invention proposes an analog-digital converter comprising a network of N differential amplifiers of rank j=1 to N, each having four inputs, two inputs receiving a differential input voltage to be converted V_{in}-V_{ref}, the third and the fourth inputs receiving reference voltages arising from a set of resistors of identical nominal values R traversed by a current of nominal value I_o, the amplifier of rank j providing a voltage proportional to V_{in}-V_{ref}-K*R*I_o (K integer) when the differential input voltage V_{in}-V_{ref} is close to the voltage K*R*I_o, characterized in that the set of resistors comprises a first network of N resistors of value R in series connected on one side to a voltage source and on the other to a reference current source, the ends of the resistors defining N first taps of rank j=1 to N, and a second network of N resistors of value R in series on one side to the same voltage source as the first and on the other to a reference current source such that the two networks are supplied by identical currents, the resistors of the second network defining N second taps of rank j=1 to N, the amplifier of rank j having its third input linked to a tap of rank j of the first network and to a tap of rank N-j+1 of the second network.

The two networks are strictly identical. They are supplied by a common voltage source. A respective current source of value I_o can be provided in series with each network to impose the current which will traverse them. However it is more advantageous to provide a single common current source of double value 2I_o, simultaneously supplying the two (identical) networks, each of them then being traversed by half the current, namely a current I_o.

If it is desired to use N differential amplifiers for the conversion, provision may be made for the converter to comprise a number of amplifiers greater than N, the additional amplifiers being present solely to avoid edge effects. The networks of resistors then comprise more than N resistors each.

The integral non-linearity of the structure thus obtained turns out to be much better (in a ratio of about 30 to 50, which is considerable) than that obtained with the other structures tried. Although supplying power to a simple network with the aid of two reference voltages turns out to be markedly better than supplying power to a simple network through a voltage source and a current source, it has been found that an unexpected improvement of a much greater order of magnitude could be obtained by using a double network on condition that it is not supplied between two reference voltage sources.

Under the same measurement conditions as above, an integral non-linearity of 0.1 LSB peak-to-peak has been obtained for a 14-bit converter, i.e. 75 times better than a simple network supplied in the same manner, 30 times better than a simple network supplied by voltage references, and 50 times better than a double network supplied by voltage references.

Still other objects and advantages of the present invention will become readily apparent to those skilled in the art from the following detailed description, wherein the preferred embodiments of the invention are shown and described, simply by way of illustration of the best mode contemplated for carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious aspects, all without departing from the invention. Accordingly, the drawings and description thereof are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF DRAWINGS

The present invention is illustrated by way of example, and not by limitation, in the figures of the accompanying drawings, wherein elements having the same reference numeral designations represent like elements throughout and wherein:

FIG. 1 represents a flash analog-digital converter principle of the prior art;

FIG. 2 represents another flash converter principle of the prior art;

FIG. 3 represents a flash conversion structure according to the invention;

FIG. 4 represents an alternative structure according to the invention;

FIG. 5 represents a folded construction of the networks of resistors;

FIG. 6 represents an exemplary differential amplifier embodiment with four inputs.

DESCRIPTION OF PREFERRED EMBODIMENTS

The structure of the converter of FIG. 3 uses N differential amplifiers with four inputs similar to those which are used in FIG. 2. Each differential amplifier A_i of rank j, where j varies from 1 to N, possesses two first inputs receiving the differential voltage to be converted V_{in}-V_{ref}. A voltage V_{ref} is therefore applied to a first input of all the differential amplifiers, and a voltage V_{ref} is applied to a second input of all the differential amplifiers.
A reference potential difference, different for each amplifier, is applied between the third and the fourth input. This potential difference is established on the basis of taps of two distinct networks of resistors, one network dedicated to the application of a reference potential to the third input, the other dedicated to the application of another reference potential to the fourth input. In FIG. 2, a single reference network was used.

The two networks of resistors are identical and traversed by identical currents I_{rj} defined by current sources. They each comprise at least N-1 identical resistors, of value R, in series, and the ends of these N-1 resistors define N taps intended to be linked to the inputs of the amplifiers. Thus, the tap P_j of rank j is the junction point of the resistor R_j of the current source I_{rj}.

For the first network, the taps are denoted P_j to P_{N-1} and the resistors R_j to R_{N-1}. For the second network, “prime” indices are used: taps P'_1, P'_2, ..., P'_{N-1}.

The increasing direction of the indices from 1 to N is taken by convention in the direction of flow of the current in the networks, that is to say, when referring to the figure, the indices increase from top to bottom for the two networks which are both traversed by a current flowing from top to bottom (supply potential VH more positive at the top than at the bottom). The two networks are connected on one side to a voltage source which defines the supply potential VH. On the other side, the networks are connected to a current source in a manner such that they are traversed by identical currents.

According to the invention, the tap P_j of rank j of the first network is linked to the third input of the amplifier A_j and the tap P'_{N-j+1} of rank N-1 of the second network is linked to the fourth input of the amplifier A_j. This is so for all ranks j.

The potential difference between these two taps constitutes a reference voltage K_{rj} for the differential amplifier A_j which provides at its output a voltage proportional to the disparity between the input voltage to be converted and this reference voltage when the input voltage is close to this reference voltage. The reference potential differences K_{rj} are regularly strung out between -(N-1)R-I_{rj} and +(N-1)R-I_{rj} at intervals 2R-I_{rj}.

The integer K is in practice equal to N-2j+1 for amplifier A_j.

It will be noted that, by comparison with FIG. 2 and to have the same resolutions and ranges of reference voltage as in FIG. 2, the value of the resistance R used in the networks of FIG. 3 will be double that of FIG. 2, and the value of the current I_{rj} will be half that of FIG. 2.

It has been observed according to the invention not only that the first-order non-linearity error, due to the existence of the currents I_{rj} drawn off by each amplifier input, is corrected in the same manner as in the case of FIG. 2, but also that the second-order non-linearity errors, due to the fact that the current I_{rj} varies according to the level of the input voltage V_{i,j}-V_{o,j}, tend to compensate one another. It will be noted that the input currents I_{rj} of all the third inputs of the amplifiers are drawn off from one of the networks while the currents I_{rj} of all the fourth inputs are drawn off from the other network.

A simulation analogous to that which was indicated above for the case of FIG. 2 has made it possible to observe an integral non-linearity error as low as 0.1 LSB, i.e. much less than previously, under the same conditions.

In the layout of FIG. 2, it has been considered that the two networks of resistors are supplied independently by two different current sources of the same value I_{rj} disposed at the foot of the networks, through foot resistors R_{fj} and R'_{fj}, the head of the networks being supplied by the same supply voltage source VH. However, provision may advantageously be made for a single current source of double value 2xI_{rj} to supply both the two networks in parallel. The head is still supplied by a voltage source VH common to the two networks. The current is divided into two equal parts of value I_{rj} since the networks are identical, but a further improvement in the second-order non-linearity error is observed.

In the foregoing it has been considered that there was a network of N amplifiers with N voltage taps of a network of N-1 resistors. The number N represents the number of conversion spans produced by the stage. For example, if the stage has to establish the 6 high-order bits of a conversion, there will be N=64 amplifiers which will deliver voltages that vary as a function of the input voltage, this voltage being used in following conversion stages to establish the low-order bits of the conversion. These following stages can be structures with folding amplifiers or other types of structures.

But even if the first stage has to establish only N conversion spans, it may be useful to make provision for there to be a larger number of amplifiers and a larger number of resistors extending the networks of FIG. 3 or 4 upwards and downwards. These additional resistors and amplifiers serve to avoid edge effects which would tend to impair the linearity towards the ends of the conversion span. It is thus possible to add several tens of amplifiers and resistors on each side of the network of N useful resistors and amplifiers.

Finally, the networks of resistors stretch over a fairly large length on an integrated circuit microchip, for example 1 millimeter; now, over such a distance, the effects of thermal gradients or of technological dispersion may make themselves felt. It is advantageous under these conditions to decompose each resistor into two resistors in parallel but these two resistors being placed symmetrically with respect to the middle of the network in such a way that the temperature gradients compensate one another. FIG. 5 represents such a configuration of the networks of resistors. The resistors R_1, R_2, R_3 of the previous figures are each made up here of resistors in parallel, R_{11}, R_{12}, R_{13}, R_{21}, R_{22}, R_{23}, make up the resistor R_1, R_{21}, R_{22}, make up the resistor R_2, etc.

Given that the structure of the invention comprises networks of resistors supplied by a continuous voltage and continuous current and not by the input voltage to be converted (so-called static network or ladder of resistors, unlike other dynamic-ladder structures where it is the input voltage which is applied to the network), it is advantageous to decouple this network by capacitors each connected between a tap of the network and ground (or a terminal at fixed potential). This decoupling avoids disturbances to the reference voltages by dynamic signals such as the clock signals of sample and hold modules, or even the input signals to be converted which could be coupled by stray capacitances to the network of resistors. The added capacitances short-circuit these stray signals. It will be noted that this decoupling also reduces the thermal noise engendered by the resistors.

FIG. 6 represents an exemplary detailed make-up of a differential amplifier A_j usable in the structure of the invention. The amplifier has four inputs receiving the input signals to be converted and the voltages present on the taps P_j and P'_{N-j+1}. It is made in the form of a double amplifier composed of two simple differential transconductance amplifiers whose outputs are crossed to produce a voltage proportional to the difference between the input voltage of the first and the input voltage of the second. The assembly then produces a voltage proportional to V_{o,j} - V_{o,j} - K R I_{rj} when the voltage V_{o,j} - V_{o,j} is close to K R I_{rj}. The term K R I_{rj} represents the potential difference between the taps P_j and P'_{N-j+1}.

The first amplifier (on the left) receives the voltage V_{o,j} on input (which is the first input of the amplifier A_j) and the
The second amplifier (on the right) receives the voltage $V_{op}$ on one input (which is the second input of the amplifier $A_j$) and the voltage present on the tap $P_j$ on another input (which is the third input of $A_j$).

The current outputs of the amplifiers are joined so as to act as a summer; by crossing the outputs a difference is effected, so that the outputs provide a differential voltage representing, with a coefficient corresponding to the gain of the amplifier, the difference of the voltage differences applied to the inputs taken pairwise. This difference represents the quantity:

$$V_{op} - V_{in} = K \cdot R \cdot I_0$$

More precisely, each simple differential amplifier comprises two symmetric branches supplied by the current of a single constant current source, each branch comprising a transistor in series with a load resistor $R_{load}$. The bases of the transistors are the inputs of the amplifiers. The first amplifier receives $V_{in}$ on the base of the first transistor $T_1$ and receives the tap $P_{N-j+1}$ on the base of the second transistor $T_2$. The second amplifier receives $V_{in}$ on the base of the first transistor $T_1$ and receives the tap $P_j$ on the base of the second transistor $T_2$. The outputs are arranged summator fashion but crossed: the output constituted by the collector of $T_1$ is linked to the output constituted by the collector of $T_2$ so as to constitute a first output of the double differential amplifier, and vice versa the collectors of $T_1$ and $T_2$ are linked to constitute a second output of the double differential amplifier. The output of the differential amplifier is constituted by one of these outputs, for example the collector of $T_1$ if the output of the amplifier is a simple output, or by the two outputs (collectors of $T_1$ and $T_2$) if the output of the amplifier must be differential. The currents of the current sources are identical and the transistors and resistors of the layout are all identical.

It will be readily seen by one of ordinary skill in the art that the present invention fulfills all of the objects set forth above. After reading the foregoing specification, one of ordinary skill in the art will be able to affect various changes, substitutions of equivalents and various aspects of the invention as broadly disclosed herein. It is therefore intended that the protection granted hereon be limited only by definition contained in the appended claims and equivalents thereof.

The invention claimed is:

1. An analog-digital converter comprising a network of $N$ differential amplifiers of rank $j=1$ to $N$, each having four inputs, two inputs receiving a differential input voltage to be converted $V_{op} - V_{in}$, the third and the fourth inputs receiving reference voltages arising from a set of resistors of identical nominal values $R$ traversed by a current of nominal value $I_0$, the amplifier of rank $j$ providing a voltage proportional to $V_{op} - V_{in} = K \cdot R \cdot I_0$, when the differential input voltage $V_{op} - V_{in}$ is close to a voltage value $K \cdot R \cdot I_0$,

wherein

- the set of resistors comprises a first network of $N$ resistors of value $R$ in series connected on one side to a constant voltage source and on the other to a constant reference current source, the ends of the resistors defining $N$ first taps of rank $j=1$ to $N$,

- a second network of $N$ resistors of value $R$ in series connected on one side to the said constant voltage source and on the other to another constant reference current source or the constant reference current source such that the two networks are supplied by identical currents, the resistors of the second network defining $N$ second taps of rank $j=1$ to $N$, and

2. The converter as claimed in claim 1, wherein a respective current source of value $I_0$ is provided in series with each network to impose the current which will traverse them.

3. The converter as claimed in claim 1, wherein a current source of value $2I_0$ is designed to supply the set of the two networks, each of them then being essentially traversed by half the current, namely a current $I_0$.

4. The converter as claimed in claim 1, producing $N$ useful output voltages on converters comprising a number of amplifiers and resistors greater than $N$, the additional amplifiers and resistors being present solely to avoid edge effects.

5. The converter as claimed in claim 1, wherein a decoupling capacitor is connected between each tap of the network and a terminal at fixed potential.

6. The converter as claimed in claim 2, wherein a current source of value $2I_0$ is designed to supply the set of the two networks, each of them then being essentially traversed by half the current, namely a current $I_0$.

7. The converter as claimed in claim 2, producing $N$ useful output voltages on conversion, comprising a number of amplifiers and resistors greater than $N$, the additional amplifiers and resistors being present solely to avoid edge effects.

8. The converter as claimed in claim 3, producing $N$ useful output voltages on conversion, comprising a number of amplifiers and resistors greater than $N$, the additional amplifiers and resistors being present solely to avoid edge effects.

9. The converter as claimed in claim 2, wherein each of the networks of resistors has a configuration in which each resistor is formed of two resistors in parallel, placed symmetrically with respect to the middle of the network.

10. The converter as claimed in claim 3, wherein each of the networks of resistors has a configuration in which each resistor is formed of two resistors in parallel, placed symmetrically with respect to the middle of the network.

11. The converter as claimed in claim 2, wherein a decoupling capacitor is connected between each tap of the network and a terminal at fixed potential.

12. The converter as claimed in claim 3, wherein a decoupling capacitor is connected between each tap of the network and a terminal at fixed potential.

13. An analog-digital converter comprising:

- a first network of resistors in series coupled on one side to a voltage source and on the other to a first reference current source, the resistors of the first network of resistors defining $N$ first taps of rank $j=1$ to $N$, and each resistor having resistance of a predetermined value $R$ and being supplied with current of a predetermined value $I_0$;

- a second network of resistors having $N$ resistors in series coupled on one side to the voltage source and on the other to a second reference current source, the resistors of the second network of resistors defining $N$ second taps of rank $j=1$ to $N$, and each resistor having resistance of the predetermined value $R$ and being supplied with current of the predetermined value $I_0$; the first and second reference current sources being arranged for supplying the first and second networks of resistors with identical amount of current;
a network of amplifiers having \( N \) differential amplifiers of rank \( j = 1 \) to \( N \), each amplifier being configured to receive a pair of input signals \( V_{ep} \) and \( V_{en} \) and to provide an output signal responsive to \( V_{ep} - V_{en} - K \cdot R \cdot I_o \), \( K \) being \( N-2j+1 \), and having four inputs:

a first and second inputs of the four inputs being arranged for receiving the pair of input signals \( V_{ep} \) and \( V_{en} \);

a third input of the amplifier of rank \( j \) being connected to a tap of rank \( j \) of the first network of resistors, and

a fourth input of the amplifier of rank \( j \) being connected to a tap of rank \( N-j+1 \) of the second network of resistors,

wherein each of the networks of resistors has a configuration in which each resistor is formed of two resistors in parallel, placed symmetrically with respect to the middle of the network.

14. An analog-digital converter comprising:

a first network of resistors having \( N \) resistors in series coupled on one side to a voltage source and on the other to a reference current source, the resistors of the first network of resistors defining \( N \) first taps of rank \( j = 1 \) to \( N \), and each resistor having resistance of a predetermined value \( R \) and being supplied with current of a predetermined value \( I_o \);

a second network of resistors having \( N \) resistors in series coupled on one side to the voltage source and on the other to the reference current source, the resistors of the second network of resistors defining \( N \) second taps of rank \( j = 1 \) to \( N \), and each resistor having resistance of the predetermined value \( R \) and being supplied with current of the predetermined value \( I_o \), the reference current source being arranged for supplying the first and second networks of resistors with identical amount of current; and

a network of amplifiers having \( N \) differential amplifiers of rank \( j = 1 \) to \( N \), each amplifier being configured to receive a pair of input signals \( V_{ep} \) and \( V_{en} \) and to provide an output signal responsive to \( V_{ep} - V_{en} - K \cdot R \cdot I_o \), \( K \) being \( N-2j+1 \), and having four inputs:

a first and second inputs of the four inputs being arranged for receiving the pair of input signals \( V_{ep} \) and \( V_{en} \);

a third input of the amplifier of rank \( j \) being connected to a tap of rank \( j \) of the first network of resistors, and

a fourth input of the amplifier of rank \( j \) being connected to a tap of rank \( N-j+1 \) of the second network of resistors,

wherein each of the networks of resistors has a configuration in which each resistor is formed of two resistors in parallel, placed symmetrically with respect to the middle of the network.