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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: **KARPOV, Elijah V.**; 4386 Lakeshore Drive, Santa Clara, California 95054 (US). **SHAH, Uday**; 13409 NW Keeton Park Lane, Portland, Oregon 97229 (US). **MAJHI, Prashant**; 1754 Indigo Oak Lane, San Jose, California 95121 (US). **MUKHERJEE, Niloy**; 16781 NW Vetter Drive, Portland, Oregon 97229 (US). **PILLARISETTY, Ravi**; 925 NW Hoyt Street, Apt. 226, Portland, Oregon 97209 (US).

(74) Agents: **RICHARDS, II, E.E. "Jack"** et al.; Trop, Pruner & Hu, P.C., 1616 S. Voss Rd., Ste. 750, Houston, Texas 77057-2631 (US).

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(54) Title: THERMALLY INSULATED RESISTIVE RANDOM ACCESS MEMORY

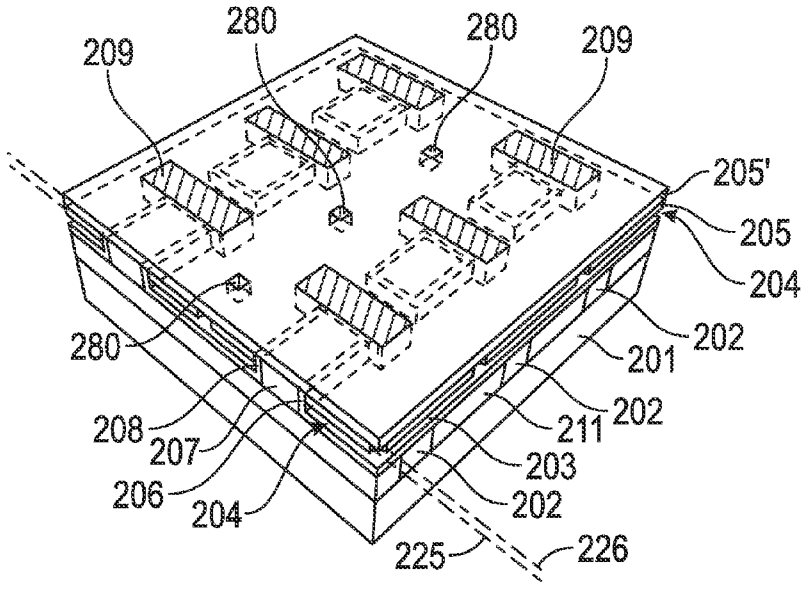

FIG. 3N

(57) Abstract: An embodiment includes a resistive random access memory (RRAM) comprising: a top electrode portion and a bottom electrode portion; and an oxide layer between the top and bottom electrode portions; wherein (a) a conductive filament is within the oxide layer and is adjacent the top electrode portion, (b) the oxide layer includes oxide layer sidewalls, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is parallel to the oxide layer sidewalls, and (d) a void, which includes air, is adjacent the oxide layer sidewalls. Other embodiments are described herein.

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Thermally Insulated Resistive Random Access Memory

Technical Field

[0001] Embodiments of the invention are in the field of semiconductor devices and, in particular, non-volatile memory.

Background

[0002] Resistive random access memory (RRAM or ReRAM) relies on a class of materials that switch in a one-time event from a virgin insulating state to a low resistive state by way of a “forming” event. In the forming event, the device goes through “soft breakdown” in which a localized filament forms in a dielectric layer located between two electrodes. This filament shunts current through the filament to form a low resistance state. The RRAM switches from a low to a high resistive state (by disbanding the filament) and from a high to a low resistive state (by reforming the filament) by applying voltages of different polarities to the electrodes to switch the state. Thus, conventional RRAM can serve as a memory.

Brief Description of the Drawings

[0003] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

Figure 1 includes a conventional RRAM stack;

Figure 2A includes a perspective view of a RRAM memory array in an embodiment of the invention. Figure 2B includes a top view of a portion of the RRAM memory array in an embodiment of the invention;

Figures 3A-3N include a method of forming an RRAM memory array in an embodiment of the invention; and

Figure 4 includes a system including an embodiment of an RRAM memory array.

Detailed Description

[0004] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of semiconductor/circuit structures. Thus, the actual appearance of the fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. For example, not every layer of a semiconductor device is necessarily shown. “An embodiment”, “various embodiments” and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. “First”, “second”, “third” and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. “Connected” may indicate elements are in direct physical or electrical contact with each other and “coupled” may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

[0005] Figure 1 includes a conventional RRAM stack 100 including top electrode 101, oxygen exchange layer (OEL) 111 (e.g., Hf, Ti, and the like), oxide 121 (e.g., HfOx), and bottom electrode 131. Oxygen vacancies 144 have a higher concentration in region 141 and a relatively lower concentration in region 142. The vacancies collectively form a filament that serves as a memory. As addressed above, a “soft breakdown” occurs whereby, for example, an anneal takes place such that oxygen is scavenged by OEL 111 thereby producing vacancies 144. The vacancies cluster near the OEL/oxide interface (interface between layers 111 and 121) because that is where the scavenging takes place. Biasing electrodes 101, 131 with one polarity may purposely remove vacancies in area 143 to disband or disrupt

the filament and create a high resistance state (a “0” memory state). Reversing the bias to electrodes 101, 131 with an opposite polarity may reform vacancies in area 143 to reform the filament and create a low resistance state (a “1” memory state).

[0006] However, sometimes the “0” and “1” memory states are not “retained” because the vacancies may disband or otherwise fail to retain their initially programmed configuration (e.g., fail to remain a filament that represents relatively low resistance) when exposed to extreme thermal stress. Specifically, the temperature for the filament can approach almost 500 degrees C during a write operation of a “0” or “1” to the RRAM cell including the filament. Consequently, writing to one RRAM cell may cause a 500 degree C environment that “leaks” to an adjacent cell. The adjacent cell (which was not being written to) may then fail to retain its desired memory state due to thermal stress from the writing of the neighboring cell. As such, any memory based on stack 100 is unstable—a quality undesirable for non-volatile memories (NVMs).

[0007] As described herein, Applicant has addressed this retention issue. By properly designing the RRAM cell’s thermal environment, Applicant has minimized thermal disturbances from a first RRAM cell to a second neighboring RRAM cell by reducing heat leaks from the first cell to the second cell. To reduce the heat leaks an embodiment uses an air gap substantially surrounding the first cell and/or an air gap substantially surrounding the second cell.

[0008] Figure 2a includes an RRAM memory array in an embodiment of the invention. Specifically, Figure 2a includes a memory 200 comprising: a top electrode portion 209 and a bottom electrode portion 202; and an oxide layer 207 between the top and bottom electrode portions. Electrode “portion” is used because, for example, portion 202 may be a part of a larger electrode. A conductive filament is within the oxide layer 207 and is adjacent the top electrode 209 in a manner similar to how a filament comprised of oxygen vacancies 144 is adjacent top electrode 101 in Figure 1. However, not all embodiments require an OEL 111 or that the filament be comprised of oxygen deficiencies. Instead, the filament may be formed of metal portions that, for example, migrate out or otherwise are derived from a metal layer where OEL 111 is seen in Figure 1. Embodiments broadly include resistive

switching memories, which include, without limitation, oxide vacancy filament RRAM, conductive bridging RAM (CBRAM), phase change memory (PCM) RAM, and interfacial switching RRAM. Such examples of RRAM have a thermal component to be managed. Not all RRAM require forming events and embodiments include such RRAMs.

[0009] Returning to Figure 2A, oxide layer 207 includes oxide layer sidewalls 212, 213. In an embodiment these two sidewalls may be orthogonal to each other. A vertical axis 221 intersects the oxide layer 207 and the top and bottom electrode portions 209, 202 and is parallel to the oxide layer sidewalls 212, 213. As used herein, "parallel" is to be considered as it would by a person of ordinary skill in the art. For example, sidewall 212 may have some slant due to etching and general processing so it may not be 100% parallel with a hypothetical vertical axis that is not subject to real world semiconductor processing. Void 204, which includes air, is adjacent the oxide layer sidewalls 212, 213.

[0010] In an embodiment (but not all embodiments) the void 204 surrounds the oxide layer 207 (see Figure 2B) and does not intersect the vertical axis 221. Thus, "surrounds" does not necessarily mean that the void must also extend around top and bottom surfaces of the oxide layer. A horizontal axis 222, orthogonal to the vertical axis 221, intersects the void 204 and the oxide layer 207.

[0011] Some embodiments, but not necessarily all embodiments, include an OEL 214 between the oxide layer 207 and the top electrode 209. As seen in Figure 2A, the void 204 surrounds OEL 214 and an additional horizontal axis 223, orthogonal to the vertical axis 221, intersects the void 204 and the OEL 214. In some embodiments OEL 214 directly contacts the oxide layer 207. In some embodiments, OEL 214 may be substituted with a layer containing a metal (or derivatives thereof) that may form the conductive filament in the resistive memory. As indicated above, embodiments include many forms of RRAM, such PCM RRAM, and the like. Also, an OEL is not the only sublayer that may be included between top and bottom electrodes. Many such sublayers not specifically addressed herein may be included between the electrodes or even within the electrodes themselves.

[0012] As seen in Figure 2B, void 204 is ring-shaped or could also be referred to a having a horizontal cross section in the shape of a loop, hoop, hallo, or band. The ring-shaped void may have a cross section that is square, rectangular, circular, ovular, and the like. As seen in Figure 2B, the ring may be continuous and uninterrupted throughout its horizontal cross section. However, in other embodiments there may be small walls or other structures that do not provide a continuous uninterrupted loop in the void horizontal cross-section and such embodiments may still provide adequate thermal isolation between adjacent memory cells. For example, in an embodiment the void includes a cross section that is in a plane that is coplanar with the horizontal axis, and continuous and uninterrupted along its entire outermost perimeter that extends 360 degrees around the oxide layer. Such an embodiment is shown in Figure 2B. Note the outermost perimeter need not be straight or curved along a continuous arc of curvature. Such an embodiment does not include, for example, a crescent shaped structure where the tips of the crescent would not satisfy a continuous and uninterrupted outermost perimeter due to the space between the tips of the crescent. Some embodiments (event though not shown herein) include such a structure (a structure that has varying thicknesses in the horizontal plane and an interrupted space).

[0013] As seen in Figure 3N (addressed further below), the void 204 is not above the top electrode 209 and the void is not below the bottom electrode 202. However, in other embodiments the void may be taller in the vertical direction and may be above the oxide layer 207 and between top electrodes 209, 209' as seen in Figure 2A. In still other embodiments (not shown) the void may extend above the top electrode 209 and/or below bottom electrode 202.

[0014] Figure 2A shows an additional top electrode portion 209' and an additional bottom electrode portion 202'. An additional oxide layer 207' is between the additional top and bottom electrode portions 209', 202'. An additional conductive filament (not shown) is within the additional oxide layer 207'. The additional oxide layer 207' includes additional oxide layer sidewalls 212', 213'. An additional vertical axis 221' intersects the additional oxide layer 207', and the additional top and bottom electrode portions 209', 202' and is parallel to the additional oxide layer sidewalls

212', 213'. An additional void 204', which includes air, is adjacent the additional oxide layer sidewalls 212', 213'. As seen in Figure 2B, void 204 directly contacts (i.e., coalesces with) the additional void 204'. In other words, in the embodiment of Figure 2B there is no material structure between oxide portions 207, 207' along axis 222.

[0015] In an embodiment the additional void 204' surrounds the additional oxide layer 207' and does not intersect the additional vertical axis 221', and the horizontal axis 222 intersects the additional void 204' and the additional oxide layer 207'.

[0016] As seen in Figure 3M, addressed further below, an embodiment includes a barrier layer 203 between the void 204 and the oxide layer 207. The barrier layer 203 intersects horizontal axis 225 at vertical reaching barrier portions 206, 208 (both contacting portion 207). Axis 225 intersects portions 204, 206, 208. In an embodiment the barrier layer 203 directly contacts the void 204 and the oxide layer 207 but that is not the case in other embodiments.

[0017] As further seen in Figure 3M, in an embodiment the barrier layer 203 directly contacts a dielectric layer 205. Barrier layer 203 may be between the oxide layer 207 and the dielectric layer 205. In such a case an additional horizontal axis 226 may intersect the oxide layer 207, the barrier layer 203, and the dielectric layer 205. Axis 226 is above portion 104.

[0018] As seen in Figure 3N, in an embodiment an additional horizontal axis 227 intersects the top electrode 209 and the dielectric layer 205.

[0019] As seen in Figure 2A, in an embodiment void 204 surrounds the top electrode 209, and another horizontal axis 224 intersects the void and the top electrode.

[0020] Functionally, the embodiment of Figure 2A operates by having a first state when energy is applied to the top electrode 209 at a first polarity so the filament has a first electrical resistance (e.g., a "0" state); and in a second state when energy is applied to the top electrode at a second polarity, which is opposite the first polarity, so the filament has a second electrical resistance (e.g., a "1" state) that is greater than the first electrical resistance. Thus, the filament may not completely reach to

layer 202, thereby causing the higher resistivity. Having infinite or no electrical resistance is still considered a “resistance” as that term is used herein.

[0021] In an embodiment oxide layer 207 includes at least one of HfO2, SiO2, Al2O3,TiO2, SrTiO3, Cr-SrTiO3, NiO, CuOx, ZrO2, Nb2O5, MgO, Fe2O3, Ta2O5, ZnO, CoO, CuMnOx, CuMoOx, InZnO, Cr-SrZrO3, PrCaMnO3, SrLaTiO3, LaSrFeO3, (Pr,Ca)MnO3, Nb-SrTiO3, and LaSrCoO3. As used herein, SiOx is shorthand for a silicon oxide such as SiO_2.

[0022] In an embodiment, a system (such as the system of Figure 4) comprises a processor; a memory (e.g., any of the memory arrays or stacks described herein), coupled to the processor, and a communication module (e.g., radio and/or antenna), coupled to the processor, to communicate with a computing node external to the system.

[0023] Figures 3a-3n include a method of forming an RRAM memory array in an embodiment of the invention.

[0024] In Figure 3A material for a lower electrode 202 is formed adjacent dielectric 211 and on substrate 201. Figure 3B discloses formation of cells embodied by oxide layer 207. These cells will eventually include conductive filaments that serve as memory cells in an RRAM array. Such cells include oxide layers 207 and possibly OEL layers in some embodiments. In Figure 3C a barrier layer 203 is formed and then in Figure 3D interlayer dielectric (ILD) 205 is formed. Planarization occurs in Figure 3E until the cells are exposed in Figure 3F. ILD 205 is then recessed exposing barrier layer 203 in Figure 3G. A second ILD 205’ is then formed in Figure 3H until devices 207 are again exposed in Figure 3I.

[0025] In an embodiment, via lithography is performed with the use of an anti-reflective layer to align the vias between the active devices. Via holes 230, 231 are then patterned/etched in Figure 3J to gain access to ILD 205. In Figure 3K ILD 205 is removed via wet etch. As a result, void 204 is formed. Having completed their role, the via holes are then filled with dielectric 205’ in Figure 3L and the top surface oxide is planarized. Another lithography step is utilized to align via holes to contact the devices. Holes 209’’ are made for eventual top electrodes in Figure 3M. In an

embodiment care is taken to not go through layer 203 during the via etch otherwise potential shorting can occur. Then, in Figure 3N top electrodes 209 are formed by depositing fill metal and polishing. Also, a final lithography step is employed to make holes 280 contact with bottom electrodes 202. The via etch, this time, may completely remove portions of layer 203 in order to contact the bottom electrodes 202. These vias 280 will also be subsequently filled with contact metal and polished. Additional processing and layers may be added atop the top surface of Figure 3N and the additional processing is not addressed here. At some point an anneal is performed to generate vacancies to aid in the filament formation step. Some embodiments may include devices, such as the device of Figure 3N, before filament formation occurs.

[0026] Embodiments described herein improve the reliability of filamentary based RRAM memory and makes the memory more suitable for, as an example, embedded nonvolatile memory (eNVM).

[0027] In an embodiment OEL 214 includes a metal such as one or more of the following: Copper (Cu), Hafnium (Hf), Titanium (Ti), Ruthenium (Ru), Aluminum (Al), and Silver (Ag). In an embodiment, a second oxide layer 254 (between OEL 214 and the bottom electrode) may include at least one of HfSiOx, HfAlOx, SiO_2, MgOx, LaAlOx, LaSiOx, and GdSiOx. In an embodiment the oxide layer 207 includes at least one of HfO_2, SiO_2, Al_2O_3,TiO_2, $SrTiO_3$, Cr-$SrTiO_3$, NiO, CuOx, ZrO_2, Nb_2O_5, MgO, Fe_2O_3, Ta_2O_5, ZnO, CoO, CuMnOx, CuMoOx, InZnO, Cr-$SrZrO_3$, $PrCaMnO_3$, $SrLaTiO_3$, $LaSrFeO_3$, (Pr,Ca)MnO_3, Nb-$SrTiO_3$, and $LaSrCoO_3$. In an embodiment top electrode 209 includes at least one of Hf, Ti, Ta, Pd, W, Mo, and Pt and the bottom electrode 202 includes at least one of Hf, Ti, Ta, Pd, W, Mo, and Pt. Additionally, electrodes 209, 202 may include multiple layers of materials with differing properties.

[0028] Various embodiments disclosed herein have addressed RRAM cells. Any such RRAM cell may be used in a memory cell by coupling one portion or node of the cell (e.g., top electrode of Figure 2A) to a bit-line and another node of the stack (e.g., bottom electrode of Figure 2A) to a source or drain node of a switching device, such as a selection transistor. The other of the source and drain node of the

selection transistor may be coupled to a source line of the memory cell. The gate of the selection transistor may couple to a word-line. Such a memory cell may utilize resistance to store memory states. Embodiments provide smaller and more power efficient and yet still reliable memory cells that can be scaled below, for example, 22 nm CD. The RRAM cell may couple to a sense amplifier. A plurality of the RRAM memory cells may be operably connected to one another to form a memory array, wherein the memory array can be incorporated into a NVM device. It is to be understood that the selection transistor may be connected to the top electrode or the bottom electrode of a RRAM cell.

[0029] Figure 4 includes a system that may include any of the above described embodiments. Figure 4 includes a block diagram of a system embodiment 1000 in accordance with an embodiment of the present invention. System 1000 may include hundreds or thousands of the above described memory cells/stacks (stack 200 of Figure 2A) and be critical to memory functions in system 1000. System 1000 may be included in, for example, a mobile computing node such as a cellular phone, smartphone, tablet, Ultrabook®, notebook, laptop, personal digital assistant, and mobile processor based platform. The stability and power efficiency of such memory cells accumulates when the memory cells are deployed in mass and provides significant performance advantages (e.g., longer memory state storage in a broader range of operating temperatures) to such computing nodes.

[0030] Shown is a multiprocessor system 1000 that includes a first processing element 1070 and a second processing element 1080. While two processing elements 1070 and 1080 are shown, it is to be understood that an embodiment of system 1000 may also include only one such processing element. System 1000 is illustrated as a point-to-point interconnect system, wherein the first processing element 1070 and second processing element 1080 are coupled via a point-to-point interconnect 1050. It should be understood that any or all of the interconnects illustrated may be implemented as a multi-drop bus rather than point-to-point interconnect. As shown, each of processing elements 1070 and 1080 may be multicore processors, including first and second processor cores (i.e., processor

cores 1074a and 1074b and processor cores 1084a and 1084b). Such cores 1074, 1074b, 1084a, 1084b may be configured to execute instruction code.

[0031] Each processing element 1070, 1080 may include at least one shared cache or memory unit which may include memory stacks/cells described herein. The shared cache may store data (e.g., instructions) that are utilized by one or more components of the processor, such as the cores 1074a, 1074b and 1084a, 1084b, respectively. For example, the shared cache may locally cache data stored in a memory 1032, 1034 for faster access by components of the processor. In one or more embodiments, the shared cache may include one or more mid-level caches, such as level 2 (L2), level 3 (L3), level 4 (L4), or other levels of cache, a last level cache (LLC), and/or combinations thereof.

[0032] While shown with only two processing elements 1070, 1080, it is to be understood that the scope of the present invention is not so limited. In other embodiments, one or more additional processing elements may be present in a given processor. Alternatively, one or more of processing elements 1070, 1080 may be an element other than a processor, such as an accelerator or a field programmable gate array. For example, additional processing element(s) may include additional processors(s) that are the same as a first processor 1070, additional processor(s) that are heterogeneous or asymmetric to first processor 1070, accelerators (such as, e.g., graphics accelerators or digital signal processing (DSP) units), field programmable gate arrays, or any other processing element. There can be a variety of differences between the processing elements 1070, 1080 in terms of a spectrum of metrics of merit including architectural, microarchitectural, thermal, power consumption characteristics, and the like. These differences may effectively manifest themselves as asymmetry and heterogeneity amongst the processing elements 1070, 1080. For at least one embodiment, the various processing elements 1070, 1080 may reside in the same die package.

[0033] First processing element 1070 may further include memory controller logic (MC) 1072 and point-to-point (P-P) interfaces 1076 and 1078. Similarly, second processing element 1080 may include a MC 1082 and P-P interfaces 1086 and 1088. MC's 1072 and 1082 couple the processors to respective memories, namely a

memory 1032 and a memory 1034, which may be portions of main memory locally attached to the respective processors. Memory 1032, 1024 may include memory stacks described herein. While MC logic 1072 and 1082 is illustrated as integrated into the processing elements 1070, 1080, for alternative embodiments the MC logic may be discreet logic outside the processing elements 1070, 1080 rather than integrated therein.

[0034] First processing element 1070 and second processing element 1080 may be coupled to an I/O subsystem 1090 via P-P interfaces 1076, 1086 via P-P interconnects 1062, 10104, respectively. As shown, I/O subsystem 1090 includes P-P interfaces 1094 and 1098. Furthermore, I/O subsystem 1090 includes an interface 1092 to couple I/O subsystem 1090 with a high performance graphics engine 1038. In one embodiment, a bus may be used to couple graphics engine 1038 to I/O subsystem 1090. Alternately, a point-to-point interconnect 1039 may couple these components.

[0035] In turn, I/O subsystem 1090 may be coupled to a first bus 10110 via an interface 1096. In one embodiment, first bus 10110 may be a Peripheral Component Interconnect (PCI) bus, or a bus such as a PCI Express bus or another third generation I/O interconnect bus, although the scope of the present invention is not so limited.

[0036] As shown, various I/O devices 1014, 1024 may be coupled to first bus 10110, along with a bus bridge 1018 which may couple first bus 10110 to a second bus 1020. In one embodiment, second bus 1020 may be a low pin count (LPC) bus. Various devices may be coupled to second bus 1020 including, for example, a keyboard/mouse 1022, communication device(s) 1026 (which may in turn be in communication with a computer network), and a data storage unit 1028 such as a disk drive or other mass storage device (which may include the RRAM stacks/cells described herein) which may include code 1030, in one embodiment. The code 1030 may include instructions for performing embodiments of one or more of the methods described above. Further, an audio I/O 1024 may be coupled to second bus 1020.

[0037] Note that other embodiments are contemplated. For example, instead of the point-to-point architecture shown, a system may implement a multi-drop bus or another such communication topology. Also, the elements of Figure 4 may alternatively be partitioned using more or fewer integrated chips than shown in the Figure 4. For example, a field programmable gate array may share a single wafer with a processor element and memory including MTJs described herein.

[0038] Various embodiments include a semiconductive substrate. Such a substrate may be a bulk semiconductive material this is part of a wafer. In an embodiment, the semiconductive substrate is a bulk semiconductive material as part of a chip that has been singulated from a wafer. In an embodiment, the semiconductive substrate is a semiconductive material that is formed above an insulator such as a semiconductor on insulator (SOI) substrate. In an embodiment, the semiconductive substrate is a prominent structure such as a fin that extends above a bulk semiconductive material.

[0039] "Adjacent" or "immediately adjacent", as used herein, are relative terms. Thus, filaments having oxygen vacancies may have those vacancies adjacent electrode 209 or OEL 214 but not (relatively speaking) electrode 202. "Top" and "bottom" are relative terms and may change based on the orientation of the stack/cell. OEL is a term of art known to those of ordinary skill in the art. The OEL may also be referred to as a "metal cap layer". The OEL may include a metal such that, when the OEL is adjacent or contacting an oxygen source (e.g., oxide layer), the OEL facilitates "oxygen exchange" with the oxygen source. By saying "a first layer includes a first material different from a second material included in a second layer" the first material may include, for example, Hf while the second material includes Al or the first material may include HfOx while the second material includes HfSiOx. Also, a term like SiOx and the like is shorthand and includes instances such as SiO_2.

[0040] In an embodiment the top and bottom electrodes include different materials. In an embodiment, electrodes may include conductive oxides (ITO), nitrides (TiN), and the like.

[0041] The following examples pertain to further embodiments.

[0042] Example 1 includes a memory comprising: a top electrode portion and a bottom electrode portion; and an oxide layer between the top and bottom electrode portions; wherein (a) a conductive filament is within the oxide layer, (b) the oxide layer includes oxide layer sidewalls that are not coplanar with each other, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is substantially parallel to the oxide layer sidewalls, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

[0043] An version of Example 1 includes a memory comprising: a top electrode portion and a bottom electrode portion; and an oxide layer between the top and bottom electrode portions; wherein (a) a conductive filament is within the oxide layer and is adjacent the top electrode portion, (b) the oxide layer includes oxide layer sidewalls that are not coplanar with each other, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is substantially parallel to the oxide layer sidewalls, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

[0044] In example 2 the subject matter of the Example 1 can optionally include wherein (a) the void surrounds the oxide layer and does not intersect the vertical axis, and (b) a horizontal axis, orthogonal to the vertical axis, intersects the void and the oxide layer.

[0045] In example 3 the subject matter of the Examples 1-2 can optionally include an oxygen exchange layer (OEL) between the oxide layer and the top electrode portion; wherein (a) the void surrounds the OEL, and (b) an additional horizontal axis, orthogonal to the vertical axis, intersects the void and the OEL.

[0046] In example 4 the subject matter of the Examples 1-3 can optionally include wherein the OEL directly contacts the oxide layer.

[0047] In example 5 the subject matter of the Examples 1-4 can optionally include wherein the void is ring-shaped.

[0048] In example 6 the subject matter of the Examples 1-5 can optionally include wherein the void includes a cross section that is: (a) in a plane that is coplanar with

the horizontal axis, and (b) continuous and uninterrupted along its entire outermost perimeter that extends 360 degrees around the oxide layer.

[0049] In example 7 the subject matter of the Examples 1-6 can optionally include wherein the void does not extend above the top electrode portion and the void does not extend below the bottom electrode portion.

[0050] In example 8 the subject matter of the Examples 1-7 can optionally include an additional top electrode portion and an additional bottom electrode portion; and an additional oxide layer between the additional top and bottom electrode portions; wherein (a) an additional conductive filament is within the additional oxide layer, (b) the additional oxide layer includes additional oxide layer sidewalls, (c) an additional vertical axis intersects the additional oxide layer, and the additional top and bottom electrode portions and is substantially parallel to the additional oxide layer sidewalls, and (d) an additional void, which includes air, is adjacent the additional oxide layer sidewalls.

[0051] In example 9 the subject matter of the Examples 1-8 can optionally include wherein the void directly contacts the additional void and no other oxide layer is immediately between the oxide layer and the additional oxide layer.

[0052] In example 10 the subject matter of the Examples 1-9 can optionally include wherein (a) the additional void surrounds the additional oxide layer and does not intersect the additional vertical axis, and (b) the horizontal axis intersects the additional void and the additional oxide layer.

[0053] In example 11 the subject matter of the Examples 1-10 can optionally include wherein the additional void is ring-shaped.

[0054] In example 11 the subject matter of the Examples 1-10 can optionally include wherein the additional void is ring-shaped and the conductive filament is adjacent the top electrode portion.

[0055] In example 12 the subject matter of the Examples 1-11 can optionally include a barrier layer between the void and the oxide layer and the barrier layer intersects the horizontal axis.

[0056] In example 13 the subject matter of the Examples 1-12 can optionally include wherein the barrier layer directly contacts the void and the oxide layer.

[0057] In example 14 the subject matter of the Examples 1-13 can optionally include wherein (a) the barrier layer directly contacts a dielectric layer, (b) the barrier layer is between the oxide layer and the dielectric layer, and (b) an additional horizontal axis, orthogonal to the vertical axis, intersects the oxide layer, the barrier layer, and the dielectric layer.

[0058] In example 15 the subject matter of the Examples 1-14 can optionally include a dielectric layer and an additional horizontal axis, orthogonal to the vertical axis, which intersects the top electrode portion and the dielectric layer.

[0059] In example 16 the subject matter of the Examples 1-15 can optionally include wherein (a) the void surrounds the top electrode portion, and (b) another horizontal axis, orthogonal to the vertical axis, intersects the void and the top electrode portion.

[0060] In example 17 the subject matter of the Examples 1-16 can optionally include wherein the memory is a resistive random access memory (RRAM).

[0061] In example 18 the subject matter of the Examples 1-17 can optionally include wherein: in a first state when energy is applied to the top electrode portion at a first polarity the filament has a first electrical resistance; and in a second state when energy is applied to the top electrode portion at a second polarity, which is opposite the first polarity, the filament has a second electrical resistance that is greater than the first electrical resistance.

[0062] In example 19 the subject matter of the Examples 1-18 can optionally include wherein the oxide layer includes at least one of HfO_2, SiO_2, Al_2O_3,TiO_2, $SrTiO_3$, Cr-$SrTiO_3$, NiO, CuOx, ZrO_2, Nb_2O_5, MgO, Fe_2O_3, Ta_2O_5, ZnO, CoO, CuMnOx, CuMoOx, InZnO, Cr-$SrZrO_3$, $PrCaMnO_3$, $SrLaTiO_3$, $LaSrFeO_3$, $(Pr,Ca)MnO_3$, Nb-$SrTiO_3$, and $LaSrCoO_3$.

[0063] In another version of example 19 the subject matter of the Examples 1-18 can optionally include wherein the oxide layer includes at least one sub-stoichiometric oxide having a composition AOx or ABOx, where A and B are metals.

[0064] In example 20 the subject matter of the Examples 1-19 can optionally include a system comprising: a processor; a memory, coupled to the processor, according to any one of claims 1 to 19; and a communication module, coupled to the processor, to communicate with a computing node external to the system.

[0065] Example 21 includes an apparatus comprising: at least one processor; at least one resistive random access memory (RRAM), coupled to the at least one processor, comprising: a top electrode portion and a bottom electrode portion; and an oxide layer between the top and bottom electrode portions; wherein (a) a conductive filament is within the oxide layer and is adjacent the top electrode portion, (b) the oxide layer includes oxide layer sidewalls that are not coplanar with each other, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is substantially parallel to the oxide layer sidewalls, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

[0066] In example 22 the subject matter of the Example 21 can optionally include wherein (a) the void surrounds the oxide layer and does not intersect the vertical axis, and (b) a horizontal axis, orthogonal to the vertical axis, intersects the void and the oxide layer.

[0067] Example 23 includes a memory comprising: a top electrode portion and a bottom electrode portion; and an oxide layer between the top and bottom electrode portions; wherein (a) a conductive filament is within the oxide layer, (b) the oxide layer includes oxide layer sidewalls, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

[0068] In example 24 the subject matter of the Example 23 can optionally include wherein (a) the void surrounds the oxide layer and does not intersect the vertical axis, and (b) a horizontal axis, orthogonal to the vertical axis, intersects the void and the oxide layer.

[0069] Example 25 addresses an embodiment that includes devices, such as the device of Figure 3N, before filament formation occurs. The device may exist before an anneal is performed that creates the filament. Thus, the embodiment includes a memory comprising: a top electrode portion and a bottom electrode portion; and an oxide layer between the top and bottom electrode portions; wherein (a) the oxide layer includes oxide layer sidewalls that are not coplanar with each other, (b) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is substantially parallel to the oxide layer sidewalls, and (c) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls. A filament may later be formed in the oxide layer.

[0070] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and still fall within the meaning of the term "top." The term "on" as used herein (including in the claims) does not indicate that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

1. A memory comprising:
a top electrode portion and a bottom electrode portion; and
an oxide layer between the top and bottom electrode portions;
wherein (a) a conductive filament is within the oxide layer, (b) the oxide layer includes oxide layer sidewalls that are not coplanar with each other, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is substantially parallel to the oxide layer sidewalls, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

2. The memory of claim 1, wherein (a) the void surrounds the oxide layer and does not intersect the vertical axis, and (b) a horizontal axis, orthogonal to the vertical axis, intersects the void and the oxide layer.

3. The memory of claim 2 comprising:
an oxygen exchange layer (OEL) between the oxide layer and the top electrode portion;
wherein (a) the void surrounds the OEL, and (b) an additional horizontal axis, orthogonal to the vertical axis, intersects the void and the OEL.

4. The memory of claim 3 wherein the OEL directly contacts the oxide layer.

5. The memory of claim 2, wherein the void is ring-shaped.

6. The memory of claim 5, wherein the void includes a cross section that is: (a) in a plane that is coplanar with the horizontal axis, and (b) continuous and uninterrupted along its entire outermost perimeter that extends 360 degrees around the oxide layer.

7. The memory of claim 5, wherein the void does not extend above the top electrode portion and the void does not extend below the bottom electrode portion.

8. The memory of claim 2 comprising:

an additional top electrode portion and an additional bottom electrode portion; and

an additional oxide layer between the additional top and bottom electrode portions;

wherein (a) an additional conductive filament is within the additional oxide layer, (b) the additional oxide layer includes additional oxide layer sidewalls, (c) an additional vertical axis intersects the additional oxide layer, and the additional top and bottom electrode portions and is substantially parallel to the additional oxide layer sidewalls, and (d) an additional void, which includes air, is adjacent the additional oxide layer sidewalls.

9. The memory of claim 8, wherein the void directly contacts the additional void and no other oxide layer is immediately between the oxide layer and the additional oxide layer.

10. The memory of claim 9, wherein (a) the additional void surrounds the additional oxide layer and does not intersect the additional vertical axis, and (b) the horizontal axis intersects the additional void and the additional oxide layer.

11. The memory of claim 10, wherein the additional void is ring-shaped and the conductive filament is adjacent the top electrode portion.

12. The memory of claim 2 comprising a barrier layer between the void and the oxide layer and the barrier layer intersects the horizontal axis.

13. The memory of claim 12, wherein the barrier layer directly contacts the void and the oxide layer.

14. The memory of claim 12, wherein (a) the barrier layer directly contacts a dielectric layer, (b) the barrier layer is between the oxide layer and the dielectric layer, and (b) an additional horizontal axis, orthogonal to the vertical axis, intersects the oxide layer, the barrier layer, and the dielectric layer.

15. The memory of claim 2 comprising a dielectric layer and an additional horizontal axis, orthogonal to the vertical axis, which intersects the top electrode portion and the dielectric layer.

16. The memory of claim 2, wherein (a) the void surrounds the top electrode portion, and (b) another horizontal axis, orthogonal to the vertical axis, intersects the void and the top electrode portion.

17. The memory of claim 2, wherein the memory is a resistive random access memory (RRAM).

18. The memory of claim 17, wherein:

in a first state when energy is applied to the top electrode portion at a first polarity the filament has a first electrical resistance; and

in a second state when energy is applied to the top electrode portion at a second polarity, which is opposite the first polarity, the filament has a second electrical resistance that is greater than the first electrical resistance.

19. The memory of claim 2, wherein the oxide layer includes at least one of HfO_2, SiO_2, Al_2O_3,TiO_2, $SrTiO_3$, Cr-$SrTiO_3$, NiO, CuOx, ZrO_2, Nb_2O_5, MgO, Fe_2O_3, Ta_2O_5, ZnO, CoO, CuMnOx, CuMoOx, InZnO, Cr-$SrZrO_3$, $PrCaMnO_3$, $SrLaTiO_3$, $LaSrFeO_3$, $(Pr,Ca)MnO_3$, Nb-$SrTiO_3$, and $LaSrCoO_3$.

20. A system comprising:

a processor;

a memory, coupled to the processor, according to any one of claims 1 to 19; and

a communication module, coupled to the processor, to communicate with a computing node external to the system.

21. An apparatus comprising:

at least one processor;

at least one resistive random access memory (RRAM), coupled to the at least one processor, comprising:

a top electrode portion and a bottom electrode portion; and

an oxide layer between the top and bottom electrode portions;

wherein (a) a conductive filament is within the oxide layer and is adjacent the top electrode portion, (b) the oxide layer includes oxide layer sidewalls that are not coplanar with each other, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions and is substantially parallel to the oxide layer sidewalls, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

22. The apparatus of claim 1, wherein (a) the void surrounds the oxide layer and does not intersect the vertical axis, and (b) a horizontal axis, orthogonal to the vertical axis, intersects the void and the oxide layer.

23. A memory comprising:

a top electrode portion and a bottom electrode portion; and

an oxide layer between the top and bottom electrode portions;

wherein (a) a conductive filament is within the oxide layer, (b) the oxide layer includes oxide layer sidewalls, (c) a vertical axis intersects the oxide layer and the top and bottom electrode portions, and (d) a singular void, which includes air, is adjacent to each of the oxide layer sidewalls.

24. The memory of claim 23, wherein (a) the void surrounds the oxide layer and does not intersect the vertical axis, and (b) a horizontal axis, orthogonal to the vertical axis, intersects the void and the oxide layer.

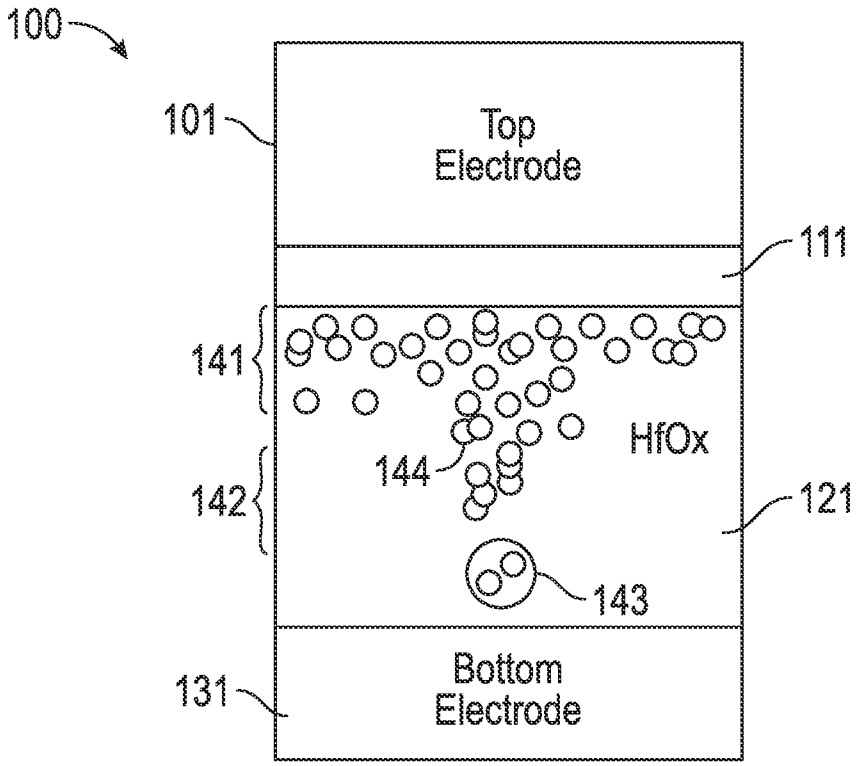
100
101
Top
Electrode
111
141
HfOx
144
142
121
143
131
Bottom
Electrode

FIG. 1

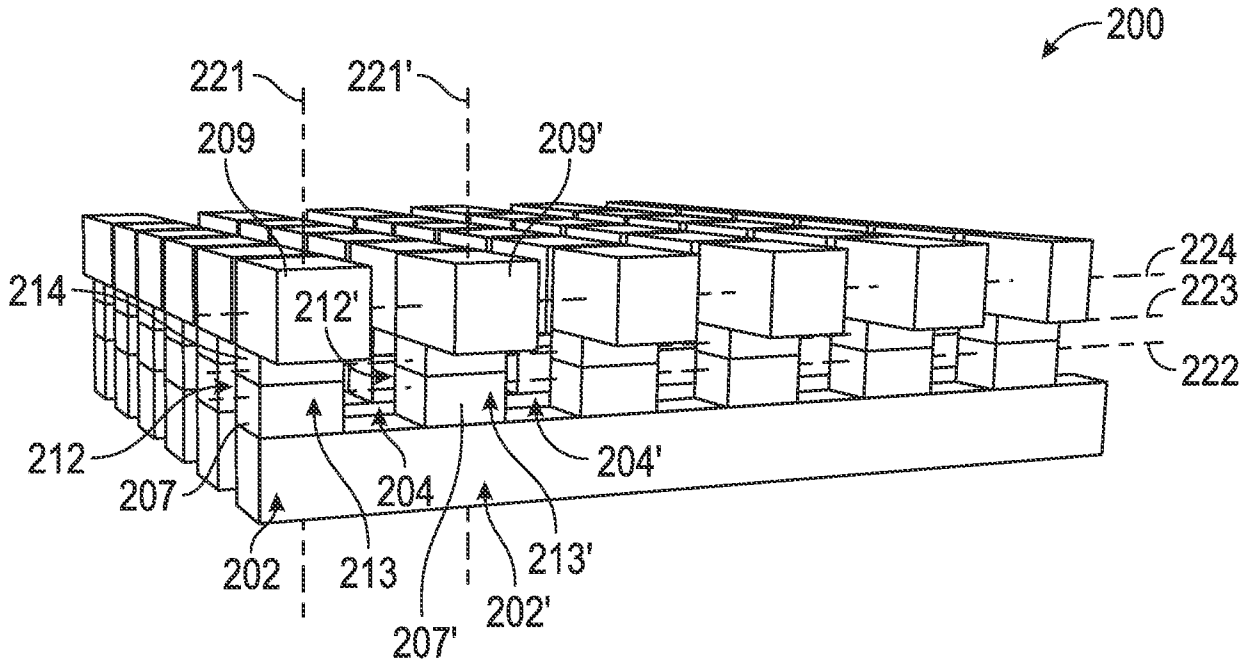
200
221
221'
209
209'
214
212'
224
223
222
212
207
204
204'
202
213
213'
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FIG. 2A

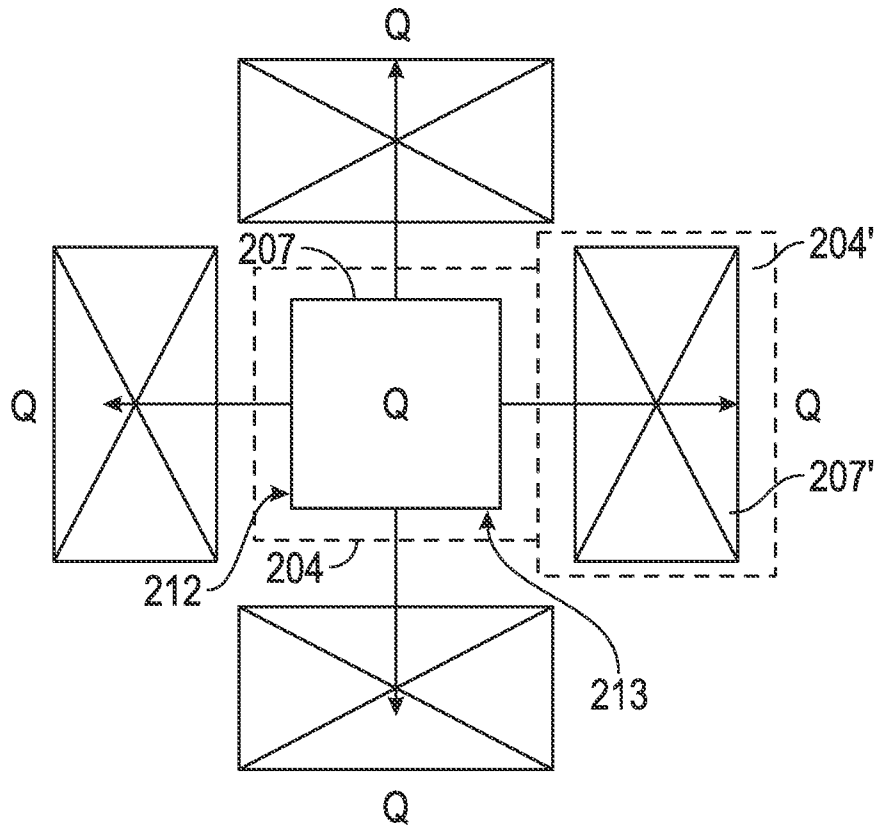
Q
207
204'
Q
Q
Q
207'
204
212
213
Q

FIG. 2B

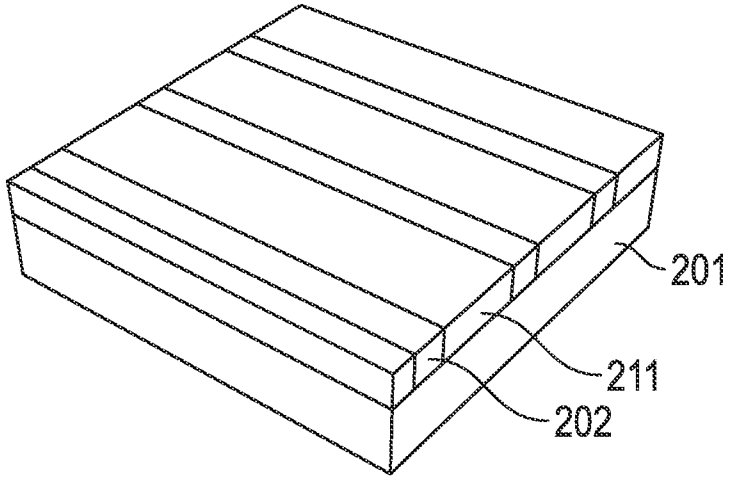

FIG. 3A

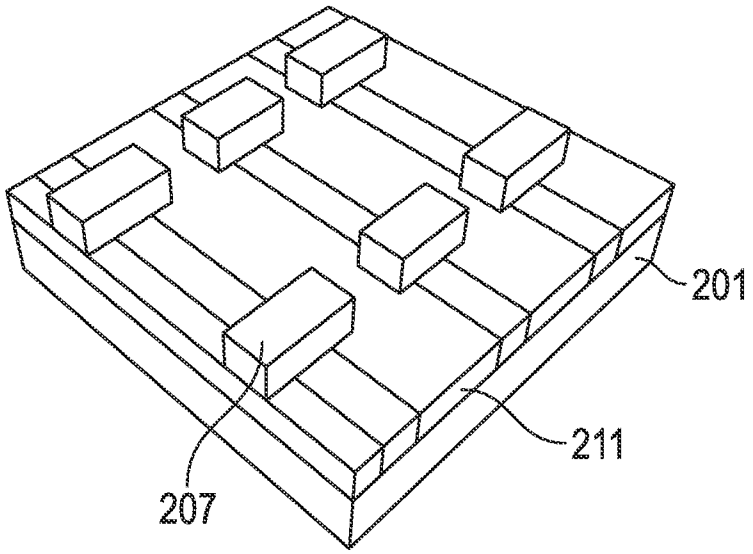

FIG. 3B

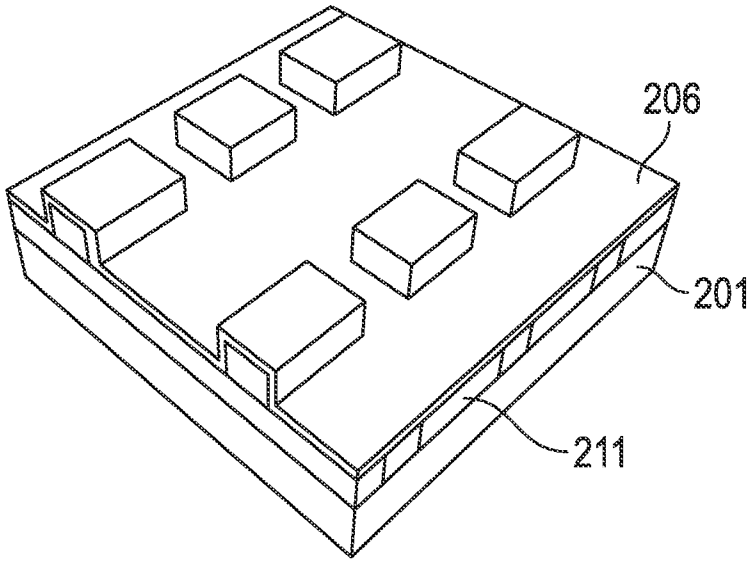

FIG. 3C

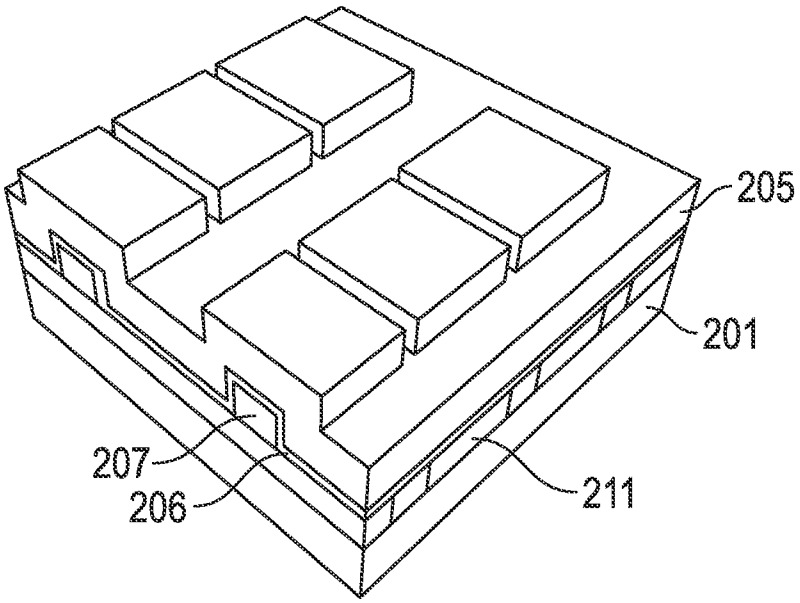

FIG. 3D

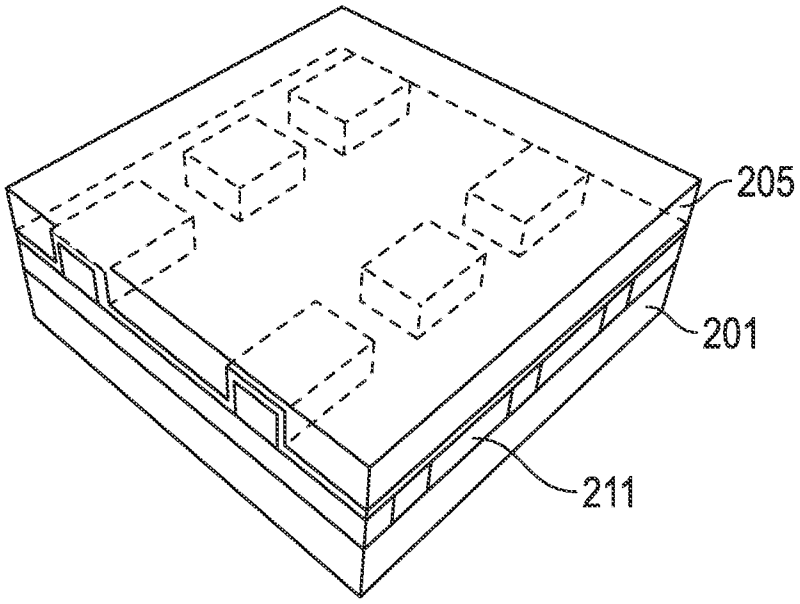

FIG. 3E

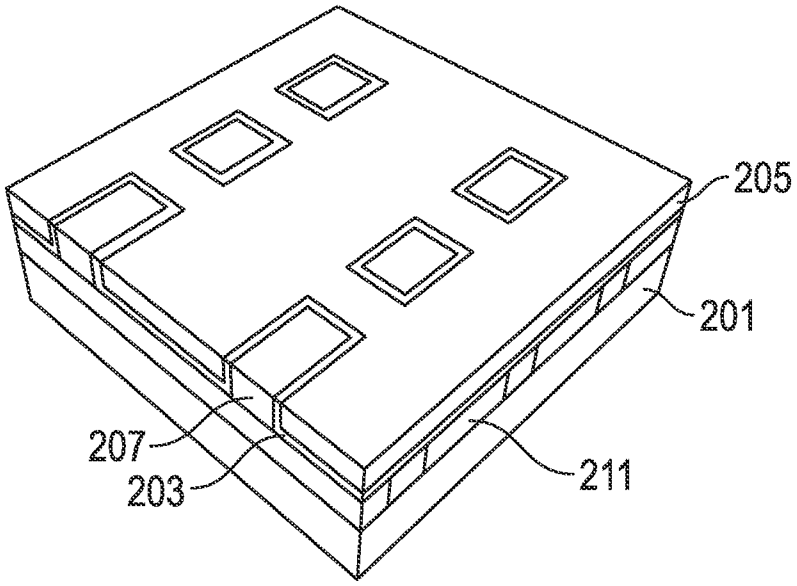

FIG. 3F

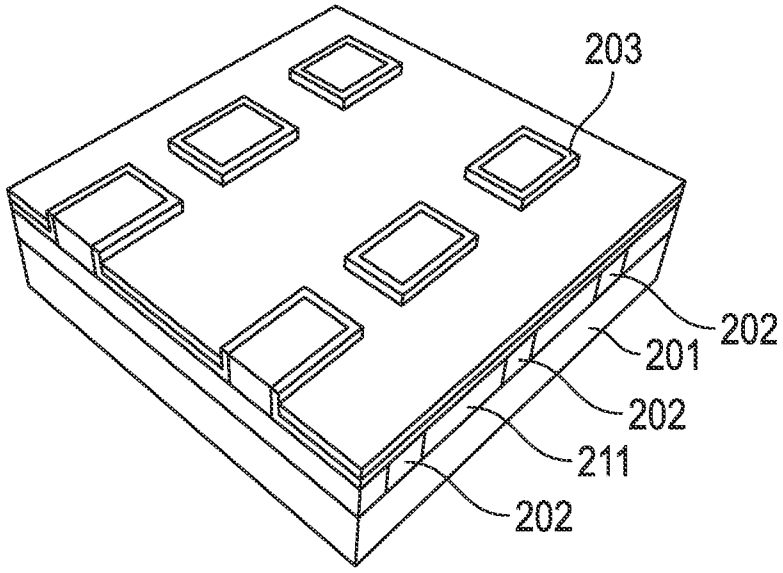

FIG. 3G

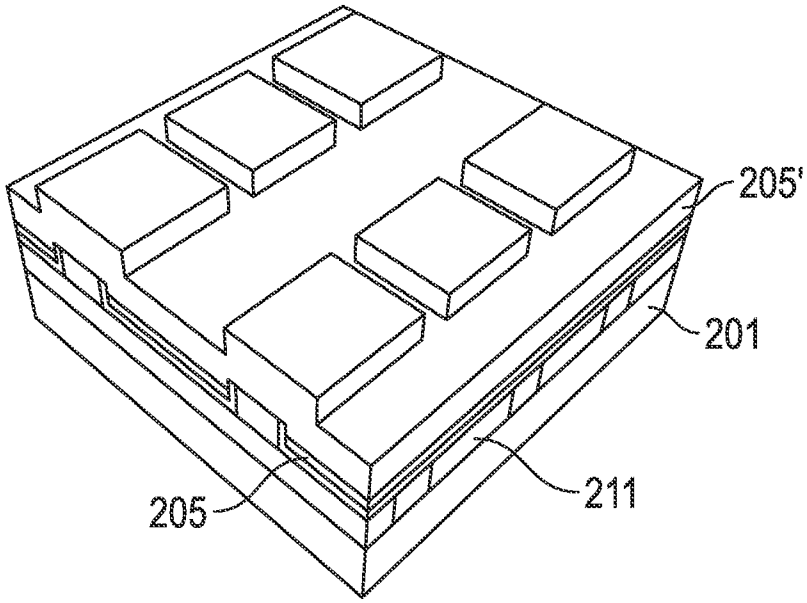

FIG. 3H

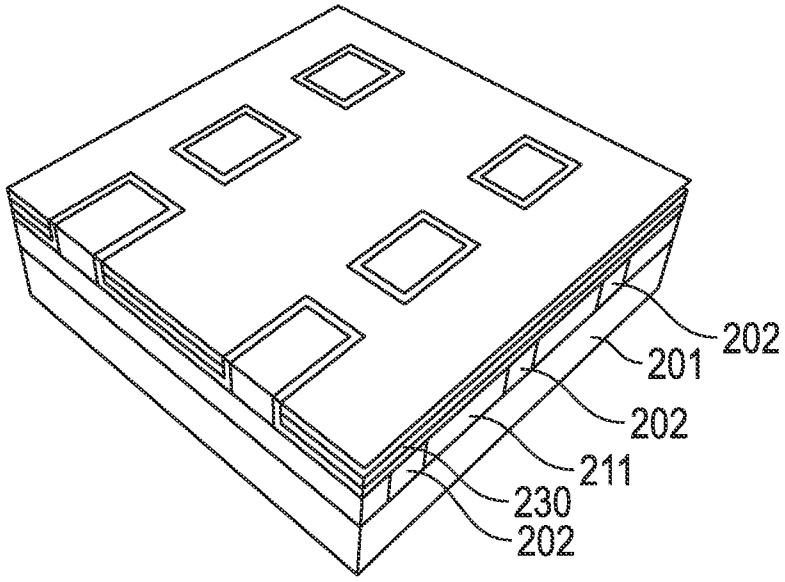

FIG. 3I

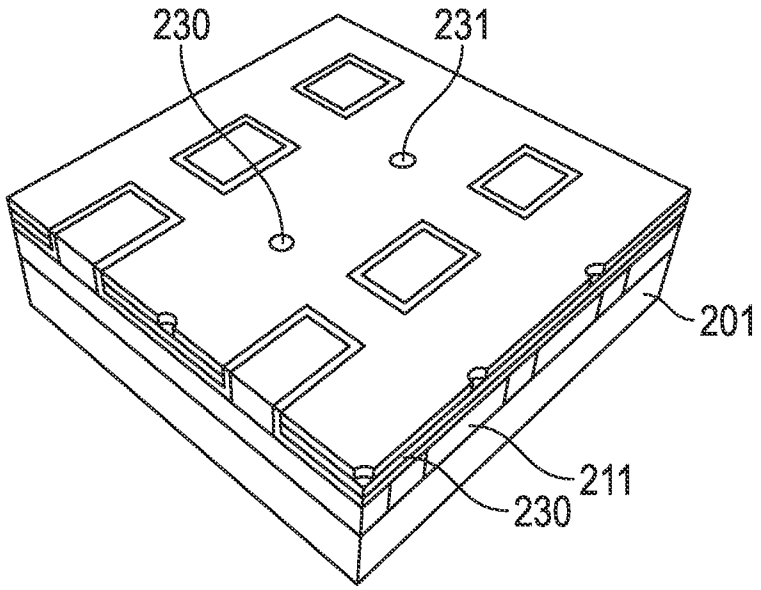

FIG. 3J

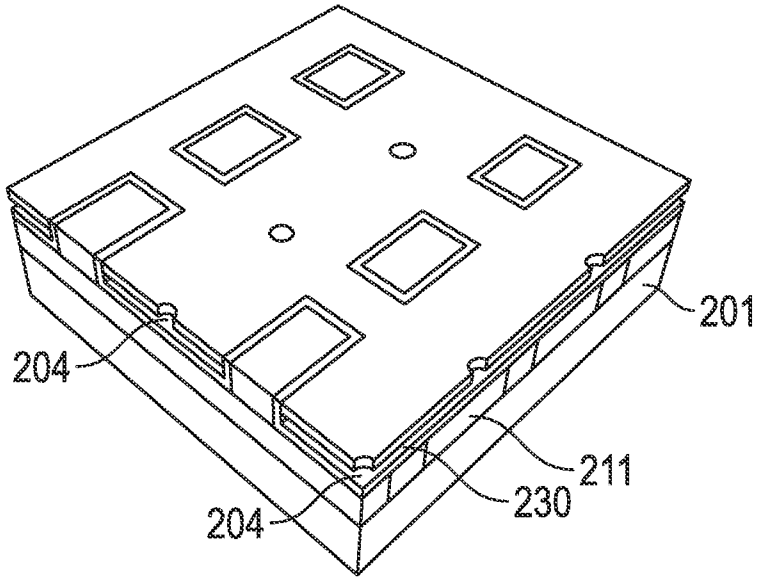

FIG. 3K

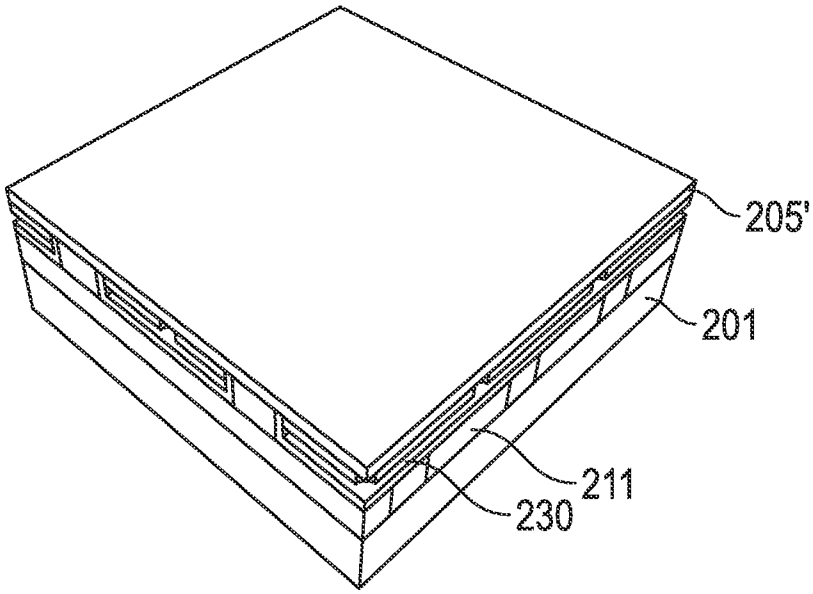

FIG. 3L

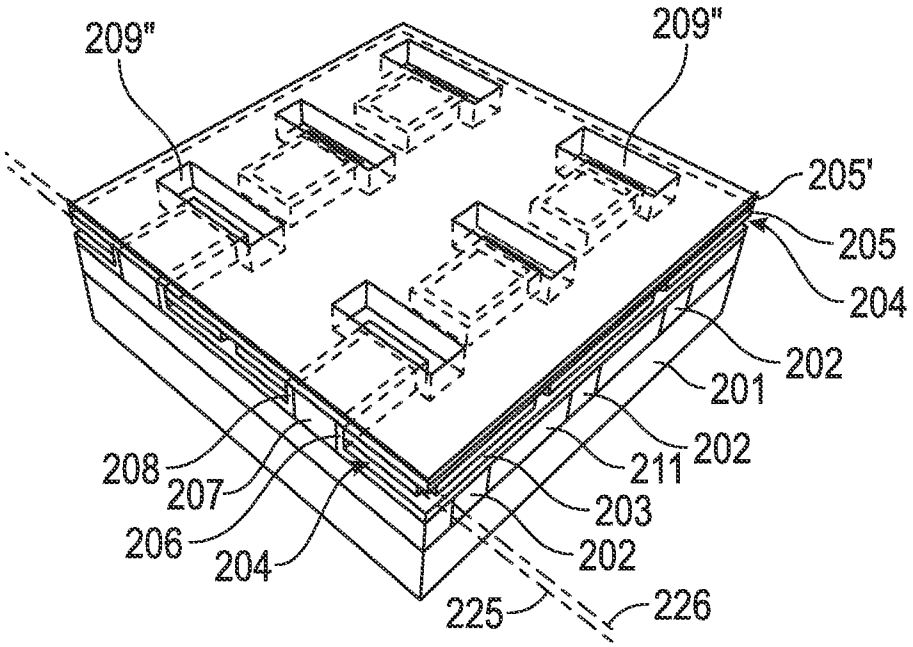
209"
209"
205'
205
204
202
201
202
211
203
202
208
207
206
204
225
226

FIG. 3M

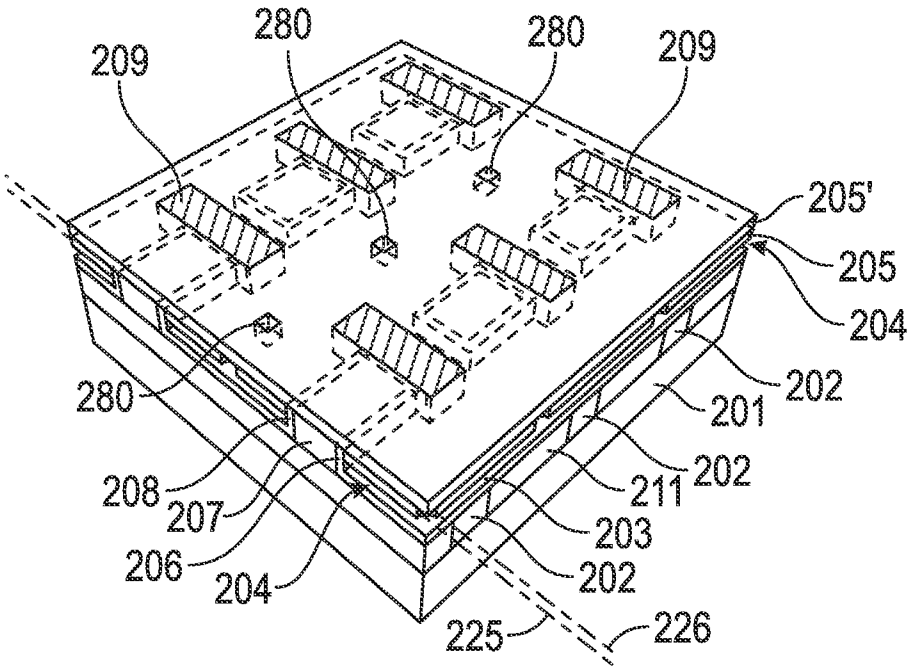
280
280
209
209
205'
205
204
202
201
202
211
203
202
280
208
207
206
204
225
226

FIG. 3N

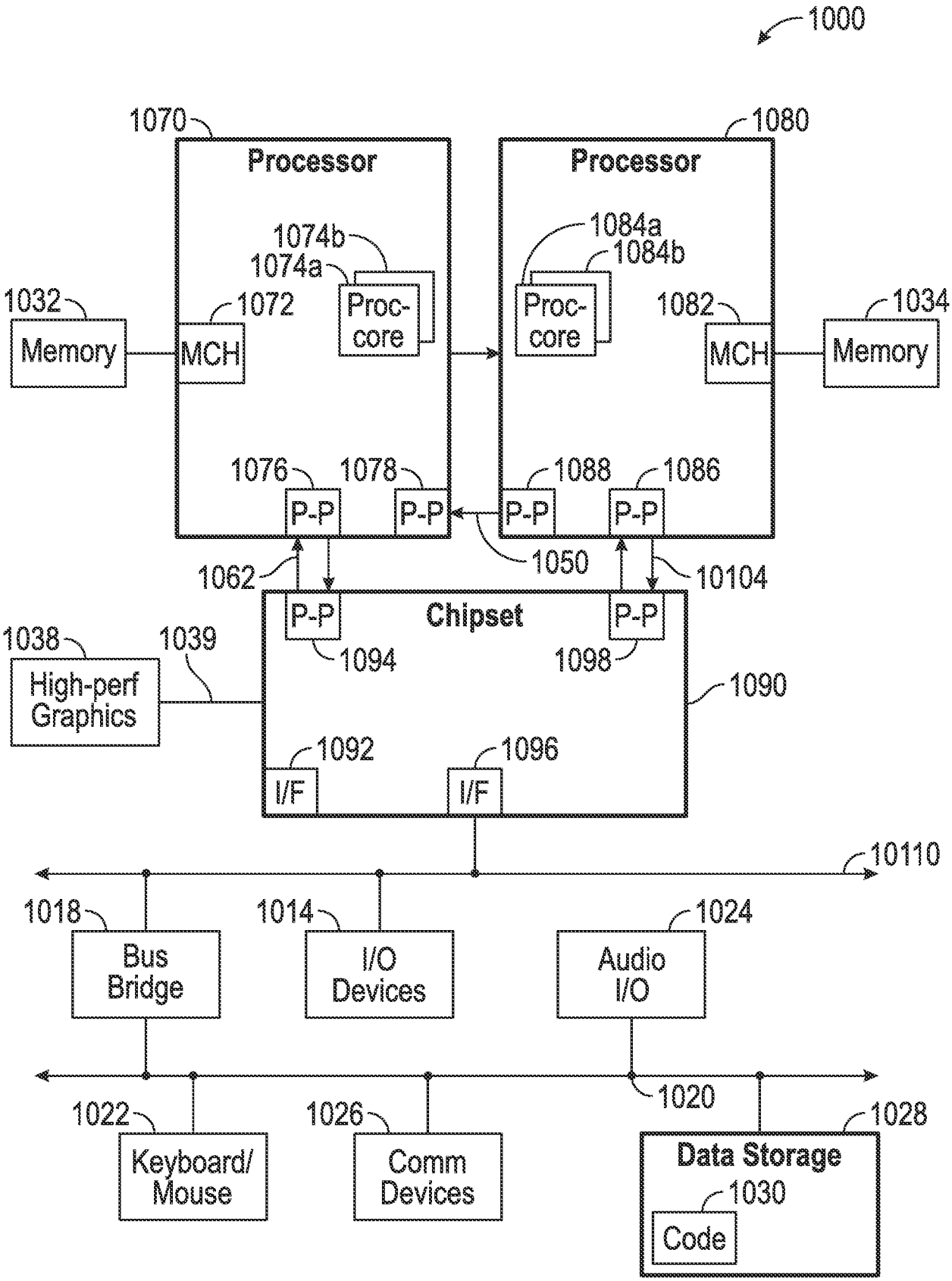
1000
1070
Processor
1080
Processor
1074b
1074a
1084a
1084b
1032
Memory
1072
MCH
Proc-core
Proc-core
1082
MCH
1034
Memory
1076
1078
1088
1086
P-P
P-P
P-P
P-P
1062
1050
10104
P-P
Chipset
P-P
1038
High-perf Graphics
1039
1094
1098
1090
1092
1096
I/F
I/F
10110
1018
Bus Bridge
1014
I/O Devices
1024
Audio I/O
1020
1022
Keyboard/ Mouse
1026
Comm Devices
1028
Data Storage
1030
Code

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/052198

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/115; G06F 3/06; H01L 45/00; H01L 27/24; G11C 11/00; G11C 29/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: memory, filament, sidewall, void

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0214478 A1 (JUNG-MOO LEE et al.) 30 July 2015 See abstract, paragraphs [0035], [0060]-[0085], [0289]-[0291] and figures 1-3B, 52.	1-24
A	US 2012-0132879 A1 (MASAHARU KINOSHITA et al.) 31 May 2012 See abstract, paragraphs [0085]-[0089] and figures 1-5.	1-24
A	US 2015-0155482 A1 (SK HYNIX INC.) 04 June 2015 See abstract, paragraphs [0034]-[0063] and figures 1-6.	1-24
A	US 2014-0054537 A1 (SK HYNIX INC.) 27 February 2014 See abstract, paragraphs [0025]-[0031] and figures 2A-2E.	1-24
A	US 2010-0202186 A1 (MITSURU SATO et al.) 12 August 2010 See abstract, paragraphs [0041]-[0086] and figures 1-11.	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2016 (31.05.2016)	**31 May 2016 (31.05.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/052198

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