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[Continued on nextpage]

(54) Title: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FIG. 9A

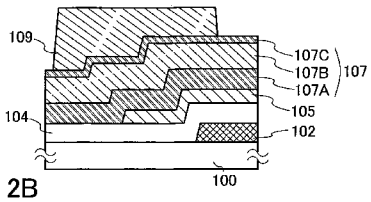


FIG. 2B

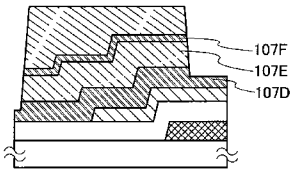


FIG. 2C

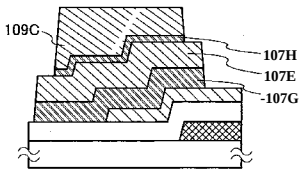
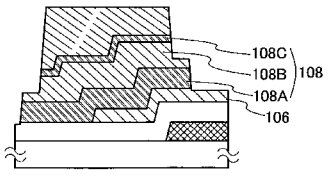


FIG. 2D



(57) Abstract: When a transistor including a conductive layer having a three-layer structure is manufactured, three-stage etching is performed. In the first etching process, an etching method in which the etching rates for the second film and the third film are high is employed, and the first etching process is performed until the first film is at least exposed. In the second etching process, an etching method in which the etching rate for the first film is higher than that in the first etching process and the etching rate for a layer provided below and in contact with the first film is lower than that in the first etching process is employed. In the third etching process, an etching method in which the etching rates for the first to the third films are higher than those in the second etching process is preferably employed.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

[0001]

The technical field of the present invention relates to a semiconductor device and a manufacturing method thereof. Note that in this specification, a semiconductor device refers to a semiconductor element itself or a device including a semiconductor element. As an example of such a semiconductor element, for example, a transistor (a thin film transistor and the like) can be given. In addition, a semiconductor device also refers to a display device such as a liquid crystal display device.

BACKGROUND ART

[0002]

In recent years, metal oxides having semiconductor characteristics (hereinafter, referred to as oxide semiconductors) have attracted attention. Oxide semiconductors may be applied to transistors (see Patent Documents 1 and 2), for example.

[0003]

There are many types of transistors. For example, transistors may be classified as a bottom gate-type structure and a top gate-type structure according to the positional relationship among a substrate, a gate, and a channel formation region. A transistor structure having a gate placed between a channel formation region and a substrate is called a bottom gate-type structure. A transistor structure having a channel formation region placed between a gate and a substrate is called a top gate-type structure.

[0004]

In addition, transistors may be classified as a bottom contact type and a top contact type according to connection portions of a source and a drain with a semiconductor layer in which a channel is formed. A transistor with a structure where the connection portions of a source and a drain with a semiconductor layer in which a channel is formed is placed on a substrate side is called a bottom contact type. A

transistor with a structure where the connection portions of a source and a drain with a semiconductor layer in which a channel is formed is placed on a side opposite to a substrate (that is, a counter substrate side in a liquid crystal display device) is called a top contact type.

[0005]

Types of transistors can be classified as a BGBC (bottom gate bottom contact) structure, a BGTC (bottom gate top contact) structure, a TGTC (top gate top contact) structure, and a TGBC (top gate bottom contact) structure.

[Reference]

[Patent Documents]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

DISCLOSURE OF INVENTION

[0007]

An object of one embodiment of the present invention is to provide a transistor having a sufficiently large on-state current and a sufficiently small off-state current. Such a transistor having a sufficiently large on-state current and a sufficiently small off-state current has good switching characteristics.

[0008]

Meanwhile, a transistor when applied to many types of products preferably has high reliability.

[0009]

One of methods for examining reliability of transistors is a bias-temperature stress test (hereinafter, referred to as a Gate Bias Temperature (GBT) test). The GBT test is one kind of accelerated test and a change in characteristics, caused by long-term usage, of transistors can be evaluated in a short time. In particular, the amount of shift in threshold voltage of the transistor between before and after a GBT test is an important indicator for examining reliability. The smaller the shift in the threshold voltage between before and after a GBT test is, the higher the reliability of the transistor is.

[0010]

In particular, the temperature of a substrate over which a transistor is formed is set at a fixed temperature. A source and a drain of the transistor are set at the same potential, and a gate is supplied with a potential different from those of the source and the drain for a certain period. The temperature of the substrate may be determined depending on the purpose of the test. Further, the potential applied to the gate is higher than the potential of the source and the drain (the potential of the source and the drain is the same) in a "+GBT test" while the potential applied to the gate is lower than the potential of the source and the drain (the potential of the source and the drain is the same) in a "-GBT test."

[0011]

Strength of the GBT test may be determined based on the temperature of a substrate and electric field intensity and time period of application of the electric field to a gate insulating layer. The electric field intensity in the gate insulating layer is determined as the value of a potential difference between a gate, and a source and a drain divided by the value of the thickness of the gate insulating layer. For example, when an electric field intensity of the gate insulating layer having a thickness of 100 nm is 2 MV/cm, the potential difference is 20 V.

[0012]

Furthermore, the shift in the threshold voltage of a transistor having an oxide semiconductor in a channel formation region is also confirmed by a GBT test.

[0013]

Therefore, one embodiment of the present invention is to provide a semiconductor device having high reliability and threshold voltage which is difficult to shift despite long term usage.

[0014]

Further, another embodiment of the present invention is to provide a semiconductor device having high reliability and good switching characteristics.

[0015]

Furthermore, a gate, a source and a drain of a transistor are preferably formed over the same layer as a gate wiring and a source wiring. The gate wiring and the

source wiring are preferably formed of a material having high conductivity.

[0016]

The semiconductor device having good switching characteristics, which is one embodiment of the present invention, can be obtained by forming a semiconductor layer serving as a channel formation region to have a sufficient thickness to the thickness of the gate insulating layer.

[0017]

Further, the semiconductor device having high reliability, which is one embodiment of the present invention, can be obtained by improving coverage of each layer to be provided.

[0018]

Specific structures of one preferred embodiment of the present invention will be described below.

[0019]

One embodiment of the present invention is an etching method including at least first to third etching processes. Here, a "film to be etched" preferably has a three-layer structure including a first film, a second film, and a third film from the lower side. In a first etching process, an etching method in which the etching rates for at least the second film and the third film are high is employed, and the first etching process is performed until at least the first film is exposed. In a second etching process, an etching method in which the etching rate for the first film is higher than that in the first etching process and the etching rate for a "layer provided below and in contact with the first film" is lower than that in the first etching process is employed. In a third etching process, an etching method in which the etching rates for the first to the third films are higher than those in the second etching process is preferably employed.

[0020]

In the third etching process, the etching rate for the "layer provided below and in contact with the first film" may be higher than that in the second etching process. At that time, the third etching process is preferably performed in a shorter time than the first etching process.

[0021]

The above-described etching method that is one embodiment of the present invention can be applied to a manufacturing process of a semiconductor device. In particular, when the "film to be etched" is a conductive film, the etching method that is one embodiment of the present invention, described above is preferably used. Especially, the " layer provided below and in contact with the first film" is preferably a semiconductor layer. In other words, a transistor included in the semiconductor device described in one embodiment of the present invention is preferably a top contact type.

[0022]

In other words, one embodiment of the present invention is a method for manufacturing a semiconductor device including the steps of forming a first wiring layer; forming an insulating layer to cover the first wiring layer; forming a semiconductor layer over the insulating layer; stacking a first conductive film, a second conductive film, and a third conductive in this order over the semiconductor layer; and performing at least three-stage etching on the first to third conductive films to form separated second wiring layers having a three-layer structure. The three-stage etching includes a first etching process, which is performed until at least the first conductive film is exposed; a second etching process, which is performed under the condition that the etching rate for the first conductive film is higher than that in the first etching process and the etching rate for the semiconductor layer is lower than that in the first etching process; and a third etching process, which is performed under the condition that the etching rates for the first to the third conductive films are higher than those in the second etching process.

[0023]

Another embodiment of the present invention is a method for manufacturing a semiconductor device including the steps of forming a semiconductor layer; stacking a first conductive film, a second conductive film, and a third conductive film in this order over the semiconductor layer; performing at least three-stage etching on the first to third conductive films to form separated first wiring layers having a three-layer structure; forming an insulating layer to cover the first wiring layer and the semiconductor layer; and forming a second wiring layer to overlap with the semiconductor layer over the insulating layer. The three-stage etching includes a first etching process, which is performed until at least the first conductive film is exposed; a second etching process,

which is performed under the condition that the etching rate for the first conductive film is higher than that in the first etching process and the etching rate for the semiconductor layer is lower than that in the first etching process; and a third etching process, which is performed under the condition that the etching rates for the first to the third conductive films are higher than those in the second etching process.

[0024]

Note that the present invention is not limited thereto and a transistor may be a bottom contact type. In other words, in the BGBC or TGBC structure, the above-described etching method may be used for the formation of the source and the drain having a three-layer structure. In the BGBC structure, the "layer provided below and in contact with the first film" is a gate insulating layer. In the TGBC structure, the "layer provided below and in contact with the first film" is an insulating film or substrate to be a base.

[0025]

However, the present invention is not limited thereto, and the above-described etching method that is one embodiment of the present invention can be used when a conductive film to be a gate electrode is etched.

[0026]

In one embodiment of the present invention having any one of the above-described structures, the first etching process is performed using a gas containing more chlorine than fluorine as its main component; the second etching process is performed using a gas containing more fluorine than chlorine as its main component; and the third etching process is performed using a gas containing more chlorine than fluorine as its main component.

[0027]

More specifically, a mixture gas of a $BC1_3$ gas and a Cl_2 gas are given as a gas containing more chlorine than fluorine as its main component. As a gas containing more fluorine than chlorine, a SF_6 gas is given.

[0028]

Note that the third etching process is preferably performed in a shorter time than the first etching process.

[0029]

In one embodiment of the present invention having any one of the above-described structures, it is preferable that the first conductive film and the second conductive film be thicker than the third conductive film. This is because the layer provided below and in contact with the first film is not easily exposed when the first conductive film is formed to be thick in the first etching process, and further because wiring resistance is reduced when the second conductive film is formed to be thick.

[0030]

In one embodiment of the present invention having any one of the above-described structures, when the second conductive film is formed to be thick, a conductive material for forming the second conductive film preferably has higher conductivity than a conductive material for forming the first conductive film and the third conductive film. This is because wiring resistance is reduced when the second conductive film is formed to be thick.

[0031]

In one embodiment of the present invention having any one of the above-described structures, the first conductive film and the third conductive film may be titanium films and the second conductive film may be aluminum film, for example.

[0032]

In one embodiment of the present invention having any one of the above-described structures, the semiconductor layer may be an oxide semiconductor layer, for example.

[0033]

In one embodiment of the present invention having any one of the above-described structures the material for the oxide semiconductor layer may be IGZO, for example.

[0034]

According to one embodiment of the present invention, the "layer provided below and in contact with the first film" can be prevented from being thin. Thus, in the case where the "layer provided below and in contact with the first film" is a semiconductor layer, the thickness of the semiconductor layer can be adjusted.

Moreover, by adjusting the thickness of the semiconductor layer, the on-state current of a transistor including the semiconductor layer can become sufficiently high and the off-state current of a transistor including the semiconductor layer can become sufficiently low. Further, variation in the thickness of the semiconductor layer within a substrate surface, which occurs due to etching, can be prevented and variation in characteristics can also be prevented.

[0035]

According to one embodiment of the present invention, a semiconductor device having characteristics which hardly shift in a GBT test can be obtained.

BRIEF DESCRIPTION OF DRAWINGS

[0036]

FIGS. 1A to 1C illustrate a method for manufacturing a semiconductor device of Embodiment 1.

FIGS. 2A to 2D illustrate a method for manufacturing a semiconductor device of Embodiment 1.

FIGS. 3A to 3D illustrate a method for manufacturing a semiconductor device of Embodiment 1.

FIGS. 4A to 4D illustrate a method for manufacturing a semiconductor device of Embodiment 2.

FIGS. 5A to 5D illustrate a method for manufacturing a semiconductor device of Embodiment 2.

FIGS. 6Ato 6F are electronic devices of Embodiment 3.

FIGS. 7Aand 7B are STEM images described in Example 1.

BEST MODE FOR CARRYING OUT THE INVENTION

[0037]

Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the following description and it is easily understood by those skilled in the art that the mode and details can be variously changed without departing from the scope and spirit of the present invention. Accordingly, the invention should not be construed

as being limited to the description of the embodiments below. In describing structures of the present invention with reference to the drawings, the same reference numerals are used in common for the same portions in different drawings. The same hatching pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases. In addition, for convenience, an insulating layer is, in some cases, not illustrated in plan views.

[0038]

Furthermore, hereinafter, ordinal numbers, such as "first" and "second," are used merely for convenience, and the present invention is not limited to the numbers.

[0039]

(Embodiment 1)

In this embodiment, a semiconductor device that is one embodiment of the present invention and a manufacturing method thereof are described. A transistor is given as an example of a semiconductor device.

[0040]

A method for manufacturing a transistor of this embodiment, which is described with reference to FIGS. 1A to 1C, FIGS. 2A to 2D, and FIGS. 3A to 3D includes the steps of forming a first wiring layer 102; forming a first insulating layer 104 to cover the first wiring layer 102; forming a semiconductor layer 105 over the first insulating layer 104; stacking a first conductive film 107A, a second conductive film 107B, and a third conductive 107C in this order over the semiconductor layer 105 to form a multilayer conductive film 107; and performing at least three-stage etching on the multilayer conductive film 107 to form separated second wiring layers 108 having a three-layer structure. The three-stage etching includes a first etching process, which is performed until at least the first conductive film 107A is exposed; a second etching process, which is performed under the condition that the etching rate for the first conductive film 107A is higher than that in the first etching process and the etching rate for the semiconductor layer 105 is lower than that in the first etching process; and a third etching process, which is performed under the condition that the etching rate for at least the multilayer conductive film 107 is higher than that in the second etching process.

[0041]

First, the first wiring layer 102 is selectively formed over a substrate 100, the first insulating layer 104 is formed to cover the first wiring layer 102, and the semiconductor layer 105 is selectively formed over the first insulating layer 104 (FIG 1A).

[0042]

A substrate having an insulative surface may be used as the substrate 100. For example, a glass substrate, a quartz substrate, a semiconductor substrate having an insulating layer formed on its surface, or a stainless steel substrate having an insulating layer formed on its surface may be used as the substrate 100.

[0043]

The first wiring layer 102 constitutes at least a gate electrode of a transistor. The first wiring layer 102 may be formed of a conductive material. The first conductive layer 102 may be formed in such a manner that a conductive film is formed and is processed by photolithography and etching.

[0044]

The first insulating layer 104 constitutes at least a gate insulating layer of the transistor. The first insulating layer 104 may be formed of silicon oxide, silicon nitride, silicon oxynitnde, or the like. When the semiconductor layer 105 is an oxide semiconductor layer, the first insulating layer 104 is preferably formed by a sputtering method so that moisture and hydrogen are removed as much as possible from the first insulating layer 104 which is in contact with the semiconductor layer 105. The first insulating layer 104 may be a single layer or a stack of a plurality of layers. The first insulating layer 104 may be formed using gallium oxide, aluminum oxide, or other oxygen-excess oxides.

[0045]

Note that "silicon oxynitride" contains more oxygen than nitrogen.

[0046]

Further, "silicon nitride oxide" contains more nitrogen than oxygen. Note that percentages of nitrogen, oxygen, silicon, and hydrogen fall within the ranges given above, where the total number of atoms contained in the silicon oxynitride or the silicon nitride oxide is defined as 100 at.%.

[0047]

Here, the semiconductor layer 105 is formed using an oxide semiconductor. The semiconductor layer 105 may be formed in such a manner that a semiconductor film is formed and is processed by photolithography and etching. For forming the semiconductor layer 105, an oxide semiconductor, which becomes an intrinsic (I-type) or substantially an intrinsic (I-type) by removing impurities to highly purify the oxide semiconductor so that impurities which are carrier donors besides main components do not exist in the oxide semiconductor as much as possible, is used.

[0048]

The highly purified oxide semiconductor layer contains extremely few carriers (close to zero), and the carrier concentration thereof is lower than 1×10^{14} /cm^3, preferably lower than 1×10^{12} /cm^3, more preferably lower than 1×10^{11} /cm^3.

[0049]

The off-state current can be small in a transistor because the number of carriers in the oxide semiconductor layer for forming the semiconductor layer 105 is extremely small. It is preferable that off-state current be as low as possible

[0050]

It is important that the state of the interface (interface state, interface charge, and the like) between the first insulating layer 104 and the semiconductor layer 105 be adjusted to be appropriate because such a highly purified oxide semiconductor is very sensitive to the interface state and interface charge. Thus, it is preferable that the first insulating layer 104 which is in contact with the highly purified oxide semiconductor have high quality. Here, the "first insulating layer 104 has high quality" means that there are few defects on the surface or inside the first insulating layer 104 and few defect levels and interface states to trap charge, and it is difficult to generate a fixed charge.

[0051]

The first insulating layer 104 is preferably formed by, for example, a high-density plasma CVD method using a microwave (e.g., a frequency of 2.45 GHz) because the first insulating layer 104 can be a dense layer having high withstand voltage. This is because a close contact between the purified oxide semiconductor layer and a

high-quality gate insulating layer reduces interface states and produces desirable interface characteristics

[0052]

Needless to say, another film formation method such as a sputtering method or a plasma CVD method can be employed as long as it enables formation of a high-quality insulating layer as the first insulating layer 104.

[0053]

As an oxide semiconductor for forming the semiconductor layer 105, the following metal oxide can be used: a four-component metal oxide such as an In-Sn-Ga-Zn-O-based oxide semiconductor; a three-component metal oxide such as an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor, an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, or a Sn-Al-Zn-O-based oxide semiconductor; a two-component metal oxide such as an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, or an In-Mg-O-based oxide semiconductor; an one-component metal oxide such as an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, or a Zn-O-based oxide semiconductor; or the like. The above oxide semiconductor may contain SiO_2. Here, for example, an In-Ga-Zn-O-based oxide semiconductor means an oxide semiconductor containing In, Ga, or Zn, and there is no particular limitation on the composition ratio thereof. Further, In-Ga-Zn-O-based oxide semiconductor may contain an element other than In, Ga, or Zn.

[0054]

An oxide semiconductor for forming the semiconductor layer 105 may be represented by the chemical formula, $InMO_3(ZnO)_m$ ($m>0$). Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, or Ga and Co. The above oxide semiconductor may contain SiO_2.

[0055]

A target containing In_2O_3, Ga_2O_3, and ZnO at a composition ratio of 1:1:1 [molar ratio] may be used for forming the oxide semiconductor film for forming the

semiconductor layer 105 by a sputtering method. Without limitation on the material and the composition of the target, for example, a target containing In_2O_3, Ga_2O_3, and ZnO at a composition ratio of 1:1:2 [molar ratio] may be used. Here, for example, an In-Ga-Zn-0 film means an oxide film containing indium (In), gallium (Ga), and zinc (Zn), and there is no particular limitation on the composition ratio.

[0056]

The oxide semiconductor film for forming the semiconductor layer 105 is formed by a sputtering method with use of an In-Ga-Zn-O-based oxide semiconductor target. Further, the semiconductor layer 105 can be formed by a sputtering method under a rare gas (e.g., Ar) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas and an oxygen gas.

[0057]

Further, the filling rate of the target is 90 % to 100 % inclusive, preferably 95 % to 99.9 % inclusive. With the use of the target having a high filling rate, the oxide semiconductor film to be formed can be a dense film.

[0058]

Next, first heat treatment is performed on the semiconductor layer 105. The oxide semiconductor layer can be dehydrated or dehydrogenated by the first heat treatment. The temperature of the first heat treatment is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. In this embodiment, heat treatment may be performed in a nitrogen gas atmosphere at 450 °C for one hour as the first heat treatment. Note that there is no particular limitation on timing of the first heat treatment as long as it is after formation of the oxide semiconductor layer. Further, the atmosphere for performing the first heat treatment may be not only a nitrogen gas atmosphere, but also a mixed gas atmosphere containing an oxygen gas and a nitrogen gas, an oxygen gas atmosphere, and an atmosphere from which moisture is sufficiently removed (dry air). After the first heat treatment, the oxide semiconductor layer is preferably processed without exposure to the air so that water or hydrogen can be prevented from reentering the oxide semiconductor layer

[0059]

Dehydration or dehydrogenation may be performed on the first insulating layer

104 in advance by performing preheating before the semiconductor layer 105 is formed.

[0060]

It is preferable that remaining moisture and hydrogen in a film-formation chamber be sufficiently removed before the semiconductor film to be the semiconductor layer 105 is formed. That is, before formation of the semiconductor film for forming the semiconductor layer 105, evacuation is preferably performed with an entrapment vacuum pump (e.g., a cryopump, an ion pump, or a titanium sublimation pump).

[0061]

Next, the multilayer conductive film 107 is formed to cover the first insulating layer 104 and the semiconductor layer 105 (FIG IB).

[0062]

The multilayer conductive film 107 includes the first conductive film 107A, the second conductive film 107B, and the third conductive film 107C in this order from the substrate 100 side. The first conductive film 107A, the second conductive film 107B, and the third conductive film 107C may be each formed of a conductive material. As a conductive material for forming the first conductive film 107A and the second conductive film 107C, Ti, W, Mo or Ta, or a nitride thereof can be given, for example. As a conductive material for forming the second conductive film 107B, Al is given, for example.

[0063]

Next, a resist mask 109 is selectively formed over the multilayer conductive film 107 (FIG 1C). The resist mask 109 may be formed by photolithography.

[0064]

Next, etching is performed on the multilayer conductive film 107 using the resist mask 109, whereby the second wiring layer 108 is formed. The second wiring layer 108 constitute at least source and drain electrodes of a transistor. The etching process for forming the second wiring layer 108 includes three-stage etching. Here, the first to the third etching processes for forming the second wiring layer 108 are described with reference to FIGS. 2A to 2D, paying attention to a region in FIG 1C surrounded by a dotted frame.

[0065]

First, using the resist mask 109 (FIG 2A), the multilayer conductive film 107 is

etched until at least the first conductive film 107A is exposed (the first etching process). Here, the first conductive film 107A is etched, whereby a first conductive film 107D is formed. The first conductive film 107D exists over the entire surface of the first insulating layer 104 and the semiconductor layer 105, and there is no particular limitation on the etching depth of the first conductive film 107A as long as the insulating layer 104A and the semiconductor layer 105 are not exposed (FIG. 2B). Note that a portion of the second conductive film 107B, which does not overlap with the resist mask 109, is etched, whereby a second conductive film 107E is formed. Further, a portion of the third conductive film 107C, which does not overlap with the resist mask 109, is etched, whereby a third conductive film 107F is formed.

[0066]

Note that the first etching process may be performed in a gas atmosphere containing a large amount of chlorine as its main component (a larger amount of chlorine than fluorine). Here, as an example of the gas containing a large amount of chlorine, a $CC1_4$ gas, a $SiCl_4$ gas, a $BC1_3$ gas, or a Cl_2 gas can be given. Specifically, a mixed gas of a $BC1_3$ gas and a Cl_2 gas is preferably used.

[0067]

Then, the first conductive film 107D is etched until the first insulating layer 104 and the semiconductor layer 105 are exposed, whereby a first conductive film 107G is formed (the second etching process). Here, the third conductive film 107F is etched because of recession of the resist, whereby a conductive film 107H is formed. Note that in the second etching process, it is only necessary that at least the first insulating layer 104 and the semiconductor layer 105 are exposed and the exposed semiconductor layer 105 is not removed by the etching (FIG 2C).

[0068]

Note that the second etching process may be performed in a gas atmosphere containing a large amount of fluorine as its main component (a larger amount of fluorine than chlorine). Here, as an example of the gas containing a large amount of fluorine, a CF_4 gas, a SF_6 gas, a NF_3 gas, a $CBrF_3$ gas, **$CF3SO_3H$** gas, or C_3F_8 can be given. Specifically, a SF_6 gas is preferably used.

[0069]

As described above, it is known that the gas containing a large amount of

fluorine as its main component (specifically, a SF_6 gas) has a high etching rate for a resist mask and reduce the size of the resist mask (the resist mask is made to recede). Thus, the resist mask 109 is reduced in size by the second etching, whereby a resist mask 109C is formed. Further, by the reduction in size of the resist mask 109, a portion of the third conductive film 107F, which does not overlap with the resist mask 109C, is also etched. However, in the case where the second conductive film 107E is formed of a material containing Al as its main component, for example, the second conductive film 107E is not etched.

[0070]

However, the present invention is not limited thereto, and a portion of the second conductive film 107E, which does not overlap with the resist mask 109C may be etched.

[0071]

Next, etching is performed so that portions of the second wiring layers 108, which overlap with the semiconductor layer 105, are completely separated from each other. It is preferable that the semiconductor layer 105 be slightly etched (the third etching process). Here, the first conductive film 107G is etched to be a first layer 108A; the second conductive film 107E is etched to be a second layer 108B; and the third conductive film 107H is etched to be a third layer 108C (FIG 2D). The etching depth of the semiconductor layer 105 is preferably greater than or equal to 0 nm to less than or equal to 5 nm.

[0072]

Note that the third etching process may be performed in a gas atmosphere containing a large amount of chlorine as its main component (a larger amount of chlorine than fluorine). Here, as an example of the gas containing a large amount of chlorine, a $CC1_4$ gas, a $SiCl_4$ gas, a $BC1_3$ gas, or a Cl_2 gas can be given. Specifically, a mixed gas of a $BC1_3$ gas and a Cl_2 gas is preferably used.

[0073]

As described above, the multilayer conductive film 107 is etched to form the second wiring layers 108, so that the separated second wiring layers 108 can be formed while the thickness of the semiconductor layer 106 in a portion to be a channel formation region is kept. By forming the second wiring layers 108 using such an

etching method, variation in thickness of the semiconductor layer 106 in the portion to be a channel formation region within the substrate surface can be small even when the substrate 100 has a large area.

[0074]

Then, the resist mask 109C is removed. As explained above, the transistor according to this embodiment is achieved (FIG 3B).

[0075]

Further, the transistor shown in FIG 3B is provided over the substrate 100 and includes the first wiring layer 102, the first insulating layer 104 formed to cover the first wiring layer 102, the semiconductor layer 106 formed over the first insulating layer 104, and the second wiring layer 108 formed to cover the semiconductor layer 106. The thickness (hereinafter, "first thickness") of a portion of the semiconductor layer 106, which does not overlap with the second wiring layer 108, is smaller than the thickness (hereinafter, "the second thickness") of a portion of the semiconductor layer 106, which overlaps with the second wiring layer 108. The difference between the first and second thicknesses may be greater than or equal to 0 nm and less than or equal to 10 nm, preferably greater than or equal to 0 nm and less than or equal to 5 nm.

[0076]

Further, the second wiring layer 108 includes the first layer 108A, the second layer 108B, and the third layer 108C. A side surface of the second wiring layer 108 includes a first side surface which has a side surface of the first layer 108A and part of a side surface of second layer 108B (upper portion), and a second side surface which has part of the side surface of the second layer 108B (lower portion) and a side surface of the third layer 108C. In other words, the second wiring layer 108 has a three-layer structure, and the side surface of the second wiring layer 108 is formed in a stepped shape.

[0077]

Further, in the transistor shown in FIG 3B, the on-state current of the transistor can be sufficiently large because the thickness of the semiconductor layer 106 can be kept thick, and the off-state current of the transistor can be sufficiently small through the third etching process. Further, even when the transistor 100 has a large area, it is possible to achieve a transistor in which variation in characteristics and variation in

thickness of the semiconductor layer within the substrate surface due to etching are small.

[0078]

The thickness of the semiconductor layer 106 may depend on the relationship with the thickness of the first insulating layer 104. When the thickness of the first insulating layer 104 is 100 nm, the thickness of the semiconductor layer 106 may be approximately greater than or equal to 15 nm. The reliability of the transistor may be improved when the thickness of the semiconductor layer 106 is greater than or equal to 25 nm. The thickness of the semiconductor layer 106 is preferably 30 nm to 40 nm.

[0079]

Meanwhile, a second insulating layer 110 is formed further in the transistor shown in FIG 3B (FIG 3C).

[0080]

The second insulating layer 110 may be formed of silicon oxide, silicon nitride, silicon oxynitride or the like, and is preferably formed by a sputtering method. It is because water or hydrogen can be prevented from reentering the semiconductor layer 106. Specifically, a portion of the second insulating layer 110, which is in contact with the semiconductor layer 106, is preferably formed of silicon oxide. Otherwise, when the second insulating layer 110 has a structure having a plurality of stacked layers, at least a layer, which is in contact with the semiconductor layer 106, may be formed of silicon oxide, and an organic resin layer or the like may be formed over the silicon oxide layer.

[0081]

Next, second heat treatment (preferably at greater than or equal to 200 °C and less than or equal to 400 °C, for example, greater than or equal 250 °C and less than or equal to 350 °C) is performed in an inert gas atmosphere, or an oxygen gas atmosphere. For example, the second heat treatment is performed in a nitrogen gas atmosphere at 250 °C for one hour. In the second heat treatment, heat is applied while part of the oxide semiconductor layer (a channel formation region) is in contact with the second insulating layer 110. Further, the second heat treatment may be performed after forming the second insulating layer 110. However, the timing is not limited thereto.

[0082]

Further, the third wiring layer 112 is selectively formed over the second insulating layer 110 to overlap with the channel formation region of the semiconductor layer 106 (FIG. 3D). Because the third wiring layer 112 functions as a back gate, it may be formed of conductive material. The third wiring layer 112 may be an electrically independent wiring, electrically connected to the first wiring layer 102, or floating. The third wiring layer 112 can be formed using a material and a method which are similar to those of the first wiring layer 102

[0083]

When the third wiring layer 112 is an electrically independent wiring, it may function as a back gate which does not depend on the potential of the first wiring layer 102. In this case, it is possible to control the threshold voltage by the back gate.

[0084]

When the third wiring layer 112 is electrically connected to the first wiring layer 102, the potential of the third wiring layer 112 can be equal to the potential of the first wiring layer 102 or the potential in accordance with the potential of the first wiring layer 102. When the third wiring layer 112 is set to the potential in accordance with the potential of the first wiring layer 102, a resistor may be provided between a gate formed using the first wiring layer 102 and a back gate formed using the third wiring layer 112. At this time, the current per unit area when the transistor is on can be increased.

[0085]

When the third wiring layer 112 is floating, the third wiring layer 112 cannot function as a back gate, but it is possible to function as an additional protection layer for the semiconductor layer 106.

[0086]

Further, a transistor having the semiconductor layer 106, which is a highly purified oxide semiconductor layer, can decrease the current in an off state (off-state current) to a level under 10 ζA/μπι per 1 μm of the channel width, under 100 ζA/μπι at 85 °C. That is, the off-state current can be lowered to be around the measurement limit or below the measurement limit.

[0087]

(Embodiment 2)

The present invention is not limited to the mode described in Embodiment 1. For example, a transistor may have a TGTC structure as a semiconductor device of one embodiment of the present invention.

[0088]

A method for manufacturing a transistor according to one embodiment of the present invention, described with reference to FIGS. 4A to 4D, and FIGS. 5A to 5D includes the steps of forming a semiconductor layer 205; stacking a first conductive film 207A, a second conductive film 207B, and a third conductive film 207C in this order over the semiconductor layer 205 to form a multilayer conductive film 207; performing at least three-stage etching on the multilayer conductive film 207 to form separated first wiring layers 208 having a three-layer structure and to form a semiconductor layer 206 at the same time; forming an insulating layer 210 so as to cover the first wiring layer 208 and the semiconductor layer 206; and forming a second wiring layer 212 over the semiconductor layer 210 to overlap with the semiconductor layer 206. The three-stage etching includes the first etching process, which is performed until at least the first conductive film 207A is exposed; the second etching process, which is performed under the condition that the etching rate for the first conductive film 207A is higher than that in the first etching process and the etching rate for the semiconductor layer 205 is lower than that in the first etching process; and the third etching process, which is performed under the condition that the etching rate for at least the multilayer conductive film 207 is higher than that in the second etching process.

[0089]

First, a base insulating layer 204 is preferably formed over the substrate 200, and the semiconductor layer 205 is selectively formed over the substrate 200 or the base insulating layer 204 (FIG. 4A).

[0090]

The substrate 200 may be the same as the substrate 100 of Embodiment 1.

[0091]

The base insulating layer 204 can be formed of the same material and by the same method as the first insulating layer 104 of Embodiment 1.

[0092]

The semiconductor layer 205 can be formed of the same material and by the same method as the semiconductor layer 105 of Embodiment 1.

[0093]

Next, the multilayer conductive film 207 is formed over the base insulating layer 204 and the semiconductor layer 205, and a resist mask 209 is selectively formed over the multilayer conductive film 207 (FIG 4A).

[0094]

The multilayer conductive film 207 can be formed of the same material and by the same method as the multilayer conductive film 107 of Embodiment 1.

[0095]

The resist mask 209 can be formed by photolithography as the resist mask 109 of Embodiment 1.

[0096]

Next, etching is performed on the multilayer conductive film 207 using the resist mask 209, whereby the first wiring layer 208 is formed. The first wiring layer 208 constitute at least source and drain electrodes of a transistor. The etching process for forming the first wiring layer 208 includes three-stage etching. Here, the first to the third etching processes for forming the first wiring layer 208 are described with reference to FIGS. 5A to 5D, paying attention to a region in FIG. 4A surrounded by a dotted frame.

[0097]

First, using the resist mask 209 (FIG 5A), the multilayer conductive film 207 is etched until at least the first conductive film 207A is exposed (the first etching process). Here, the first conductive film 207A is etched, whereby a first conductive film 207D is formed. The first conductive film 207D exists over the entire surface of the base insulating layer 204 and the semiconductor layer 205, and there is no particular limitation on the etching depth of the first conductive film 207A as long as the base insulating layer 204 and the semiconductor layer 205 are not exposed (FIG. 5B). Note that a portion of the second conductive film 207B, which does not overlaps with the resist mask 209 is etched, whereby a second conductive film 207E is formed. Further, a portion of the third conductive film 207C, which does not overlap with the resist mask

209 is etched, whereby a third conductive film 207F is formed.

[0098]

Note that the first etching process may be performed in a gas atmosphere containing a large amount of chlorine as its main component (a larger amount of chlorine than fluorine). Here, as an example of the gas containing a large amount of chlorine, a $CC1_4$ gas, a $SiCl_4$ gas, a $BC1_3$ gas, or a Cl_2 gas can be given. Specifically, a mixed gas of a $BC1_3$ gas and a Cl_2 gas is preferably used.

[0099]

Next, the first conductive film 207D is etched until the base insulating layer 204 and the semiconductor layer 205 are exposed, whereby a first conductive film 207G is formed (the second etching process). Here, the third conductive film 207F is etched because of the recession of the resist, whereby a conductive film 207H is formed. Note that in the second etching process, it is only necessary that at least the base insulating layer 204 and the semiconductor layer 205 are exposed and the exposed semiconductor layer 205 is not removed by the etching (FIG 5C).

[0100]

Note that the second etching process may be performed in a gas atmosphere containing a large amount of fluorine as its main component (a larger amount of fluorine than chlorine). Here, as an example of the gas containing a large amount of fluorine, a CF_4 gas, a SF_6 gas, a NF_3 gas, a $CBrF_3$, a CF_3S0_3H gas, or a C_3F_8 gas can be given. Specifically, a SF_6 gas is preferably used.

[0101]

As described above, it is known that the gas containing a large amount of fluorine as its main component (specifically, a SF_6 gas) has a high etching rate for a resist mask and reduce the size of the resist mask (the resist mask is made to recede). Thus, the resist mask 209 is reduced in size by the second etching, whereby resist mask 209C is formed. Further, by the reduction in size of the resist mask 209, a portion of the third conductive film 207F, which does not overlap with the resist mask 209C, is also etched. However, in the case where the second conductive film 207E is formed of a material containing Al as its main component, for example, the second conductive film 207E is not etched.

[0102]

However, the present invention is not limited thereto, and a portion of the second conductive film 207E, which does not overlap with the resist mask 209C, may be etched.

[0103]

Next, etching is performed so that portions of the second wiring layers 208, which overlap with the semiconductor layer 205, are completely separated from each other. It is preferable that the semiconductor layer 205 be slightly etched (the third etching process). Here, the first conductive film 207G is etched to be a first layer 208A; the second conductive film 207D is etched to be a second layer 208B; and the third conductive film 207H is etched to be a third layer 208C (FIG. 5D). The etching depth of the semiconductor layer 205 is preferably greater than or equal to 0 nm to less than or equal to 5 nm.

[0104]

Note that the third etching process may be performed in a gas atmosphere containing a large amount of chlorine as its main component (a larger amount of chlorine than fluorine). Here, as an example of the gas containing a large amount of chlorine, a $CC1_4$ gas, a $SiCl_4$ gas, a $BC1_3$ gas, or a Cl_2 gas can be given. Specifically, a mixed gas of a **BCI3** gas and a Cl_2 gas is preferably used.

[0105]

As described above, the multilayer conductive film 207 is etched to form the first wiring layers 208, so that the separated first wiring layers 208 can be formed while the thickness of the semiconductor layer 206 in a portion to be a channel formation region is kept. By forming the first wiring layer 208 using such an etching method, variation in thickness of the semiconductor layer 206 in the portion to be a channel formation region within the substrate surface can be small even when the substrate 200 has a large area.

[0106]

After that, the resist mask 209C is removed (FIG 4C).

[0107]

Then, the insulating layer 210 is formed over the first wiring layers 208, the semiconductor layer 206, and the base insulating layer 204 (FIG. 4D). The insulating layer 210 constitutes at least a gate insulating layer of the transistor.

[0108]

The insulating layer 210 can be formed of the same material and by the same method as the first insulating layer 104 of Embodiment 1. Thus, the first insulating layer 210 may be formed using gallium oxide, aluminum oxide, or other oxygen-excess oxides.

[0109]

Next, the second wiring layer 212 is selectively formed over the insulating layer 210 to overlap with at least the semiconductor layer 206 (FIG 4D). The second wiring layer 212 constitutes at least a gate electrode of the transistor. As such, the transistor according to this embodiment is achieved (FIG 4D).

[0110]

Further, the transistor shown in FIG 4D includes the semiconductor layer 206, the separated first wiring layers 208, over the semiconductor layer 206, the insulating layer 210 formed to cover the first wiring layer 208, and the second wiring layer 212 provided over the insulating layer 210. The thickness (hereinafter, "first thickness") of a portion of the semiconductor layer 206, which does not overlap with the first wiring layer 208, is smaller than the thickness (hereinafter, "the second thickness") of a portion of the semiconductor layer 206, which overlaps with the first wiring layer 208. The difference between the first and second thicknesses may be greater than or equal to 0 nm and less than or equal to 10 nm, preferably greater than equal to 0 nm and less than or equal to 5 nm.

[Qui]

Further, the first wiring layer 208 includes the first layer 208A, the second layer 208B, and the third layer 208C. A side surface of the first wiring layer 208 includes a first side surface which has a side surface of the first layer 208A and part of a side surface of the first layer 208B (upper portion), and a second side surface which has part of the side surface of the second layer 208B (lower portion) and a side surface of the third layer 208C. In other words, the first wiring layer 208 has a three-layer structure, and the side surface of the second wiring layer 208 is formed in a stepped shape.

[0112]

Further, in the transistor shown in FIG 4D, the on-state current of the transistor

can be sufficiently large because the thickness of the semiconductor layer 206 can be kept thick, and the off-state current of the transistor can be sufficiently small through the third etching process. Further, even when the transistor 200 has a large area, it is possible to achieve a transistor in which variation in characteristics and variation in thickness of the semiconductor layer within the substrate surface due to etching are small.

[0113]

The thickness of the semiconductor layer 206 may depend on the relationship with the thickness of the insulating layer 210. When the thickness of the insulating layer 210 is 100 nm, the thickness of the semiconductor layer 206 may be approximately greater than or equal to 15 nm. The reliability of the transistor may be improved when the thickness of the semiconductor layer 206 is greater than or equal to 25 nm. The thickness of the semiconductor layer 206 is preferably greater than or equal to 25 nm and less than or equal to 50 nm.

[0114]

As explained in this embodiment, a transistor having a TGTC structure may be manufactured by adjusting the thickness of the semiconductor layer.

[0115]

Further, although not illustrated, a back gate may be provided between the base insulating layer 204 and the substrate 200 to overlap with the semiconductor layer 206. Disposing the back gate in this manner may provide the same effect as forming the third wiring layer 112 in Embodiment 1.

[0116]

Note that the oxide semiconductor layer is highly purified also in this embodiment. Further, a transistor having the semiconductor layer 206, which is a highly purified oxide semiconductor layer, can decrease the current in an off state (off-state current) to a level under 10 ζA/μπι per 1 μπι of the channel width, under 100 ζA/μπι at 85 °C. That is, the off-state current can be lowered to be around the measurement limit or below the measurement limit.

[0117]

However, the present invention is not limited to the modes described in

Embodiments 1 and 2, and can be changed as appropriate within the range without depart from the spirit of the present invention. For example, the transistor may have a BGBC structure or a TGBC structure.

[0118]

(Embodiment 3)

Next, electronic devices according to an embodiment of the present invention will be described. In the electronic devices of this embodiment, at least one of transistors described in Embodiments 1 and 2 is mounted. Examples of the electronic devices of the present invention include a computer, a mobile phone (also referred to as a cellular phone or a mobile phone device), a portable information terminal (including a portable game machine, an audio reproducing device, and the like), a digital camera, a digital video camera, electronic paper, and a television device (also referred to as a television or a television receiver). For example, the transistor described in Embodiment 1 or 2 may be used as a pixel transistor constituting a pixel portion of such an electronic device.

[0119]

FIG 6A illustrates a laptop personal computer, which includes a housing 301, a housing 302, a display portion 303, a keyboard 304, and the like. The transistor described in either Embodiment 1 or 2 is provided in the housings 301 and 302. By mounting the transistor described in Embodiment 1 or 2 on the laptop personal computer illustrated in FIG 6A, display unevenness of the display portion can be reduced and reliability can be improved.

[0120]

FIG 6B illustrates a portable information terminal (PDA), which includes a display portion 313, an external interface 315, an operation button 314, and the like in a main body 311. Further, a stylus 312 for operating the portable information terminal or the like is provided. The transistor described in either Embodiment 1 or 2 is provided in the main body 311. By mounting the transistor described in Embodiment 1 or 2 on the PDA illustrated in FIG 6B, display unevenness of the display portion can be reduced and reliability can be improved.

[0121]

FIG 6C illustrates an e-book reader 320 mounted with electronic paper, which

includes two housings of a housing 321 and a housing 323. The housing 321 and the housing 323 include a display portion 325 and a display portion 327, respectively. The housing 321 is combined with the housing 323 by a hinge 337, so that the e-book reader 320 can be opened and closed using the hinge 337 as an axis. The housing 321 is provided with a power switch 331, operation keys 333, a speaker 335, and the like. At least one of the housing 321 and the housing 323 is provided with the transistor described in either Embodiment 1 or 2. By mounting the transistor described in Embodiment 1 or 2 on the e-book reader illustrated in FIG. 6C, display unevenness of the display portion can be reduced and reliability can be improved.

[0122]

FIG. 6D illustrates a mobile phone which includes two housings of a housing 340 and a housing 341. Moreover, the housings 340 and 341 which are shown unfolded in FIG 6D can overlap with each other by sliding. Thus, the mobile phone can be in a suitable size for portable use. The housing 341 includes a display panel 342, a speaker 343, a microphone 344, a pointing device 346, a camera lens 347, an external connection terminal 348, and the like. The housing 340 is provided with a solar cell 349 for charging the mobile phone, an external memory slot 350, and the like. In addition, an antenna is incorporated in the housing 341. At least one of the housing 340 and the housing 341 is provided with the transistor described in either Embodiment 1 or Embodiment 2. By mounting the transistor described in Embodiment 1 or 2 on the mobile phone illustrated in FIG 6D, display unevenness of the display portion can be reduced and reliability can be improved.

[0123]

FIG 6E illustrates a digital camera which includes a main body 361, a display portion 367, an eyepiece 363, an operation switch 364, a display portion 365, a battery 366, and the like. The transistor described in either Embodiment 1 or 2 is provided in the main body 361. By mounting the transistor described in Embodiment 1 or 2 on the digital camera illustrated in FIG 6E, display unevenness of the display portion can be reduced and reliability can be improved.

[0124]

FIG 6F is a television set 370 which includes a housing 371, a display portion 373, a stand 375, and the like. The television set 370 can be operated by an operation

switch included in the housing 371 or by a remote controller 380. In the housing 371 or the remote controller 380, the transistor described in either Embodiment 1 or 2 is mounted. By mounting the transistor described in Embodiment 1 or 2 on the television set illustrated in FIG 6F, display unevenness of the display portion can be reduced and reliability can be improved.

[Example 1]

[0125]

In this example, the transistor of Embodiment 1, that is, the transistor shown in FIG 3B is actually fabricated, and STEM images of a cross section of the transistor are illustrated.

[0126]

A glass substrate was used as the substrate 100. Note that, a base insulating layer was formed using silicon oxynitride between the substrate 100 and the first wiring layer 102.

[0127]

The first wiring layer 102 was formed of tungsten and had a thickness of 150 nm.

[0128]

The first insulating layer 104 was formed of a silicon oxynitride and had a thickness of 100 nm.

[0129]

The semiconductor layer 106 was formed of an In-Ga-Zn-O-based oxide semiconductor and had a thickness of 50 nm.

[0130]

The first layer 108A of the second wiring layer was formed of Ti and had a thickness of 100 nm. The second layer 108B of the second wiring layer was formed of Al and had a thickness of 200 nm. The third layer 108C of the second wiring layer was formed of Ti and had a thickness of 50 nm.

[0131]

The second insulating layer 110 was formed of a silicon oxide and had a thickness of 300 nm.

[0132]

Here, two kinds of samples were prepared for comparison.

[0133]

As for a first sample, etching for processing the multilayer conductive film 107 to form the second wiring layer 108 is performed using only a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

[0134]

As for a second sample, three-stage etching for processing the multilayer conductive film 107 to form the second wiring layer 108 was performed. The first etching process was performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas; the second etching process was performed using only a SF_6 gas; the third etching process was performed using a mixture gas of a **BCI3** gas and a Cl_2 gas.

[0135]

FIG 7A is a cross-sectional STEM image of the side surface of the second wiring layer 108 in the first sample. FIG 7B is a cross-sectional STEM image of the side surface of the second wiring layer 108 in the second sample.

[0136]

In the first sample, the difference between the first and second thicknesses of the semiconductor layer 106 was approximately 20 nm. In the second sample, the difference between the first and second thicknesses of the semiconductor layer 106 was approximately 10 nm. In other words, by the three-stage etching that is one embodiment of the present invention, the etching depth of the layer provided below and in contact with the film to be etched was able to limit to approximately 10 nm while the layer provided below and in contact with the film to be etched was etched by 20 nm in a conventional method.

EXPLANATION OF REFERENCE

[0137]

100: substrate, 102: first wiring layer, 104: first insulating layer, 105: semiconductor layer, 106: semiconductor layer, 107: multilayer conductive film, 107A: first conductive film, 107B: second conductive film, 107C: third conductive film, 107D: first conductive film, 107E: second conductive film, 107F: third conductive film, 107G: first conductive film, 107H: third conductive film, 108: second wiring layer, 108A: first layer of second

wiring layer, 108B: second layer of second wiring layer, 108C: third layer of second wiring layer, 109: resist mask, 109C: resist mask, 110: second insulating layer, 112: third wiring layer, 200: substrate, 204: base insulating layer, 205: semiconductor layer, 206: semiconductor layer, 207: multilayer conductive film, 207A: first conductive film, 207B: second conductive film, 207C: third conductive film, 207D: first conductive film, 207E: second conductive film, 207F: third conductive film, 207G: first conductive film, 207H: third conductive film, 208: first wiring layer, 208A: first layer of first wiring layer, 208B: second layer of first wiring layer, 208C: third layer of first wiring layer, 209: resist mask, 209C: resist mask, 210: insulating layer, 212: second wiring layer, 301: housing, 302: housing, 303: display portion, 304: keyboard, 311: main body, 312: stylus, 313: display portion, 314: operation button, 315: external interface, 320: e-book reader, 321: housing, 323: housing, 325: display portion, 327: display portion, 331: power switch, 333: operation key, 335: speaker, 337: hinge, 340: housing, 341: housing, 342: display panel, 343: speaker, 344: microphone, 346: pointing device, 347: camera lens, 348: external connection terminal, 349: solar cell, 350: external memory slot, 361: main body, 363: eyepiece, 364: operation switch, 365: display portion, 366: battery, 367: display portion, 370: television set, 371: housing, 373: display portion, 375: stand, 380: remote controller.

This application is based on Japanese Patent Application serial no. 2010-150012 filed with Japan Patent Office on June 30, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a first wiring layer;

forming an insulating layer to cover the first wiring layer;

forming a semiconductor layer over the insulating layer;

stacking a first conductive film, a second conductive film, and a third conductive in this order over the semiconductor layer; and

performing at least three-stage etching on the first to third conductive films to form a second wiring layer having a three-layer structure,

wherein the three-stage etching comprises:

a first etching process, which is performed until the first conductive film is exposed;

a second etching process, which is performed under a condition that an etching rate for the first conductive film is higher than the etching rate in the first etching process and an etching rate for the semiconductor layer is lower than the etching rate in the first etching process; and

a third etching process, which is performed under the condition that etching rates for the first to the third conductive films are higher than the etching rates in the second etching process.

2. The method for manufacturing a semiconductor device according to claim 1, wherein the first and the second conductive films are thicker than the third conductive film.

3. The method for manufacturing a semiconductor device according to claim 1, wherein a conductive material for forming the second conductive film has higher conductivity than a conductive material for forming the first conductive film and the third conductive film.

4. The method for manufacturing a semiconductor device according to claim 1, wherein the first conductive film and the third conductive film are titanium films and

the second conductive film is an aluminum film.

5. The method for manufacturing a semiconductor device according to claim 1,

wherein the first etching process is performed using a gas containing more chlorine than fluorine as its main component;

wherein the second etching process is performed using a gas containing more fluorine than chlorine as its main component; and

wherein the third etching process is performed using a gas containing more chlorine than fluorine as its main component.

6. The method for manufacturing a semiconductor device according to claim 5, wherein the first etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

7. The method for manufacturing a semiconductor device according to claim 5, wherein the second etching process is performed using a SF_6 gas.

8. The method for manufacturing a semiconductor device according to claim 5, wherein the third etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

9. The method for manufacturing a semiconductor device according to claim 5, wherein the third etching process is performed in a shorter time than the first etching process.

10. A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer;

stacking a first conductive film, a second conductive film, and a third conductive in this order over the semiconductor layer;

performing at least three-stage etching on the first to third conductive films to form a first wiring layer having a three-layer structure;

forming an insulating layer to cover the first wiring layer and the semiconductor layer; and

forming a second wiring layer to overlap with the semiconductor layer over the insulating layer; and

wherein the three-stage etching comprises:

a first etching process, which is performed until the first conductive film is exposed;

a second etching process, which is performed under a condition that an etching rate for the first conductive film is higher than the etching rate in the first etching process and an etching rate for the semiconductor layer is lower than the etching rate in the first etching process; and

a third etching process, which is performed under the condition that etching rates for the first to the third conductive films are higher than the etching rates in the second etching process.

11. The method for manufacturing a semiconductor device according to claim 10, wherein the first and the second conductive films are thicker than the third conductive film.

12. The method for manufacturing a semiconductor device according to claim 10, wherein a conductive material for forming the second conductive film has higher conductivity than a conductive material for forming the first conductive film and the third conductive film.

13. The method for manufacturing a semiconductor device according to claim 10, wherein the first conductive film and the third conductive film are titanium films and the second conductive film is an aluminum film.

14. The method for manufacturing a semiconductor device according to claim 10,

wherein the first etching process is performed using a gas containing more chlorine than fluorine as its main component;

wherein the second etching process is performed using a gas containing more fluorine than chlorine as its main component; and

wherein the third etching process is performed using a gas containing more chlorine than fluorine as its main component.

15. The method for manufacturing a semiconductor device according to claim 14, wherein the first etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

16. The method for manufacturing a semiconductor device according to claim 14, wherein the second etching process is performed using a SF_6 gas.

17. The method for manufacturing a semiconductor device according to claim 14, wherein the third etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

18. The method for manufacturing a semiconductor device according to claim 14, wherein the third etching process is performed in a shorter time than the first etching process.

19. A method for manufacturing a semiconductor device comprising the steps of:

forming a first wiring layer;

forming an insulating layer to cover the first wiring layer;

forming an oxide semiconductor layer over the insulating layer;

stacking a first conductive film, a second conductive film, and a third conductive in this order over the oxide semiconductor layer; and

performing at least three-stage etching on the first to third conductive films to form a second wiring layer having a three-layer structure,

wherein the three-stage etching comprises:

a first etching process, which is performed until the first conductive film is exposed;

a second etching process, which is performed under a condition that an etching rate for the first conductive film is higher than the etching rate in the first etching process and an etching rate for the oxide semiconductor layer is lower than the etching rate in the first etching process; and

a third etching process, which is performed under the condition that etching rates for the first to the third conductive films are higher than the etching rates in the second etching process.

20. The method for manufacturing a semiconductor device according to claim 19, wherein the first and the second conductive films are thicker than the third conductive film.

21. The method for manufacturing a semiconductor device according to claim 19, wherein a conductive material for forming the second conductive film has higher conductivity than a conductive material for forming the first conductive film and the third conductive film.

22. The method for manufacturing a semiconductor device according to claim 19, wherein the first conductive film and the third conductive film are titanium films and the second conductive film is an aluminum film.

23. The method for manufacturing a semiconductor device according to claim 19, wherein a material of the oxide semiconductor layer is IGZO.

24. The method for manufacturing a semiconductor device according to claim 19,

wherein the first etching process is performed using a gas containing more chlorine than fluorine as its main component;

wherein the second etching process is performed using a gas containing more fluorine than chlorine as its main component; and

wherein the third etching process is performed using a gas containing more chlorine than fluorine as its main component.

25. The method for manufacturing a semiconductor device according to claim 24, wherein the first etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

26. The method for manufacturing a semiconductor device according to claim 24, wherein the second etching process is performed using a SF_6 gas.

27. The method for manufacturing a semiconductor device according to claim 24, wherein the third etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

28. The method for manufacturing a semiconductor device according to claim 24, wherein the third etching process is performed in a shorter time than the first etching process.

29. A method for manufacturing a semiconductor device comprising the steps of:

forming an oxide semiconductor layer;

stacking a first conductive film, a second conductive film, and a third conductive in this order over the oxide semiconductor layer;

performing at least three-stage etching on the first to third conductive films to form a first wiring layer having a three-layer structure;

forming an insulating layer to cover the first wiring layer and the oxide semiconductor layer; and

forming a second wiring layer to overlap with the oxide semiconductor layer over the insulating layer; and

wherein the three-stage etching comprises:

a first etching process, which is performed until the first conductive film is exposed;

a second etching process, which is performed under a condition that an etching rate for the first conductive film is higher than the etching rate in the first etching

process and an etching rate for the oxide semiconductor layer is lower than the etching rate in the first etching process; and

a third etching process, which is performed under the condition that etching rates for the first to the third conductive films are higher than the etching rates in the second etching process.

30. The method for manufacturing a semiconductor device according to claim 29, wherein the first and the second conductive films are thicker than the third conductive film.

31. The method for manufacturing a semiconductor device according to claim 29, wherein a conductive material for forming the second conductive film has higher conductivity than a conductive material for forming the first conductive film and the third conductive film.

32. The method for manufacturing a semiconductor device according to claim 29, wherein the first conductive film and the third conductive film are titanium films and the second conductive film is an aluminum film.

33. The method for manufacturing a semiconductor device according to claim 29, wherein a material of the oxide semiconductor layer is IGZO.

34. The method for manufacturing a semiconductor device according to claim 29,

wherein the first etching process is performed using a gas containing more chlorine than fluorine as its main component;

wherein the second etching process is performed using a gas containing more fluorine than chlorine as its main component; and

wherein the third etching process is performed using a gas containing more chlorine than fluorine as its main component.

35. The method for manufacturing a semiconductor device according to claim

34, wherein the first etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

36. The method for manufacturing a semiconductor device according to claim 34, wherein the second etching process is performed using a SF_6 gas.

37. The method for manufacturing a semiconductor device according to claim 34, wherein the third etching process is performed using a mixture gas of a $BC1_3$ gas and a Cl_2 gas.

38. The method for manufacturing a semiconductor device according to claim 34, wherein the third etching process is performed in a shorter time than the first etching process.

FIG. 1A

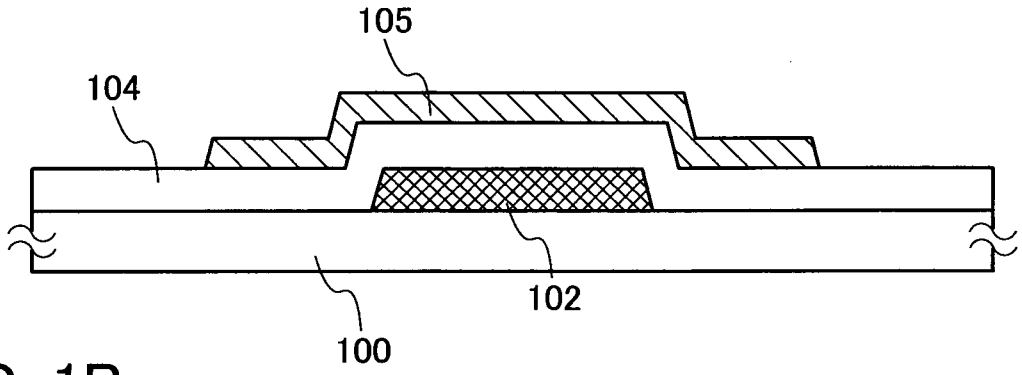


FIG. 1B

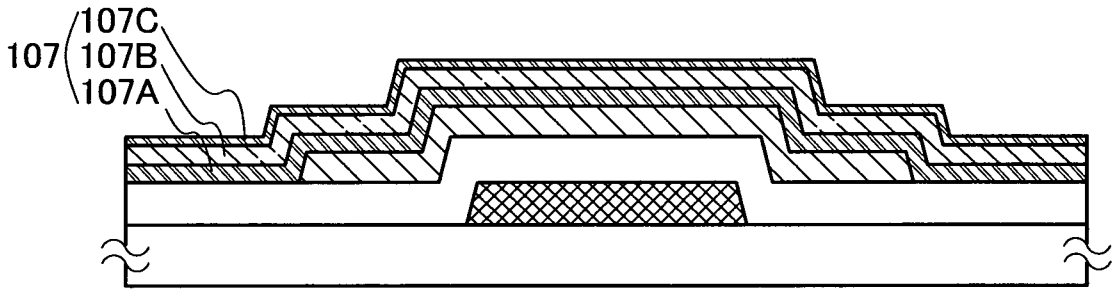


FIG. 1C

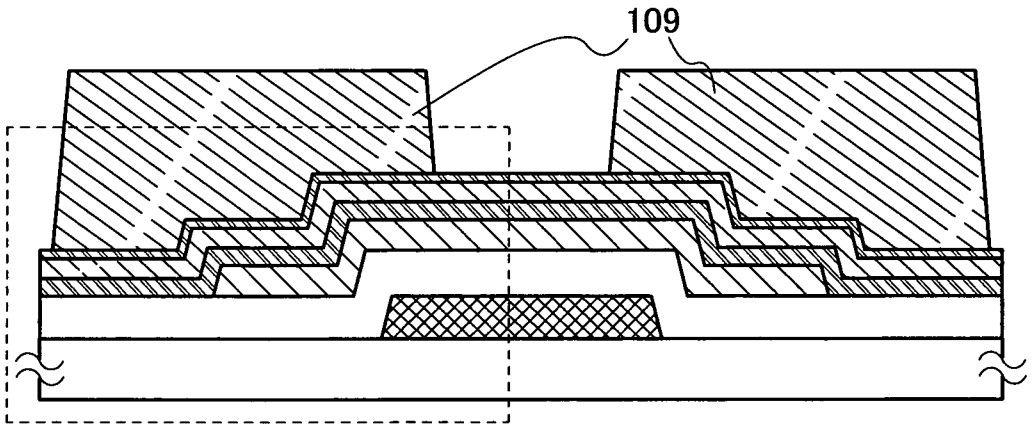


FIG. 2A

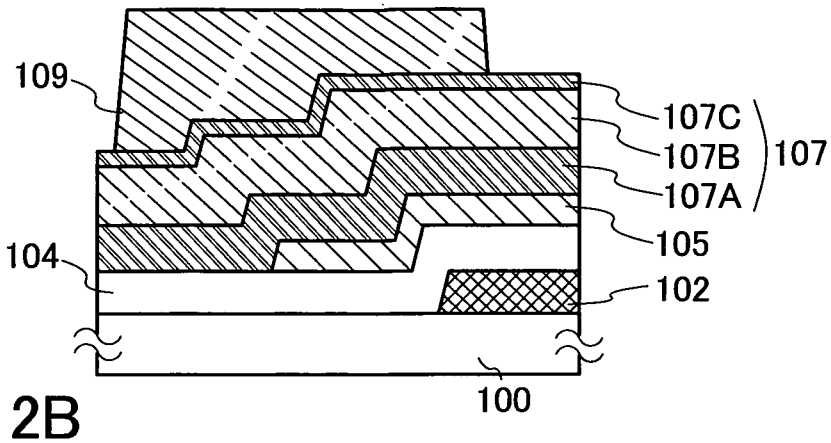


FIG. 2B

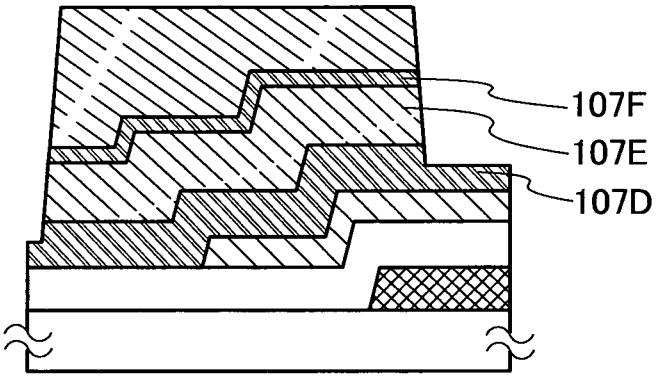


FIG. 2C

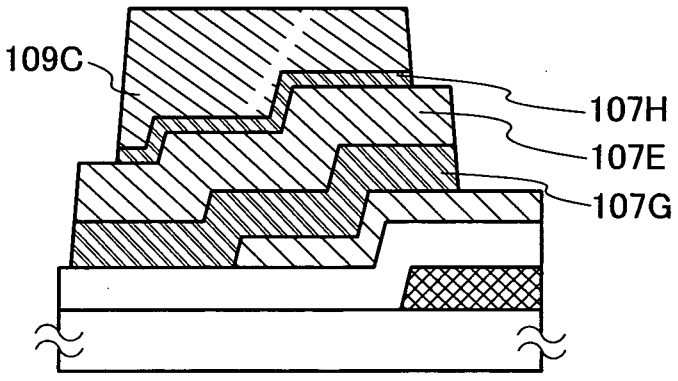


FIG. 2D

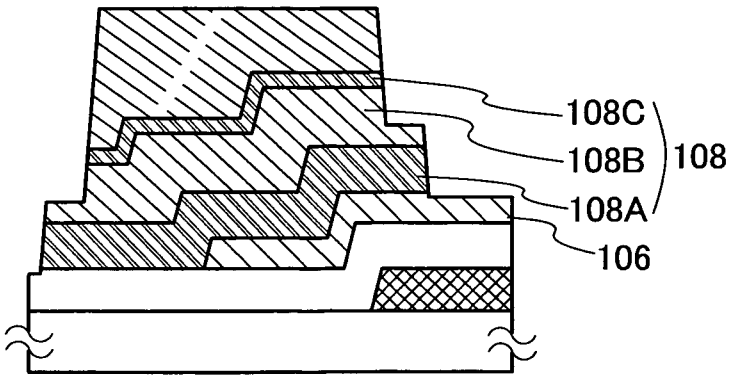


FIG. 3A

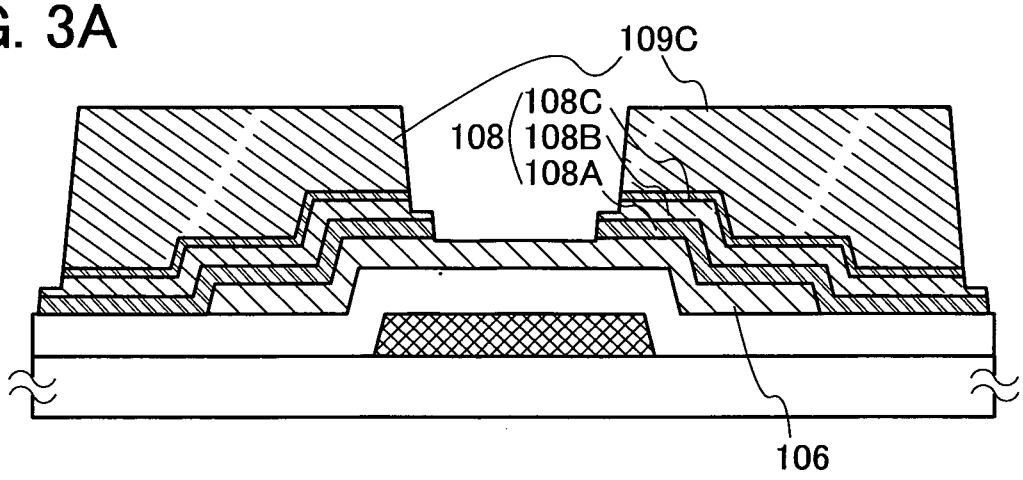


FIG. 3B

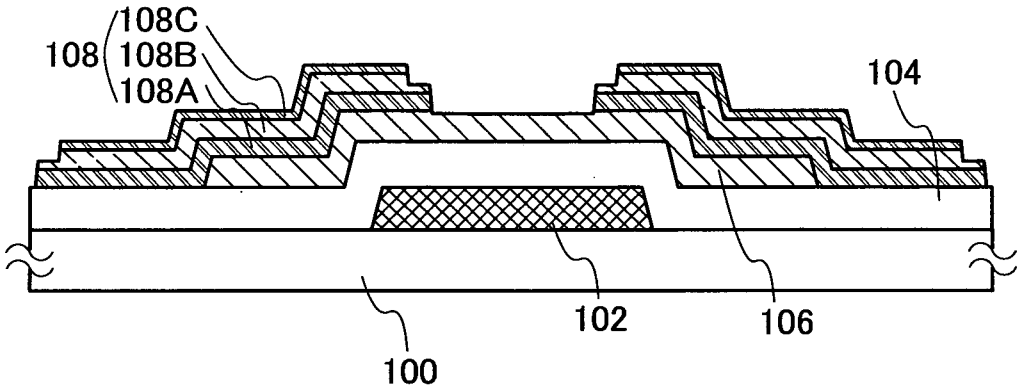


FIG. 3C

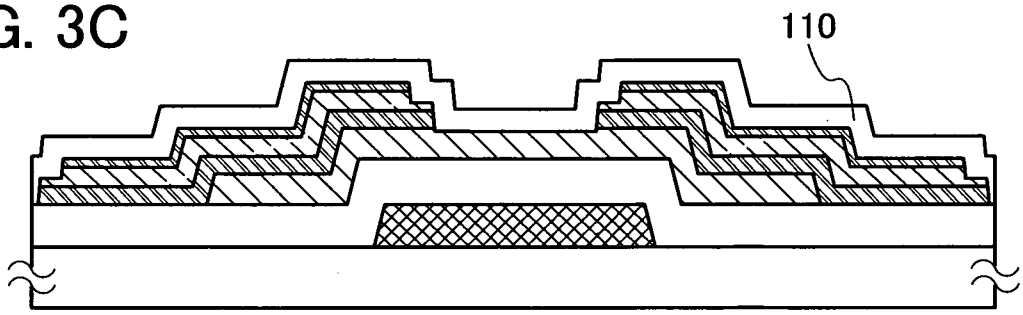


FIG. 3D

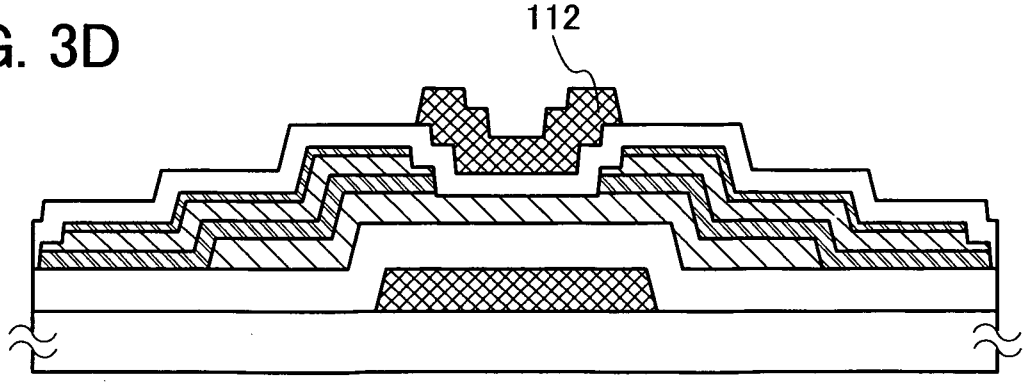


FIG. 4A

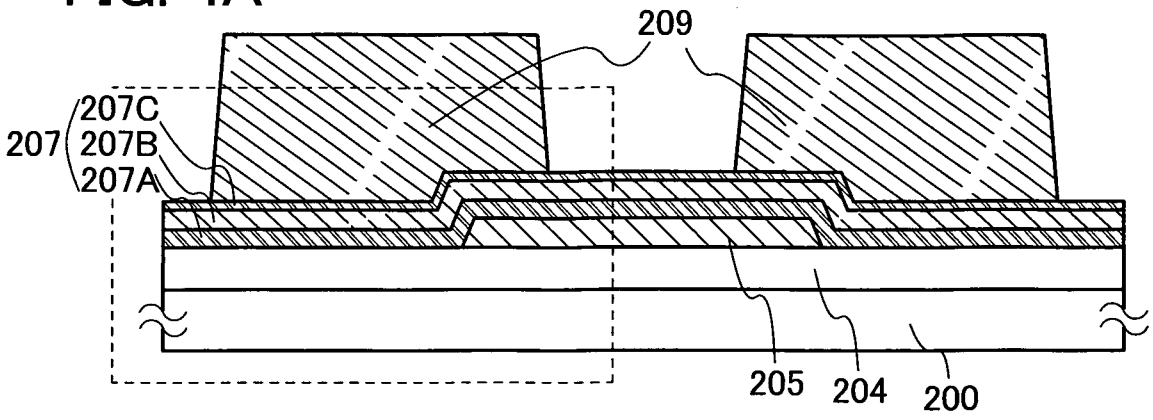


FIG. 4B

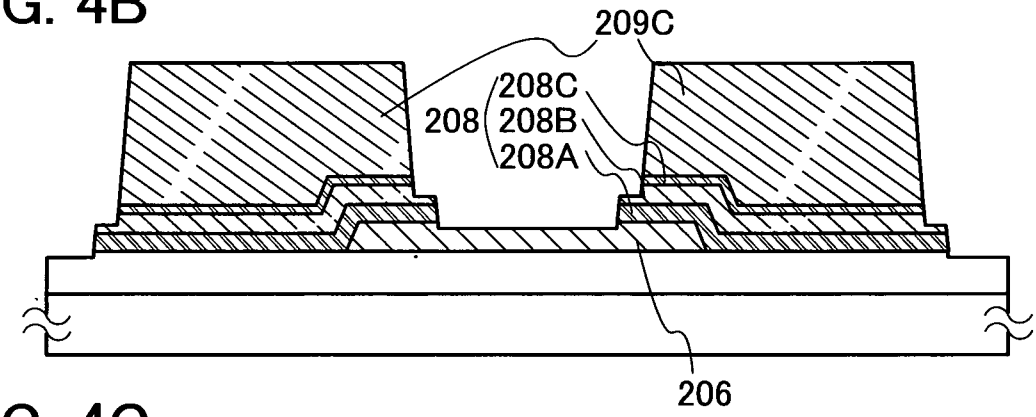


FIG. 4C

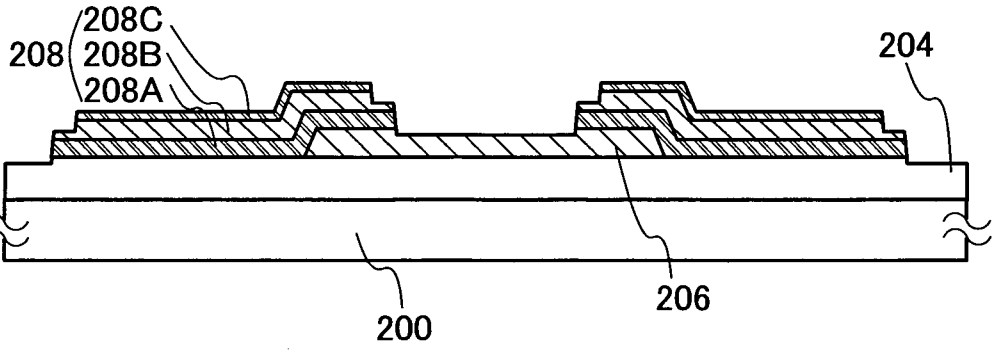


FIG. 4D

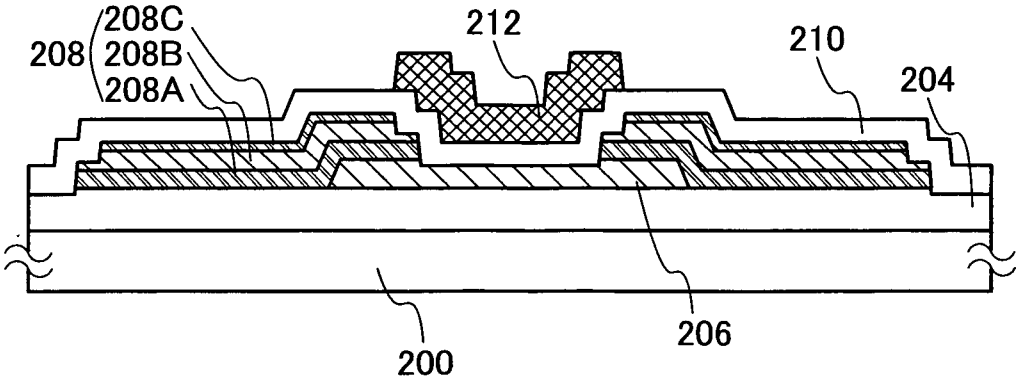


FIG. 5A

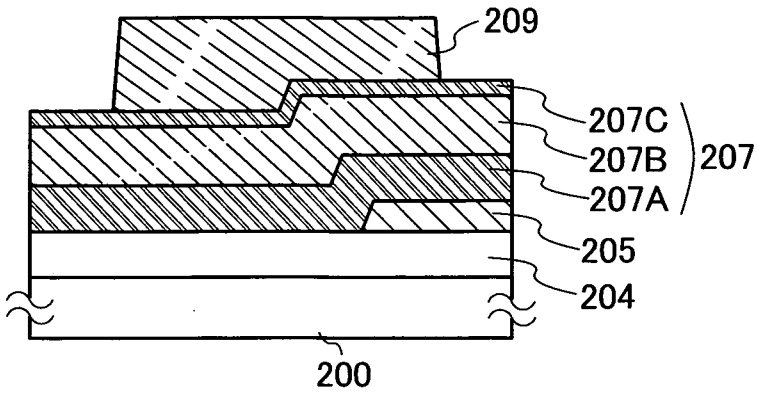


FIG. 5B

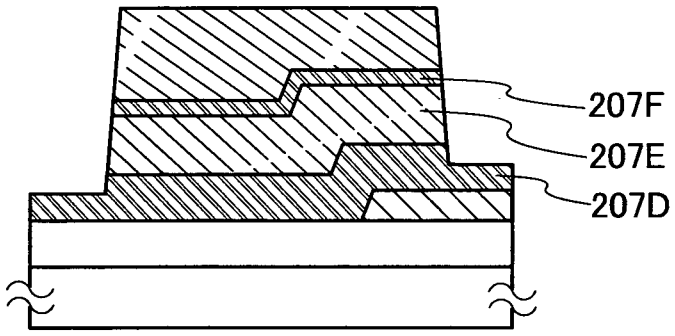


FIG. 5C

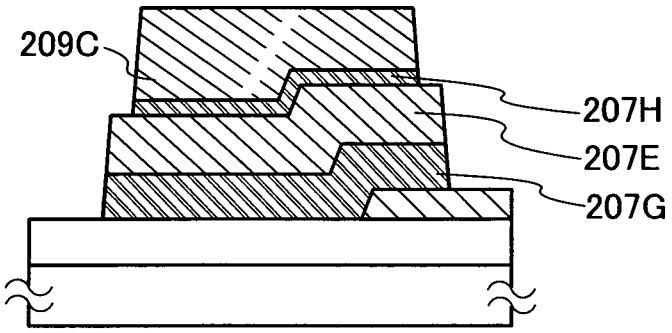


FIG. 5D

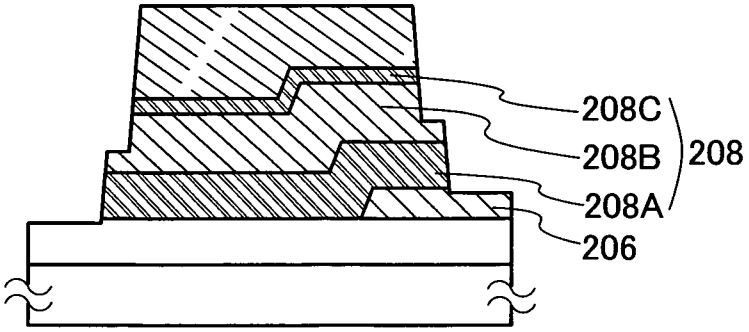


FIG. 6A

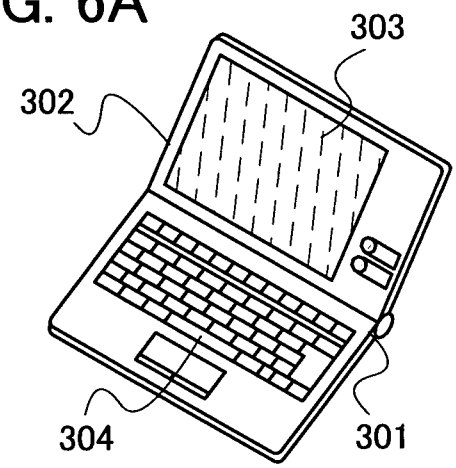


FIG. 6B

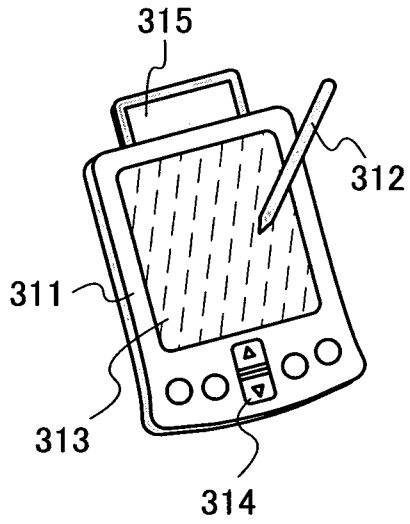


FIG. 6C

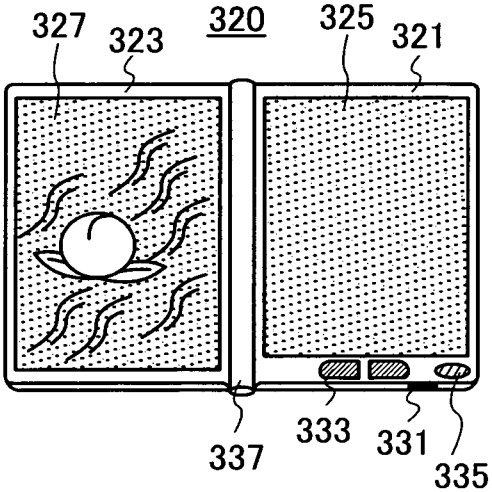


FIG. 6D

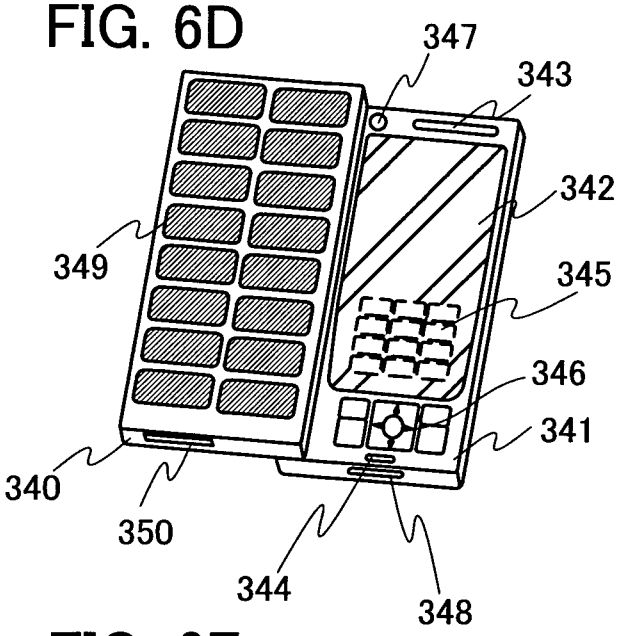


FIG. 6E

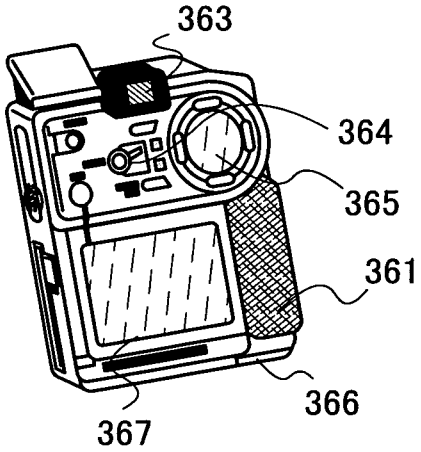


FIG. 6F

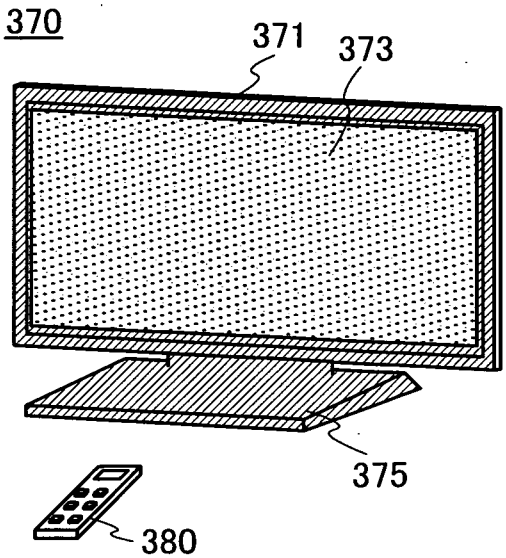


FIG. 7A

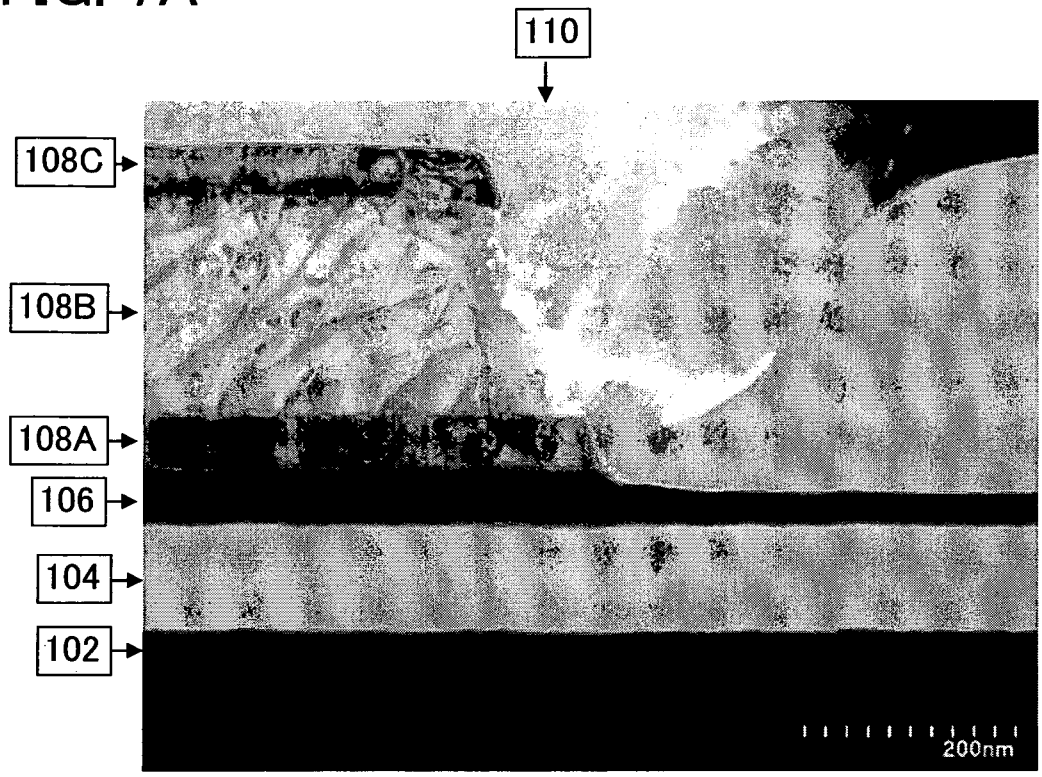
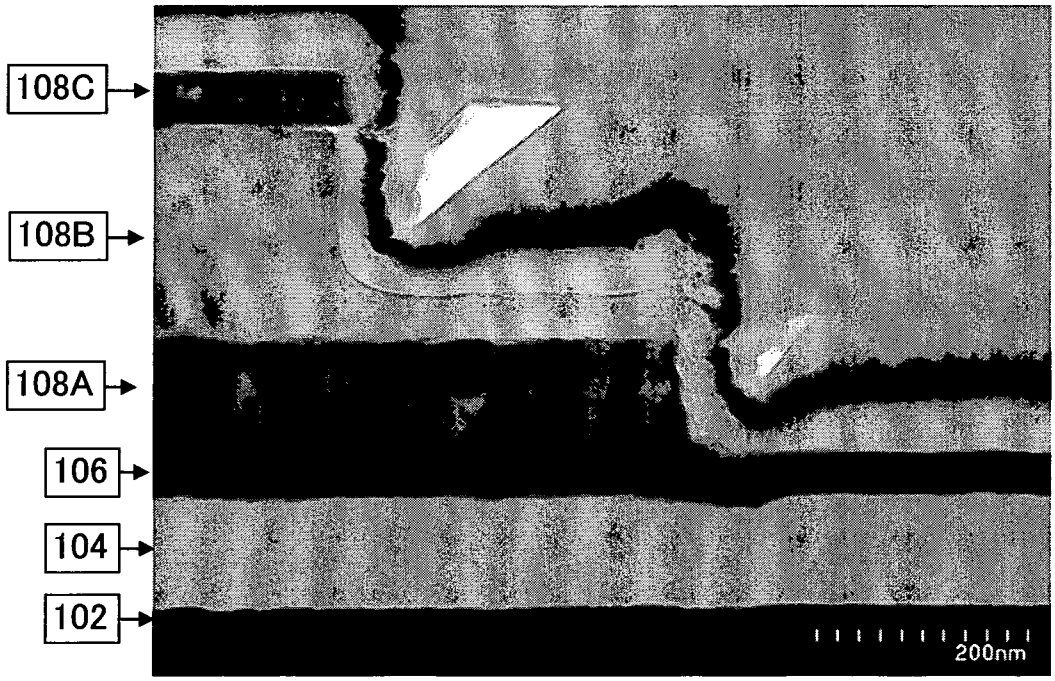

110
108C
108B
108A
106
104
102
200nm

FIG. 7B


108C
108B
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106
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200nm

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/062855

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L21/336, H01L21/28, H01L21/3065, H01L21/3205, H01L23/52, H01L29/417, H01L29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/0099216 A1 (SUZAWA et al.) 2010.04.22, Par. Nos. [0060] to [0142] & JP 2010-123923 A & KR 10-2010-0044716 A & CN 101728275 A	1-33
A	JP 2002-198360 A (TOKYO ELECTRON LIMITED) 2002.07.12, Par. Nos. [0019] to [0041] (No Family)	1-33
A	JP 2002-184760 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 2002.06.28, Par. Nos. [0026] to [0050] (No Family)	1-33

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24.08.2011	06.09.2011

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Takashi WATAHIKI Telephone No. +81-3-3581-1 101 Ext. 3462

4M 2934

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/062855

CLASSIFICATION OF SUBJECT MATTER
H01L21/336 (2006.01)i, H01L21/28 (2006.01)i, H01L21/3065 (2006.01)i,
H01L21/3205 (2006.01)i, H01L23/52 (2006.01)i, H01L29/417 (2006.01)i,
H01L29/786(2006.01)i