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**Philip** [GB/GB]; Midas Green Limited, The Irwin Centre,  
Scotland Road, Dry Drayton, Cambridge CB3 8AR (GB).

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(74) Agents: **DUNLOP, Hugh, C.** et al.; R.G.C. Jenkins & Co.,  
26 Caxton Street, London SW1H 0RJ (GB).

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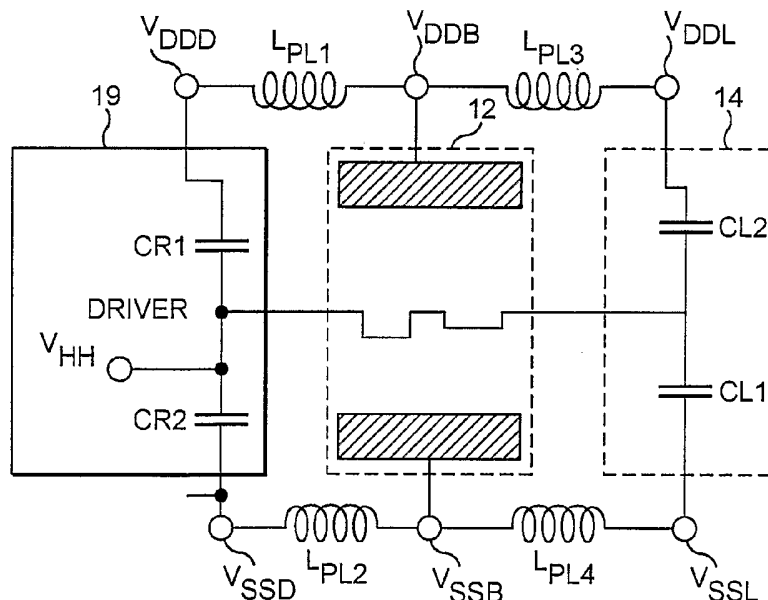
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(71) Applicant (*for all designated States except US*): **MIDAS GREEN LIMITED** [GB/GB]; The Irwin Centre, Scotland Road, Dry Drayton, Cambridge CB3 8AR (GB).

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(54) Title: IMPROVEMENTS TO RESONANT LINE DRIVERS



(57) Abstract: An electronic driver circuit for communicating a logic value along a conductor (12) from one part of a system (10) to another (14) by representing each of two logic values by one of two logic levels ( $V_{DD}$ ,  $V_{SS}$ ). A capacitor ( $C_{R1}$ ) reduces ground and power reference differences between a chip containing the driver and the board on which it is mounted. The capacitor also provides power and ground decoupling. According to another aspect, a controlled slew rate ramp initiates an incident or outbound wave or turn-on and circuits are described for this. The time taken to complete the controlled slew rate ramp can be adjusted. The arrangements allow reduced power consumption, whilst at the same time producing desirable signal characteristics.



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## IMPROVEMENTS TO RESONANT LINE DRIVERS

### Field of the Invention

5           This invention relates to electronic circuits. In particular this invention relates to improving the performance of a type of electronic driver circuit the operation of which is intended to reduce power consumption. This invention relates to achieving low power consumption in such driver circuits, whilst at the same time producing desirable signal characteristics.

### Background to the Invention

10           For many years conventional driver circuits have existed which communicate a logic value from one part of a system to another by representing each of two logic values respectively by one of two voltage levels. For example Fig. 1a shows a conventional CMOS inverting driver 10 formed as part of an IC. Output driver 10 generates an inverted driver output voltage VDO in response to a driver input voltage signal VI. Driver 10 is connected through electrical conductor 12 printed wiring board (PWB) to load circuitry 14. Specifically, electrical conductor 12 converts driver  
20           output voltage VDO into conductor output voltage VBO that drives a group of one or more digital ICs 16 in load 14.

          Driver 10 is formed with N-channel insulated gate field effect transistor ('FET') QA and P-channel insulated gate FET QB whose gate electrodes receive driver input voltage VI. The sources of FET QA and QB respectively are connected  
25           to a source of low supply voltage VSS, typically ground reference (0 volts) and a source high supply voltage VDD. The QA and QB drains are connected together to provide driver output voltage VDO. N-channel FET QA is turned on by raising input voltage VI to suitably high level. On the other hand FET QB is turned on by reducing input voltage VI to a suitably low level.

30           Accordingly, only one of FETs QA and QB is conductive during steady state operation. If input VI is high, FET QA is turned on to pull driver output voltage VDO to a low value close to VSS. Conversely, output voltage VDO is at a high value close to VDD when input voltage VI is low and causes FET QB to be turned on. The "on" resistance of each of FET QA and QB is normally quite low. Consequently

output signal VDO makes a rapid transition from VSS to VDD in response to a rapid transition of input signal VI from high to low. Likewise output signal VDO makes a rapid transition from VDD to VSS in response to a rapid transition of input signal VI from low to high. During a transition there is a typically a brief period when both

5 FETs QA and QB are conductive.

PWB electrical conductor 12, commonly referred to as an interconnect, consists of copper track and a ground plane at the VSS potential. The steps shown in the line passing through conductor 12 in Fig. 1a qualitatively represent the changes in direction that conductor 12 makes on the PWB. The ground plane is represented by  
10 the block slanted shading.

Since Fig. 1b is a simplified electrical model, it does not show the parasitic lead inductances which typically exist when driver 10 is formed as part of an integrated circuit which is contained within an integrated circuit package which is in turn mounted on a PWB. These parasitic inductances must be accounted for in the  
15 design of driver 10 if an undesirable effect known as ground/power bounce is to be avoided.

Interconnect 12 in Fig. 1a or 1b having distributed inductance and capacitance is alternatively known as a transmission line having characteristic impedance  $Z_0$ . As is well known in the art,  $R_{ON}$  in Fig. 1b is ideally chosen to match  $Z_0$  so that a half  
20 amplitude outward bound wave is launched initially which doubles its amplitude on reaching load 14 and reflects back towards driver 10 as a full amplitude wave. In the absence of  $R_{ON}$  or if  $R_{ON}$  is too small, the reflected wave is of an amplitude exceeding the level of VDD and causing signal integrity problems.

In his previous application (PCT/GB96/02199, US6,201,420B1, EP0848868  
25 etc), applicant describes a method by which, rather than generating a half amplitude outward bound wave by effectively by dropping voltage through a resistance  $R_{ON}$ , an equivalent wave can be launched by connecting signal VDO via a low "ON" resistance switch or transistor to an intermediate voltage VHH generated from an additional voltage supply or simply from a reservoir capacitor. The method has the  
30 advantage that less power is dissipated and the power consumption can be reduced by up to 75%. The technique is equally applicable to situations in which load capacitance  $C_L$  is much larger than distributed capacitance  $C_B$  in which case  $C_L$  and  $L_B$  act more like a sinusoidally LC resonant system than a transmission line. For ease

of reference a driver employing the method will be referred to as a resonant line driver.

Figs. 2a and 2b show how the resonant line driver can equivalently replace conventional line driver of Figs 1a and 1b.

5 Fig. 2b for example shows a CMOS implementation of a resonant line driver. Q1 and Q3 can connect the driver output VDO to low and high voltage sources VSS and VDD respectively as in a conventional driver. Particular to the resonant line driver, Q2 can connect driver output VDO also to an intermediate voltage source VHH during transitions. Gate electrodes (and therefore switching of Q1, Q2 & Q3)  
10 are controlled by control circuit 20 via signals VC1, VC2 & VC3 respectively. Since Q1 and Q3 are N channel MOSFET (NMOS) transistors, they provide a conductive path when VC1 and VC3 respective are at a high voltage level. Since Q2 is a P channel MOSFETs (PMOS) transistor it provides a conductive path when VC2 respective is at a low voltage level.

15 Fig. 3 shows that intermediate voltage supply VHH can be supplied by a reservoir capacitor CR.

Fig. 4 shows waveforms representative of the operation of the circuit shown in Fig. 2b when CL is much larger than CB and CL and LB act more like a sinusoidally LC resonant system than a transmission line. Initially only Q1 is "ON" and VDO is at a low level. Then in response to a change of level of the input signal VI at time t1 Q1  
20 is switched "OFF" while Q2 is switched "ON" driving VDO near to the level of VHH. Current builds sinusoidally to a maximum and then falls back to zero whilst at the same time the voltage seen at the load VBO swings sinusoidally to the level of VDD at which point control circuit 20 switches Q2 "OFF" and switches Q3 "ON" to  
25 complete the transition. As shown in Fig. 4, the circuit operates in a similar manner to produce the opposite polarity transition

Fig. 5 shows waveforms resulting from the equivalent sequence of events when CL is smaller than or of a similar value to CB, in which case the transmission line character of CB and LB is more clearly evident. In response to a change of level  
30 of the input signal VI at time t1, Q1 is switched "OFF" while Q2 is switched "ON" driving VDO near to the level of VHH. An outward bound (or incident) wave of voltage amplitude equivalent to VHH travels along the transmission line. When it reaches the load, and since the load is reasonably small and cannot provide a significant path for the current in the incident wave, a reflected wave results tending

to cancel the current of the incident wave. This reflected wave is also of amplitude equivalent to VHH but adds to the incident wave to give a voltage level at the load equal to VDD. The reflected wave travels back toward driver 18 until the whole length of the transmission line is at the level of VDD by time  $t_2$ , being the time when  
5 the reflected wave actually reaches the driver 18, at which point control circuit 20 switches Q2 "OFF" and switches Q3 "ON" to complete the transition. Control circuit 20 can be designed in a variety of ways to control the timing of this to coincide with the return of the reflected wave. The timing for the current transition of VDO can be determined by observing and storing some characteristic of a previous transition to  
10 make adjustments to some circuit capable of storing and reproducing timed sequences, for example a digitally controlled delay line controlled by a digital counter.

Resonant Line Drivers have the potential to both reduce power consumption and produce well conditioned signal without ringing and overshoot. Unfortunately  
15 though, when certain unavoidable characteristics of typical physical implementations are taken into account, whilst low power consumption can be achieved, signal conditioning may be poor.

Fig. 6 shows the circuit of Fig. 3 but modified to make it more representative of a real physical implementation. Quite typically driver 18 is formed on silicon chip  
20 which is in turn contained in a chip package in turn mounted onto PWB 12. Often, though not necessarily, reservoir capacitor CR may be contained within the chip or chip package. Fig. 3 shows driver 18, PWB 12 and load 14 all sharing a common voltage reference level VSS. In an actual physical implementation this is often not the case since as shown in Fig. 6, ground voltage levels for driver 18, PWB 12 and load  
25 14 (VSSD, VSSB and VSSL respectively) and power voltage levels for driver 18, PWB 12 and load 14 (VDDD, VDDB and VDDL respectively) are connected via parasitic package lead inductances LPL1, LPL2, LPL3, and LPL4 as shown. Also, in an actual physical implementation, the parasitic capacitances of the interconnect and load often occur not only between signal VSS but also between signal VDD as shown.

30 Turning to Fig. 7, Q2 of driver 18 in Fig. 2b is typically relatively large and consequently has a very low "ON" compared to, for example, QA or QB in the conventional driver of Fig. 1a, so the waveform produced by driver 18 as shown in Fig. 7 is very abrupt, causing VDO to go from the level of VSS to nearly the level of VHH in a relatively short space of time at about time  $t_1$ . At the same time the current

flowing from driver 18 into the interconnect increases very rapidly giving a very high rate of change of current (or  $di/dt$ ). Since the change in current causes an equal and opposite change in current in the return path via LPL1 & LPL2, these parasitic inductances respond to such a rapid change in current by allowing an appreciable voltage difference to occur between VSSD & VSSB and between VDDD & VDDB as shown in Fig. 7 which shows the levels of VSSB and VDDB referred to VSSD and VDDD as reference.

In an actual application driver 18 would normally be part of an IC not only driving output signals but also receiving input signals. Unfortunately, since the input signals have considerable capacitance coupling with VSSB and VDDB, their levels tend to be determined in reference to VSSB and VDDB so that for example an input signal which is nominally at a low level will present to its receiver on the aforementioned IC, a voltage spike very similar to that shown for VSSB in Fig. 7 at time  $t_1$ . This causes the possibility of the input signal being temporarily interpreted as being at a high level. As can be seen in Fig. 7, since all the change in output current from driver 18 in Fig. 6 is supplied from VSSD either via reservoir capacitor CR & Q2 in Fig. 2b or through Q1 in Fig. 2b, the most extreme disturbance is to the level of VSSB in relation to VSSD at time  $t_1$ ,  $t_3$  &  $t_4$ . (At time  $t_2$  the change in current is supplied in part by VDDD via Q3 in Fig. 2b so the disturbance is less serious.) Therefore a signal which inputs to the aforementioned IC and because of its particular physical routing being coupled mainly to VSSB may suffer serious disturbance as received by a receiver circuit in the IC.

### Summary of the Invention

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It is the aim of the present invention to provide improvements to resonant line drivers to allow their operation with low signal disturbance and better signal integrity whilst still allowing the benefits of reduced power consumption. These improvements may be used either in combination or individually to provide a greater or less degree of benefit.

30

In accordance with a first aspect of the invention, an electronic driver circuit is provided for generating a circuit output signal providable to an electrical conductor that furnishes a conductor output signal providable to a load where the circuit and conductor output signals respectively making corresponding circuit and conductor

output transitions approximately between a pair of output voltage levels between which there is an intermediate voltage level. Inductance and capacitance of the conductor and the load produce resonance that enables the conductor output signal to largely complete each conductor output transition while the circuit output signal is  
5 being held at approximately the intermediate voltage level for a non-zero intermediate-level holding period during the corresponding circuit output transition. The circuit includes at least a first capacitor element between the intermediate voltage level and each of the first and second voltage levels and at least a second capacitor element (preferably equal to the first capacitor element, e.g. a ) between the  
10 intermediate voltage level and the second voltage level.

The first and second capacitor elements may form a split-reservoir capacitor.

A package lead inductance may exist between the electrical conductor and a source of each of the pair of output voltage levels. In this case the first and second capacitor elements are preferably such that a change in circuit output voltage causes  
15 return current flowing back into the driver to be split approximately equally between the package lead inductances. The first and second capacitor elements may provide decoupling capacitance between the output voltage levels.

In accordance with a second aspect of the invention, an electronic driver circuit is provided for generating a circuit output signal providable to an electrical  
20 conductor that furnishes a conductor output signal providable to a load. The circuit and conductor output signals respectively make corresponding circuit and conductor output transitions approximately between a pair of output voltage levels between which there is an intermediate voltage level. Inductance and capacitance of the conductor and the load produce resonance that enables the conductor output signal to  
25 largely complete each conductor output transition while the circuit output signal is being held at approximately the intermediate voltage level for a non-zero intermediate-level holding period during the corresponding circuit output transition. The circuit comprising a ramp control circuit for controlling partial circuit output transitions between at least one of the pair of output voltage levels and the  
30 intermediate level to provide a substantially non-zero transition time for a partial circuit output transition.

The partial circuit output transition is preferably controlled to be slow relative to other switching events in the circuit.

A pull-up transistor and a pull-down transistor may be provided for pulling the circuit output up to a first of the two output voltage levels and down to a second of the two output voltage levels, in which case the partial circuit output transition is controlled to be slower than the switching of the pull-up and pull-down transistors.

5        An intermediate level driving transistor can be provided, which, in switching-on drives the circuit output up to the intermediate voltage level and in switching-off permits the circuit output to be driven up to a first of the two output voltage levels. In this case the partial circuit output transition is controlled to be slower than the switching-off of the intermediate level driving transistor.

10        The partial circuit output transition time is preferably adjustable, for example it is controllable as a function of the time taken for the conductor output signal to largely complete a conductor output transition.

      The control circuitry may comprise time-comparison circuitry for comparing the circuit output signal and the second control signal to determine whether the circuit  
15        output signal completes a circuit output transition before the second control signal completes the corresponding control transition and adjustment circuitry for adjusting the partial circuit transition time depending on the comparison.

      Alternatively the comparator circuit preferably compares a level of the partial circuit output transition with a reference voltage that is approximately midway  
20        between the intermediate voltage level and an output voltage level to which the output is transitioning at a time approximately midway between a start of the partial circuit output transition and an expected completion of the partial circuit output transition.

      Preferably, reference ramp circuitry may be provided for generating a reference ramp, together with comparator circuitry coupled to the reference ramp  
25        circuitry for comparing a partial circuit output transition with the reference ramp.

      The time taken for a partial circuit transition is preferably controlled as a function of characteristics (e.g. characteristics determined from relative timing of two signals) of at least one previous circuit output transition.

      Preferably the ramp control circuit controls a partial circuit output transition as  
30        a function of a current stored control value stored as a result of a previous partial circuit output transition.

      In accordance with a third aspect of the invention, an electronic driver circuit is provided for generating a circuit output signal providable to an electrical conductor that furnishes a conductor output signal providable to a load. The circuit and

conductor output signals respectively make corresponding circuit and conductor output transitions approximately between a first voltage, a second voltage and an intermediate voltage between the first and second voltages. In this aspect, the circuit comprises: a first transistor having (a) a first flow electrode coupled to a source of the first voltage, (b) a second flow electrode coupled to an output node from which a circuit output signal is provided, and (c) a control electrode responsive to a first control signal for controlling current flow between the first transistor's flow electrodes; a second transistor having (a) a first flow electrode coupled to a source of the second voltage, (b) a second flow electrode coupled to the output node, and (c) a control electrode responsive to a second control signal for controlling current flow between the second transistor's flow electrodes; and a third transistor having (a) a first flow electrode coupled to a source of the intermediate voltage, (b) a second flow electrode coupled to the output node, and (c) a control electrode responsive to a third control signal for controlling current flow between the third transistor's flow electrodes. Fourth and fifth transistors are connected between the control electrode of the third transistor and the sources of the first and second voltage levels respectively. Control circuitry selectively discharges the control electrode of the third transistor to the first and second voltage levels respectively through the fourth and fifth transistors such that the control electrode makes partial transitions between the first and second voltage levels. The output signal makes rising and falling circuit output transitions approximately between the first and second voltages controlled by the first, second and third control signals, and the circuit output signal stays approximately at the intermediate voltage for a non-zero intermediate-level holding period during each circuit output transition.

The features of the first, second and third aspects of the invention and their various preferred features may be combined in any combination.

In accordance with the first aspect of the invention, the split reservoir (or other) capacitor reduces ground and power reference differences (known as ground and power bounce) between a chip containing a resonant driver and the PWB on which it is mounted. The split reservoir capacitor also provides power and ground decoupling. In its second aspect the invention provides for a controlled slew rate ramp initiating an incident or outbound wave or turn-on and circuit methods for this. In a further aspect, the invention provides for the time taken to complete the

controlled slew rate ramp to be adjusted approximately proportionately in time with the intermediate voltage holding period of the resonant driver.

The controlled slew rate ramp methods can not only further reduce ground and power bounce but also reduce unnecessary high frequency components in the signal seen at the load which can cause other signal integrity and radio frequency interference issues. A further aspect of the current invention lies in matching the “ON” resistance of the driver pull-up and pull-down transistors ( for example Q3 and Q1 in Fig. 2b) approximately to the characteristic impedance interconnect 12. A still further aspect of the invention relates to means for determining a feedback control signal to adjust the internal delay of a resonant line driver.

A number of preferred embodiments will now be described by way of example only, with reference to the drawings.

#### Brief Description of the Drawings

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Figs. 1 to 3 represent prior art resonant line driver circuits.

Figs. 4 and 5 are timing diagrams illustrating the operation of the circuit of Fig. 2b for different values of CL.

Fig. 6 represents a resonant line driver similar to that of Fig. 3 in a typical physical environment.

Fig. 7 is a timing diagram for the circuit of Fig. 6.

Fig. 8 represents a resonant line driver in accordance with a first embodiment of the invention.

Figs. 9 to 11 are timing diagrams illustrating the operation of the circuit of Fig. 8.

Fig. 12 represents a resonant line driver in accordance with a second embodiment of the invention.

Fig. 13 is a timing diagram illustrating the operation of the circuit of Fig. 12.

Fig. 14 represents a resonant line driver in accordance with a third embodiment of the invention.

Figs. 15 and 16 are timing diagrams illustrating the operation of the circuit of Fig. 14.

Fig. 17 is a diagram of a control circuit suitable for use in the circuit of Fig. 12 or Fig. 14 or other embodiments.

Fig. 18 illustrates a prior art control circuit.

Fig. 19 is a timing diagram for explanation of the operation of a resonant line driver in accordance with the second aspect of the invention.

Fig. 20 illustrates a control circuit suitable for use in accordance with the  
5 second aspect of the invention.

Fig. 21 expands upon Fig. 19.

Fig. 22 illustrates a control circuit alternative to that of Fig. 20.

Fig. 23 represents a resonant line driver in accordance with a further  
embodiment.

10 Fig. 24 is a timing diagram for the circuit of Fig. 23.

Fig. 25 illustrates in greater detail a comparator suitable for use in the circuit  
shown in Fig. 23.

#### Detailed Description of the Preferred Embodiments

15

Turning to Fig. 8, it shows a circuit similar to that in Fig. 6 but instead of the reservoir capacitance being supplied entirely between the VSSD and VHHD circuit nodes, the reservoir capacitor is split into two capacitances CR1 and CR2. CR1 provides capacitance between VSSD and VHHD while CR2 provides capacitance  
20 between VDDD and VHHD. Since each of CR1 and CR2 provides reservoir capacitance in parallel, each of CR1 & CR2 can be made half the numerical size of CR in Fig. 6 to provide the same effective reservoir capacitance. But by using a split reservoir capacitor driver 19 in Fig. 8 is made more symmetrical so when a change in voltage of driver output signal VDO causes current to flow into or out of interconnect  
25 12, a return current flows back into driver 19 split equally between package lead inductances LPL1 & LPL2.

Fig. 9 shows waveforms that occur in relation to the circuit of Fig 8. Comparing Fig. 7 with Fig. 9, whereas at time t1 in Fig. 7 since in Fig. 6 all return current flows through LPL2 giving a large offset between VSSB and VSSD, at time t1  
30 in Fig. 9 both VSSB and VDDDB are offset approximately equally from VSSD and VDDD respectively but by a smaller amount since in the circuit of Fig. 8 any return current is split equally between package lead inductances LPL1 and LPL2. As a further benefit, the series combination of LPL1 and LPL2 provides a very useful degree of decoupling capacitance between VSSD and VDDD. For example, at time t2 in Fig. 9

some current is supplied from node VDDD to the driver output node via, for example MOSFET Q3 in Fig. 2b. The decoupling capacitance provided by the series combination of CR1 and CR2 can provide the necessary current which would otherwise need to be drawn externally through LPL1 causing further ground bounce.

5 Turning to Fig. 10, a second element of the current invention provides for a controlled slew rate ramp when at time t1, driver output signal is driven from the level of VSSD to VHHD. The positive going ramp takes output signal VDO smoothly at a controlled rate from the level of VSSD at time t1 nearly to the level of VHHD at time t1a and a negative going ramp takes output signal VDO smoothly at a controlled rate  
10 from the level of VDDD at time t3 nearly to the level of VHHD at time t3a.

Preferably the ramp is generated by a circuit of low output impedance so that the amplitude and duration of the ramp is largely unaffected by the degree of loading on output signal VDO. A controlled ramp considerably reduces the rate of change of current output from the driver and therefore the rate of change of return current  
15 through for example LPL1 and LPL2 and results in considerable reduction of power and ground bounce, as shown in Fig. 10 and yet adds only a small delay to the overall transit of the signal from source to load.

When the load approximates a transmission line the ramp commencing at time t1 in Fig.10 travels along the transmission line and reflects back toward the driver  
20 reaching it at time t2. At this point control circuit 20 disconnects output VDO from VHHD and connects it to VDDD via pull-up transistor for example Q3 in Fig. 2b. If Q3 is sized such that its "ON" resistance is matched to the characteristic impedance of the transmission line then the driver output voltage VDO smoothly approaches the level of VDDD without overshoot or undershoot to complete the transition. A similar  
25 sequence commences at time t3 in the opposite polarity transition and likewise Q1 in Fig.2b can be sized such that its "ON" resistance is matched to the characteristic impedance of the transmission line.

A disadvantage of the controlled ramp method is that a reduced portion of total charge for the transition is supplied from the reservoir capacitor. For example in Fig.  
30 10 the shade areas under the IHH and IDD curves show the relative proportions of charge deliver from the VHHD node (i.e. reservoir capacitor) and VDDD power supply node. As can be seen in Fig. 10, about 75% of the charge is provided by the reservoir capacitor, the remaining 25% coming from the VDDD power supply. Also indicated in Fig. 10 (dotted lines) is that if the controlled ramp rate is made still

slower the portion of charge supplied from the reservoir capacitor could drop still further to about 50%. Therefore the use of a controlled ramp leads to a slightly higher power consumption, though still much lower than a conventional driver but improves signal integrity and ground/power bounce. The timing requirements for signal integrity versus those for low power consumption and speed are therefore somewhat in opposition. Achieving a compromise between the requirements is the aim of a further element of the current invention.

Looking again Fig. 10, if the ramp rate were approximately halved such that its duration is from  $t_1$  to  $t_2$  then as discussed above, the power consumption would increase so that a driver employing such a ramp rate might be unsuitable. On the other hand, if the same driver were driving an interconnect of about twice the length (and therefore delay), such a ramp time would again have low power consumption compared with a conventional driver as well as delivering good signal integrity as show in Fig. 11, whilst a ramp of the original speed ( $t_1$  to  $t_{1a}$ ) would bring only marginal further improvement in power consumption and speed and yet greatly increase the contribution of the driver to ground/power bounce. At the same time the signal would contain an excess of high frequency harmonics adding unnecessarily to radio frequency emission. If therefore the ramp circuit is made controllable (i.e. capable of delivering ramp times of variable duration within a range, and if the ramp time is controlled by the same circuit control mechanism used in control circuit 20 to adjust the intermediate level holding period of the resonant line driver, then the driver can operate over a range of load conditions (i.e. can drive load with varying transmission line delay or LC resonant frequency) and still produce waveforms which represent close to an optimum chosen compromise between, on the one hand power consumption and speed and on the other hand signal integrity.

Fig. 12 shows a resonant line driver 118 comprising a first embodiment of a ramp control circuit 118. Comparing it with the circuit in Fig. 2b, NMOS transistor Q2 has been replaced by a pair of transistors Q2N (an NMOS device) and Q2P (a PMOS device) with their respective channels connected in parallel. At the beginning of a transition of output signal VDO the gate of Q2N is charged (positively) by a flow of current from current mirror Q21/Q20 when Q22 switches "ON", and at the same Q24 is turned "OFF" whilst the gate of Q2P is charge (negatively) by a flow of current from current mirror Q31/Q30 when Q32 switches "ON" and at the same Q34 is turned "OFF".

In a LOW to HIGH transition, for example that commencing at time  $t_1$  in Fig. 13, PMOS transistor Q2P is initially not conducting even after its gate electrode begins to fall because its channel cannot switch "ON" until the gate electrode become more negative than VHH. NMOS device Q2N on the other hand becomes conductive as soon as its gate electrode becomes more positive than VDO by at least the threshold voltage of Q2N. It will be seen that Q2N is therefore initially in a source follower configuration. During the ramp time signal, VDO is pulled gradually higher by a very low impedance, since a source follower configuration gives a very low output resistance. Q2P does eventually switch "ON" after the ramp is substantially complete and helps to attain a low overall "ON" resistance for Q2N and Q2P in parallel combination. At time  $t_2$  both Q2N and Q2P are rapidly switched "OFF", while pull-up transistor Q3 is switched "ON". In a HIGH to LOW transition, beginning at time  $t_3$ , it is Q2P which switches "ON" first in source follower mode and Q2N which switches "ON" later so that the same pattern of operation occurs as described in relation the LOW to HIGH transition. Varying the value of current reference IREF allows variable ramp rates to be generated.

A disadvantage of the circuit of Fig. 12 is that, since CMOS P-channel devices are generally much less space efficient than N-channel devices, the circuit represents an increase in silicon area for the same value of "ON" resistance when compared to the circuit in Fig. 2b. Fig. 14 shows a resonant line driver comprising an alternative ramp control circuit 119 using a single NMOS device Q2 in place of the parallel combination of Q2N and Q2P in Fig. 12. Clearly for LOW-HIGH transitions Q2 can again be driven in a source follower mode to generate a variable ramp. In Fig. 14, the gate of Q2 is again charged during LOW-HIGH ramp when Q22 switches "ON" current mirror Q21/Q20 and at the same Q24 is turned "OFF". The reference current for mirror Q21/Q20 comes in turn from current mirror Q30/Q31, which is in turn controlled by current reference IREFOUT. For HIGH-LOW transitions, Q2 cannot be used as a source follower but is effectively configured as a common source switch which would normally switch "ON" very abruptly when the gate became more positive than VHH by an amount equal to the threshold voltage of Q2. However if a feedback capacitor CFB is place between output signal VDO and the input to mirror Q41/Q40, then the ramp rate generates a rate dependent current feedback which subtracts from reference current IREFOUT. Thus the circuit uses negative feedback to control the ramp rate to depend on the reference current input, since if the ramp is

too slow the gate voltage will build at the input to mirror Q41/Q40 tending to correct the rate to that desired. In effect therefore the ramp again has a low output impedance. As shown in Fig. 15, for HIGH-LOW transitions the gate of Q2 is charged on a steadily increasing ramp whilst for HIGH-LOW transitions the gate voltage rises quite quickly at first and then slowly during an active period whilst the ramp rate is controlled. Thus capacitor CFB can be described as checking the rate of rise of the current to the control electrode of transistor Q2 when the circuit output signal falls from VDD to VSS.

A drawback with the circuit of Fig. 14 is that on HIGH-LOW transitions there is an appreciable delay from beginning to charge the gate of Q2 to the point where Q2 first becomes conductive until driver output VDO begins to move. As shown in Fig. 16, however, during the period when VDO is high, it is not necessary to discharge the gate of Q2 to the level of VSSD in order to switch Q2 "OFF". If the gate is discharged only to VHHD as shown in Fig. 16, Q2 will still be switched "OFF" but can be switched "ON" again much more quickly at the start of the next HIGH-LOW transition. This can be achieved by replacing Q24 in Fig. 14 with two transistors, one discharging the gate of Q2 to VSSD and the other discharging the gate of Q2 to VHHD under control of suitably provisioned control signals VD2S and VD2H shown in Fig. 16. Alternatively the gate of Q2 can be first discharged to VSSD and then pre-charged to the level of VHHD only before HIGH-LOW transitions.

An advantage of such a modified form of the circuit of Fig. 14 can be seen by comparing Fig. 16 for such a modified circuit with Fig. 15 for the circuit as shown. The peak voltage stress between the gate and channel of switch Q2 is approximately halved. E.g., after a low/high transition, all that is required to switch Q2 off is to return the gate electrode to VHH. This reduces power consumption and allows a thinner oxide layer to be used in the manufacture of the MOSFET channel of Q2. Note that this advantage is independent of the particular rise time control scheme or timing of control for the partial output transitions. Note also that it is described in the context of a circuit comprising exclusively N-channel technology, but is equally applicable to P-channel technology or a mixture of N and P-channels. By way of example, the same principal could be applied to the circuit of Fig. 12, with suitable modifications.

Fig. 17 shows a block diagram of a control circuit 120 in which the same current reference controls both the intermediate level holding period of a resonant line

driver via controllable delay D1 and provides current IREFOUT to a ramp circuit (for example in driver 119 of Fig. 14) so that the ramp period tracks the intermediate level holding period for chosen optimum over a range of timing conditions. As described above, IREFOUT can be adjusted according to some characteristic of a previous

5 transition as described in the prior art.

For example, Fig. 18 shows a control circuit described in US patent No. 6,201,420, in which the duration of the intermediate level holding period is set by the value of an up/down counter 32, in turn controlled by a comparator circuit 30 which compares the timing of circuit output signal VDO with control signal VC2 to produce  
10 feedback signal RP. However, comparator 30 is designed to compare the relative timing of two fast transitioning signals and may be unreliable or inaccurate for use in a resonant line driver using a controlled ramp as described previously. A further aspect of the current invention therefore provides a means of adjusting the intermediate level holding for resonant line drivers using a controlled ramp.

15 Fig. 19, for clarity, shows only the low-to-high transition of a resonant line driver using a controlled ramp. It shows an initial ramp beginning at time t1 followed by an intermediate level holding period after which the reflection of the initial ramp at time t1 (let it be called "initial reflection") arrives at approximately time t3. Time t3 is the time of the transitioning of control signals VC3 and VE2N as determined by the control circuitry. An element of the current invention is the positioning of an optimum timing for the transitioning of control signals VC3 and VE2N at t3 such that it coincides as nearly as possible with initial reflection. When this optimum timing is achieved, output signal VDO rises with approximately the same slope starting from  
20 time t3 as it does during the initial ramp starting at time t1. This optimum timing is depicted by voltage waveform VDOO in Fig. 19. When initial reflection arrives in early, in advance of time t3, signal VDO rises more quickly than the initial ramp beginning at time t1 as indicated by waveform VDOE. Conversely, when initial reflection arrives late in relation to time t3, signal VDO rises with a slope similar to the initial ramp at time t1 but commencing some time after time t3 as depicted by  
25 waveform VDOL.

30

Turning to Fig. 20, this shows control circuit 128 comprising timing circuit and control loop for use in a resonant line driver using a controlled ramp, whilst Fig. 21 depicts waveforms which occur in relation to the operation of control circuit 128.

Control circuit 128 contains latching comparator circuit 132 which has level sensitive inputs receiving signals VDO and VREF and furnishes digital output signal U/D to an N-bit up/down counter 130 in response to clock signal input VIDD. Signal U/D is set to a logic "high" on the rising edge of VIDD if at that time signal VDO has a higher voltage than signal VREF or to a logic "low" on the rising edge of VIDD if at that time signal VDO has a lower voltage than signal VREF. Signal U/D controls the N-bit up/down counter 130 such that if signal U/D is at a logic "high" during the logic "high" to logic "low" transition of input signal VI then the counter value increments. Conversely if signal U/D is at a logic "low" during the logic "high" to logic "low" transition of input signal VI then the counter value decrements. Counter 130 in turn controls digitally controlled delay circuit 134 such that input signal VI is delayed in time by an amount dependent upon the current value stored by counter 130.

Signal VID, the delayed version of signal VI, is output from delay circuit 134 and in turn initiates the transitioning of output signals VE2N, VC3 and VC1 at time t3 in Fig. 21. Current controlled delay circuit 136 further delays signal VID to produce signal VIDD which transitions at time t4 in Fig. 21. Signal VIDD in turn is the clocking signal for latching comparator 132. Delay circuit 136 is controlled by an output of current source 126 which supplies current IREF such that the greater the value of IREF the shorter the delay produced by delay circuit 136. Current source 126 furnishes a second equal or proportional current to output IREFOUT which in turn can control the rise time of the ramp beginning at time t1 in Fig. 21. When optimum timing is achieved, output signal VDO rises with approximately the same slope starting from time t3 as it does during the initial ramp starting at time t1, as depicted by waveform VDDO.

Delay circuit 136 is arranged to produce a delay always equal to approximately one half of the duration of the ramp commencing at time t1 in Fig. 21. Input signal VREF on the other hand has a potential approximately midway between the potential of VHHD and VDDD as shown in the figure. When optimum timing is achieved, waveform VDOO results such that its potential approximately equals VREF at time t4 producing an indeterminate output U/D from latching comparator 132.

On the other hand, if optimum timing has not been achieved, either waveform VDOE or waveform VDOL will result, and latching comparator 132 will drive its output signal, U/D to a logic "high" or logic "low" respectively. Since signal U/D controls the timing of signal VID and hence the positions of time t3 in Fig. 21 via

counter 130 and delay circuit 134 in Fig. 20, the overall operation of the circuit is such that output signals VE2N, VC3 and VC1 are controlled to occur at or near an optimum time. Those skilled in the art will recognize that latching comparator 132, up/down counter 130 and digitally controlled delay 134 together comprise elements of a control loop or more specifically a delay locked loop when used as the control circuit in a resonant line driver.

Turning to Fig. 22, it shows control circuit 138. which is similar to control circuit 128 in Fig. 20 but differs in that digitally controlled delay 134 in of control circuit 128 is replaced by current controlled delay 135 in control circuit 138. Furthermore delay 135 is controlled by a current supplied from digitally controlled current source 140 in place of fixed current source 126 in control circuit 128. Digitally controlled current source 140 supplies several equal or proportional output currents whose magnitudes are controlled as some function of the n-bit binary control input supplied by up/down counter 130 in control circuit 138, but typically the output currents of current source 140 are substantially proportional or inversely proportional to the binary value control input supplied by counter 130. Since counter 130 in control circuit 138 controls current source 140 which in turn controls delay 135 and via current controlled delay 136 enables latching comparator 132, these again comprise elements of a delay locked loop.

An advantage of control circuit 138 when compared with control circuit 128 is that control circuit 138 can supply additional control currents IREFOUT and IREFOUT1 which are proportional to the control input current to current controlled delay 135. As described in relation to control circuit 120 in Fig. 17, IREFOUT in Fig. 22 can be used to control the rise time of a ramp circuit allowing the ramp period to track the intermediate level holding period in a resonant line driver. The further usefulness of IREFOUT1 is described later. As described in relation to control circuit 128 in Fig. 20, control circuit 138 likewise contains current controlled delay 136, the purpose of which is to provide clock signal VIDD to latching comparator circuit 132 such that signal VDO is compared at time t3 to reference voltage VREF as shown in Fig. 21. Voltage VREF and time t3 typically have their intersection as shown in Fig. 21 coinciding with waveform VDOO so that waveform VDOE can be discriminated from waveform VDOL to produce loop feedback signal U/D.

A particular difficulty when physically implementing control circuits 128 or 138 may be in designing latching comparator 132 to work at sufficiently high speed

and providing it with reference and clocking inputs of sufficient precision. For example, whilst in Fig. 21 voltage levels VHHD and VDDD are shown as time invariant, in a physical implementation both VDDD and VHHD are subject to change, particularly the level of VHHD when it is supplied from a reservoir capacitor.

5 Therefore the choice of appropriate level for VREF in relation to the current and immediately prior levels of VHHD and VDDD and circuitry required to furnish signal VREF may become quite complex issues. Likewise, the timing of signal VIDD in control circuits 128 or 138 needs to be accurate and repeatable to a degree which may prove hard to achieve. Furthermore, latching comparator 132 in control circuits 128  
10 or 138 notionally compares the voltage of signal VDO to the voltage of signal VREF at a single instant on the rising edge of clocking signal VIDD. In reality though, due to the finite speed of circuit elements internal to latching comparator 132, that comparator will tend to compare the values of inputs signal VDO and VREF averaged throughout the time duration of a sampling window, approximately (though not  
15 precisely) coinciding with the rising edge of clocking input signal VIDD.

All of these uncertainties may combine to make circuit design difficult and circuit operation erratic. In accordance with a further embodiment of the current invention improved means are provided for furnishing loop feedback signal U/D in control circuit 128 and 138. This is achieved in part by redefining the inputs to  
20 latching comparator 132 to demand less precision and in part by providing an internal circuit for latching comparator 132 which is novel and particular to the application and further relaxes the timing accuracy demanded of clocking signal VIDD.

Fig. 23 shows an alternative resonant line driver comprising a control circuit 138, a ramp circuit 119 similar to that shown in Fig. 14, output MOSFET's Q1, Q2  
25 and Q3 and additional circuitry comprising N-channel MOSFET Q2R and capacitor CRAMP. Capacitor CRAMP furnishes a signal VREFRAMP which functions as described below. The source and drain terminals of N-Channel MOSFET Q2R are connected to signals VHHD and VREFRAMP respectively.

Referring to Fig. 24, reference current output IRFEOUT1 from control circuit  
30 138 initially charges capacitor CRAMP high to the voltage level of VDD. When signal VC2 rises initiating a low to high transition at time t1 and further rises above the level of VHHD time tA, N-Channel MOSFET Q2R turns "ON", discharging capacitor CRAMP and signal REFRAMP to the level of VHHD. Then at time immediately prior to time t3, signal VC2 falls. Prior to the falling edge of signal VC2,

output signal VDO is strongly held at a level close to the level of VHHD because large N-channel MOSFET Q2 is "ON". The falling edge of VC2 is what initiates the ramp beginning at time t3 of signal VDO when N-channel MOSFET Q2 turns "OFF".

Waveform VREFRAMP has a slope between time t3 and t5 that is arranged to  
5 be substantially the same as waveform VDDO in Fig. 21. By using waveform VREFRAMP in place of signal VREF, output signal VDO can be compared with VREFRAMP at any time between times t3 and t5 and the same result can be obtained, thus considerably relaxing the timing requirements for signal VIDD in part of Fig. 23.

It is a considerable benefit of the current invention and in particular the circuit  
10 shown in Fig. 23 that at substantially the same time (t3 in Fig. 24) that N-channel MOSFET Q2N turns "OFF" initiating the ramp of VDO, N-channel MOSFET Q2R also turns "OFF" allowing IREFOUT1 to begin charging capacitor CRAMP. The close timing coincidence of these two events at time t3 is very precise because both MOSFET Q2 and Q2R can be N-channel devices formed on the same substrate  
15 sharing a common gate signal VC2 and a common source signal VHHD. Furthermore, the slope of signal VREFRAMP between time t3 and t5 is proportional to the reference current IREFOUT1, which is in turn proportional to the reference current IREFOUT, which (through ramp circuit 119) substantially determines the slope of the VDO ramp beginning at time t1. Therefore the slope of signal VREFRAMP between  
20 times t3 and t5 can be arranged to be always substantially the same as the slope of the ramp of output signal VDO beginning at time t1, and when signals VDO and VREFRAMP are compared at any time between t3 and t5 by latching comparator 132 (Fig. 23) then a loop feedback signal U/D can be furnished, which very accurately discriminates waveform VDOE of output signal VDO from waveform VDOL of  
25 output signal VDO. Thus up/down counter 130 and digitally controlled current source 140 allow current controlled delay 135 in control circuit 138 (all shown in Fig. 22) to be adjusted very close to an optimum value.

Instead of comparing the voltage level of output signal VDO to the voltage level of signal VREFRAMP at some single time between time t3 and t5 in Fig. 24,  
30 still further accuracy may be obtained if the difference voltage between the two signals is time integrated between times t3 and t5 using what (for ease of reference) will be called an integrating latching comparator. Such a comparator has inherent advantages in terms of accuracy and noise immunity. However when implemented in a resonant line driver operating at high speed there may be difficulties in furnishing to

an integrating latching comparator a signal or combination of signals that accurately delimits the desired period of integration. A further embodiment of the current invention employs an integrating latching comparator circuit which largely overcomes this issue.

5           Turning to Fig. 25, this figure shows an integrating latching comparator 150 with comparator inputs VREFRAMP and VDO and furnishing comparator outputs Q and QN. Integrating latching comparator 150 also accepts a reference current IREF and latching control signals VE2N, EXTENT and EXTENT\_NOT where suitable. Example timing of for these control signals is shown in the lower part of Fig. 24.

10           The input stage of integrating latching comparator 150 comprises capacitors CCOMP1 and CCOMP2, current bias generating N-channel MOSFETs Q102 and Q103, shorting N-channel MOSFET Q104 and differential input N-channel MOSFETs Q105 and Q106. Output nodes Q and QN are rapidly shorted, upon VE2N going to a low level shortly before time t1 in Fig. 24, and are driven to the voltage  
15           level of VDDD by P-channel MOSFETs Q111, Q109 and Q110. Initially N-channel MOSFETs Q105 and Q106 act as source followers with bias current supplies by N-channel MOSFETs Q102 and Q103 and therefore capacitors CCOMP1 and CCOMP2 track the voltage levels of input signals VREFRAMP and VDO shifted lower by the gate-source bias voltage of Q105 and Q106. Then, when signal EXTENT goes to a  
20           high level, N-channel MOSFET Q104 is switched "ON" and shorts source terminals of N-channel MOSFETs Q105 and Q106 so that they now function as a differential pair with bias current again supplied by N-channel MOSFETs Q102 and Q103. The output current of the differential pair flows to output nodes Q and QN so that when, shortly before time t3 in Fig. 24, VE2N goes to a high level and Q109, Q110 and  
25           Q111 are switched "OFF", this output current begins charging output nodes Q and QN and associated capacitance (provided mainly by the gate capacitance of P-channel MOSFETs Q107 and Q108 and N-channel MOSFETs Q112 and Q113). The current source formed by Q102 and Q103 is arranged to supply only a modest amount of current so that even if VE2N happens relatively far in advance of time t3, output  
30           nodes Q and QN remain quite near to the level of VDDD and thus the relative timing of VE2N is non-critical in relation to time t3 save that it should go to a low level in advance of time t3. Now when input signals VREFRAMP and VDO begin their respective ramps at or near time t3, being connected to the gate terminals of N-channel MOSFETs Q105 and Q106, the respective source terminals Q105 and Q106

shorted by Q104 also begin to rise in voltage and to charge capacitors CCOMP1 and CCOMP2.

Note that when Q114 is closed for regeneration, Q104 is closed and serves to separate the differential pair of Q105 and Q106 at that time.

5       The integrating latching comparator 150 has a positive input VDO which receives the partial output transition, and a negative input VREFRAMP which receives a signal corresponding to (i.e. representative of) a reference ramp. The integrating latching comparator accumulates charge on the comparator output nodes (Q and QN) only during a time when either of the two input signals is rising. It  
10 provides an average comparison over the whole ramping period, i.e. over the time of the partial output transition.

A positive feedback regeneration circuit comprising the transistors Q107 to Q114 receives charge at the comparator output nodes Q and QN via the differential input transistor pair. The regeneration circuit takes a small difference on nodes Q and  
15 QN, and, when EXTENTNOT causes Q114 to conduct, it amplifies this small difference to a full rail voltage.

Capacitors CCOMP1 and CCOMP2 are sized such that charging them requires quite a large current in relation to the modest bias current supplied by Q102 and Q103 so that the total bias current through the differential pair formed by Q105 and Q106  
20 becomes quite large, but only while input signals VDO and VREFRAMP continue to rise. The circuit therefore embodies an inherent feature which tends to integrate the difference voltage between inputs VREFRAMP and VDO only during their respective ramp period between time t3 and t5 in Fig. 24. This feature further relaxes the timing precision required of control input signals to integrating latching comparator 150. By  
25 time t5 in Fig. 24, the difference voltage between inputs VREFRAMP and VDO will have been time integrated by charge accumulation to produce a small difference in the voltage levels of output nodes Q and QN. Finally this voltage is amplified to a full rail voltage when signal EXTENT\_NOT goes to a high level after time t5 in Fig. 24, since the current flowing through N-channel MOSFET Q114 strongly biases cross  
30 coupled N-channel MOSFET pair Q112 and Q113, which regenerate any pre-existing voltage difference at output nodes Q & QN by positive feedback assisted by a similar mechanism applying to cross coupled P-channel MOSFET pair Q107 and Q108.

Again the timing of the rising edge of control signal EXTENT\_NOT is non-critical in relation to time t5 in Fig. 24, save that it should occur after time t5. The

- final state of output signals Q & QN will be such that one is at the level of VDDD and the other at the level of VSSD depending on the time integrated difference voltage between input signals VREFRAMP and VDO between time t3 and t5 in Fig. 24. Integrating latching comparator 150 along with suitable circuitry to furnish control
- 5 signals EXTENT and EXTENT\_NOT could therefore replace latching comparator 132 in control circuit 138 of Fig. 23 with one of its output signal Q or QN chosen for appropriate logic polarity furnishing loop feedback signal U/D in Fig. 23.

## CLAIMS

1. An electronic driver circuit for generating a circuit output signal providable to an electrical conductor (12) that furnishes a conductor output signal providable to a load (14), the circuit and conductor output signals respectively making corresponding circuit and conductor output transitions approximately between a pair of output voltage levels ( $V_{DD}$ ,  $V_{SS}$ ) between which there is an intermediate voltage level ( $V_{HH}$ ), inductance and capacitance of the conductor and the load producing resonance that enables the conductor output signal to largely complete each conductor output transition while the circuit output signal is being held at approximately the intermediate voltage level for a non-zero intermediate-level holding period during the corresponding circuit output transition, the circuit comprising a ramp control circuit (118, 119) for controlling partial circuit output transitions between at least one of the pair of output voltage levels and the intermediate level to provide a substantially non-zero transition time for a partial circuit output transition.
2. A driver circuit according to claim 1 wherein the partial circuit output transition is controlled to be slow relative to other switching events in the circuit.
3. A driver circuit according to claim 1 or 2, further comprising a pull-up transistor (Q3) and a pull-down transistor (Q1) for pulling the circuit output up to a first of the two output voltage levels and down to a second of the two output voltage levels, wherein the partial circuit output transition is controlled to be slower than the switching of the pull-up and pull-down transistors.
4. A driver circuit according to claim 1, 2 or 3, further comprising an intermediate level driving transistor (Q2, Q2N) which in switching-on drives the circuit output to the intermediate voltage level and in switching-off permits the circuit output to be driven to a first of the two output voltage levels, wherein the partial circuit output transition is controlled to be slower than the switching-off of the intermediate level driving transistor.
5. A driver circuit according to any one of the preceding claims, wherein the partial circuit output transition time is adjustable.

6. A driver circuit according to any one of the preceding claims, wherein the partial circuit output transition time is controllable as a function of the time taken for the conductor output signal to largely complete a conductor output transition.

5

7. A driver circuit according to claim 1 wherein the control circuitry comprises:

time-comparison circuitry for comparing the circuit output signal and the second control signal to determine whether the circuit output signal completes a circuit output transition before the second control signal completes the corresponding control transition; and

adjustment circuitry for adjusting the partial circuit transition time depending on the comparison.

15

8. A driver circuit according to claim 1, comprising reference ramp circuitry for generating a reference ramp, and comparator circuitry coupled to the reference ramp circuitry for comparing a partial circuit output transition with the reference ramp.

9. A driver circuit according to claim 8, wherein the comparator circuitry compares a level of the partial circuit output transition with a reference voltage ( $V_{REF}$ ) that is approximately midway between the intermediate voltage level ( $V_{HHD}$ ) and an output voltage level to which the output is transitioning ( $V_{DDD}$ ,  $V_{SSD}$ ) at a time ( $t_4$ ) approximately midway between a start ( $t_3$ ) of the partial circuit output transition and an expected completion of the partial circuit output transition.

25

10. A driver circuit according to claim 8, wherein the comparator circuitry comprises an integrating latching comparator to provide an average comparison between a partial circuit output transition and a signal representative of the reference ramp over substantially the whole time of the partial output transition.

30

11. A driver circuit according to claim 10, wherein the comparator comprises:  
a first input ( $V_{DO}$ ) for receiving the partial circuit output transition;

a second input ( $V_{\text{REFRAMP}}$ ) for receiving a signal representative of a reference ramp; and

a pair of output nodes (Q and QN);

wherein the integrating latching comparator accumulates charge on the  
5 comparator output nodes only during a time when one of the first and second input signals is rising.

12. A driver circuit according to any one of claims 8 to 11, further comprising adjustment circuitry for adjusting the partial circuit transition time depending on the  
10 comparison.

13. A driver circuit according to any one of the preceding claims, wherein the time taken for a partial circuit transition is controlled as a function of characteristics of at least one previous circuit output transition.

15

14. A driver circuit according to claim 13, wherein said characteristics are determined from relative timing of two signals.

15. A driver according to any one of the preceding claims, wherein the ramp  
20 control circuit comprises a source follower for driving the circuit output signal in a controlled manner.

16. A driver according to any one of the preceding claims, comprising a switch (Q2N) connected between a source of the intermediate voltage level ( $V_{\text{HH}}$ ) and the  
25 circuit output signal, wherein the ramp control circuit comprises a current mirror (Q20, Q21) which supplies a current to the switch to drive the circuit output signal in a controlled manner.

17. A driver according to claim 16, further comprising a controlled current source  
30 (120) for supplying a controlled current to the current mirror.

18. A driver according to claim 17, wherein the current is controlled as a function of the time taken for the conductor output signal to largely complete a conductor output transition.

19. An electronic driver circuit in accordance with any one of the preceding claims, coupled between sources of different first, second, and third supply voltages, the second supply voltage ( $V_{HH}$ ) lying between the first and third supply voltages, the  
5 circuit comprising:

control circuitry responsive to a circuit input signal for generating different first, second, and third control signals;

10 a first switch (Q3) having (a) a first flow electrode coupled to the source of the first supply voltage, (b) a second flow electrode coupled to an output node from which a circuit output signal ( $V_{DO}$ ) is provided, and (c) a control electrode responsive to the first control signal for controlling current flow between the first switch's flow  
electrodes;

15 a second switch (Q1) having (a) a first flow electrode coupled to the source of the second supply voltage, (b) a second flow electrode coupled to the output node, and (c) a control electrode responsive to the second control signal for controlling current flow between the second switch's flow electrodes; and

20 a third switch (Q2) having (a) a first flow electrode coupled to the source of the third supply voltage, (b) a second flow electrode coupled to the output node, and (c) a control electrode responsive to the third control signal ( $V_{C2}$ ) for controlling current flow between the third switch's flow electrodes, the circuit output signal  
25 making rising and falling circuit output transitions approximately between the first and third supply voltages, the circuit output signal staying approximately at the second supply voltage for a non-zero intermediate-level holding period during each circuit output transition, the transition time between the first and third supply  
voltages and/or between the second and third supply voltages being controlled.

30 20. A driver according to claim 19, the circuit output signal making rising and falling circuit output transitions approximately between the first and third supply voltages, wherein the third switch operates as a source follower such that the output node follows its control electrode voltage in a controlled manner.

21. A driver according to claim 19, wherein the third switch is an N-channel transistor, and wherein a capacitor ( $C_{FB}$ ) is provided for checking the rate of rise of the current to the control electrode of the third transistor when the circuit output signal falls from the first voltage to the third voltage.

22. A driver according to any one of the preceding claims, wherein a ramp control circuit (118, 119) controls a partial circuit output transition as a function of a current stored control value stored as a result of a previous partial circuit output transition.

10

23. An electronic driver circuit for generating a circuit output signal providable to an electrical conductor (12) that furnishes a conductor output signal providable to a load (14), the circuit and conductor output signals respectively making corresponding circuit and conductor output transitions approximately between a pair of output voltage levels ( $V_{DD}$ ,  $V_{SS}$ ) between which there is an intermediate voltage level ( $V_{HH}$ ), inductance and capacitance of the conductor and the load producing resonance that enables the conductor output signal to largely complete each conductor output transition while the circuit output signal is being held at approximately the intermediate voltage level for a non-zero intermediate-level holding period during the corresponding circuit output transition, the circuit including at least a first capacitor element between the intermediate voltage level and the first voltage level and at least a second capacitor element between the intermediate voltage level and the second voltage level.

24. A driver circuit according to claim 23, wherein the first and second capacitor elements are substantially equal.

25. A driver circuit according to claim 24 wherein the first and second capacitor elements form a split-reservoir capacitor.

30

26. A driver circuit according to claim 23, 24 or 25, wherein a package lead inductance exists between the electrical conductor (12) and a source of each of the pair of output voltage levels and wherein the first and second capacitor elements are

such that a change in circuit output voltage causes return current flowing back into the driver to be split approximately equally between the package lead inductances.

27. A driver circuit according to any one of claims 23 to 26, wherein the first and  
5 second capacitor elements provide decoupling capacitance between the output voltage levels ( $V_{DD}$ ,  $V_{SS}$ ).

28. An electronic driver circuit for generating a circuit output signal providable to  
an electrical conductor (12) that furnishes a conductor output signal providable to a  
10 load (14), the circuit and conductor output signals respectively making corresponding circuit and conductor output transitions approximately between a first voltage ( $V_{DD}$ ), a second voltage ( $V_{SS}$ ) and an intermediate voltage ( $V_{HH}$ ) between the first and second voltages, the circuit comprising:

15 a first transistor (Q3) having (a) a first flow electrode coupled to a source of the first voltage, (b) a second flow electrode coupled to an output node from which a circuit output signal ( $V_{DO}$ ) is provided, and (c) a control electrode responsive to a first control signal for controlling current flow between the first transistor's flow electrodes;

20 a second transistor (Q1) having (a) a first flow electrode coupled to a source of the second voltage, (b) a second flow electrode coupled to the output node, and (c) a control electrode responsive to a second control signal for controlling current flow between the second transistor's flow electrodes;

25 a third transistor (Q2) having (a) a first flow electrode coupled to a source of the intermediate voltage, (b) a second flow electrode coupled to the output node, and (c) a control electrode responsive to a third control signal ( $V_{C2}$ ) for controlling current flow between the third transistor's flow electrodes; and

30 fourth and fifth transistors connected between the control electrode of the third transistor and the sources of the first and second voltage levels respectively, and control circuitry for selectively discharging the control electrode of the third transistor to the first and second voltage levels respectively through the fourth and fifth

transistors such that the control electrode of the third transistor makes partial transitions between the first and second voltage levels,

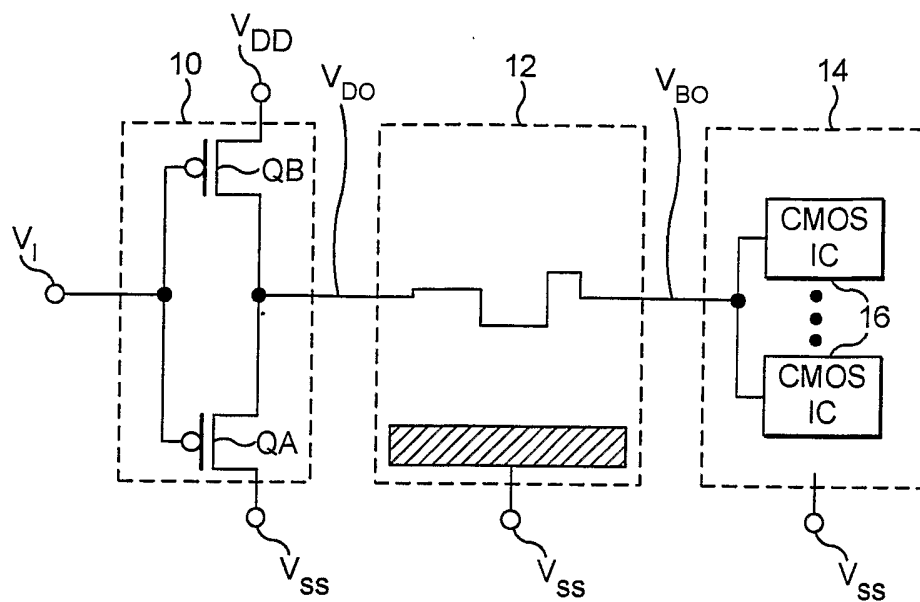
5       whereby the output signal makes rising and falling circuit output transitions approximately between the first and second voltages controlled by the first, second and third control signals, and the circuit output signal stays approximately at the intermediate voltage for a non-zero intermediate-level holding period during each circuit output transition.

10   29.     A driver circuit according to claim 28, further comprising control circuitry to provide the first, second and third control signals to cause the circuit output signal to stay approximately at the intermediate supply voltage for a non-zero intermediate-level holding period during each circuit output transition.

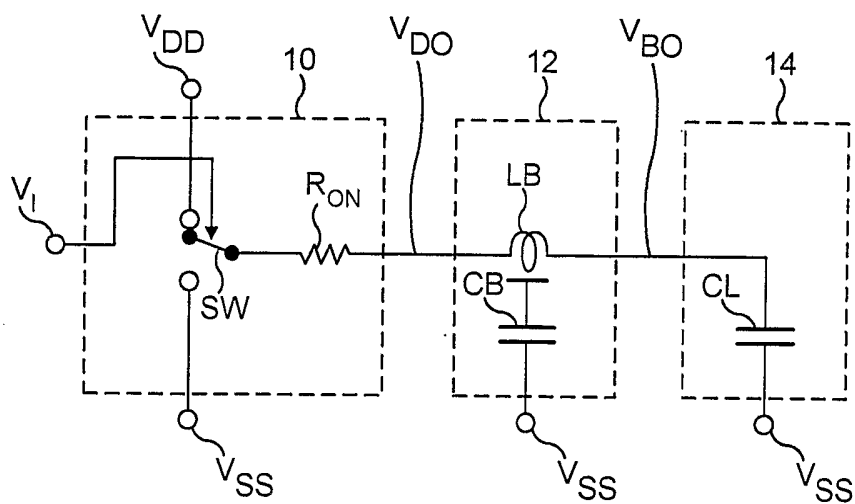
15   30.     A driver circuit according to claim 28 or 29, wherein the control circuit comprises timing control circuitry to control times of transition of the circuit output signal between one of the first and second supply voltages and the intermediate supply voltage.

20   31.     A driver circuit according to claim 29, wherein the control circuit comprises reference ramp circuitry for generating a reference ramp, and comparator circuitry coupled to the reference ramp circuitry for comparing a partial circuit output transition with the reference ramp.

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**FIG. 1a**  
PRIOR ART



**FIG. 1b**  
PRIOR ART

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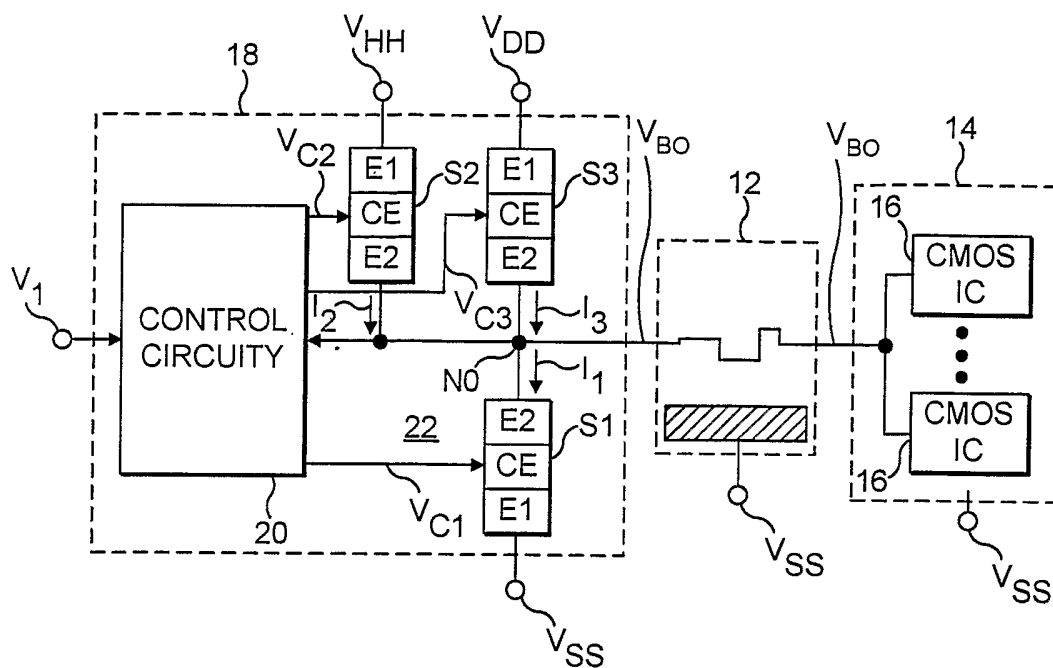


FIG. 2a  
PRIOR ART

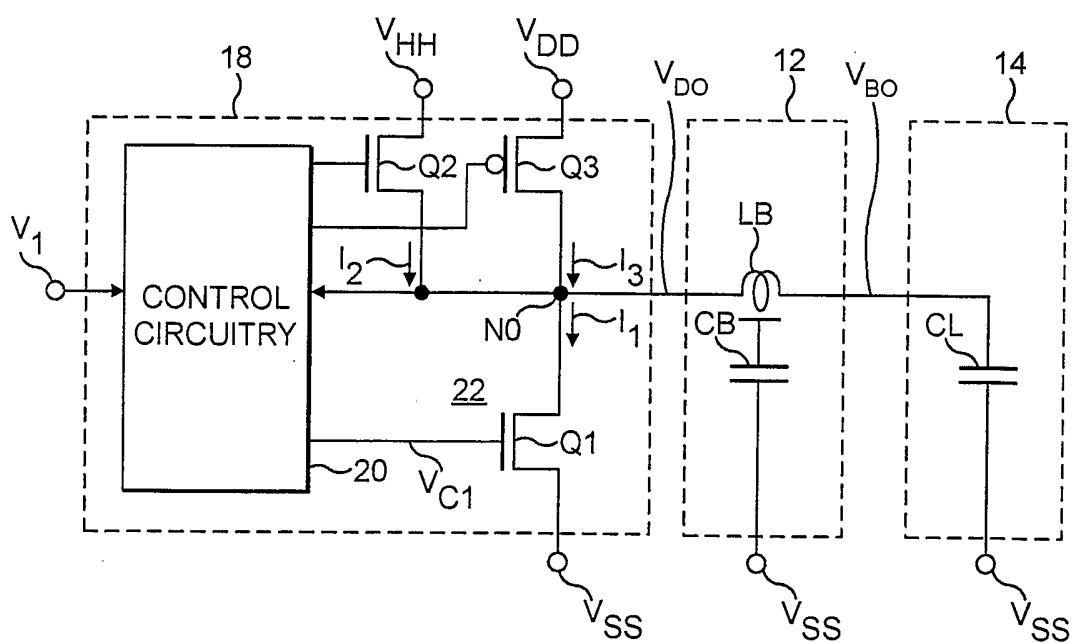


FIG. 2b  
PRIOR ART

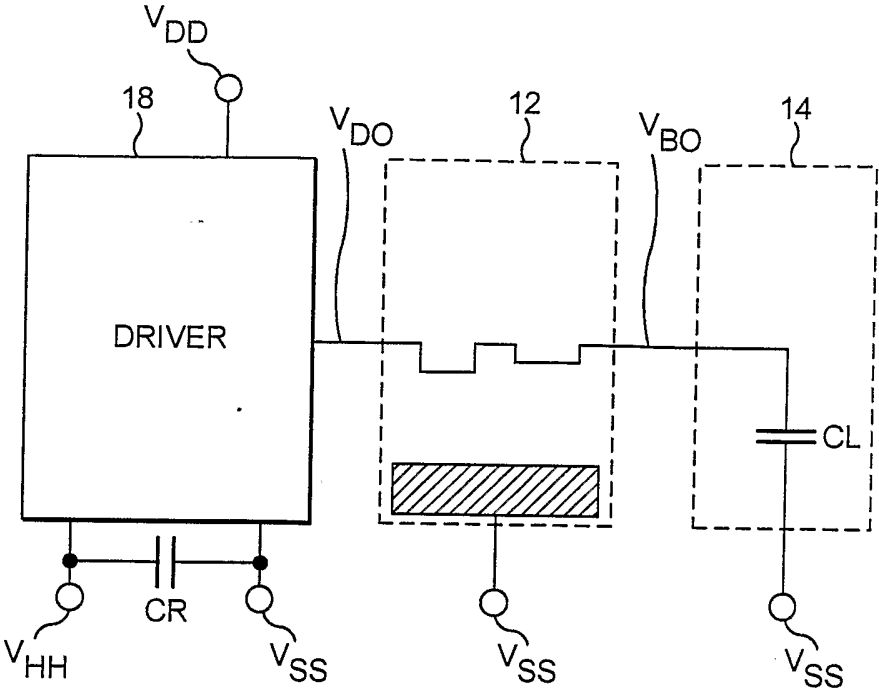


FIG. 3  
PRIOR ART

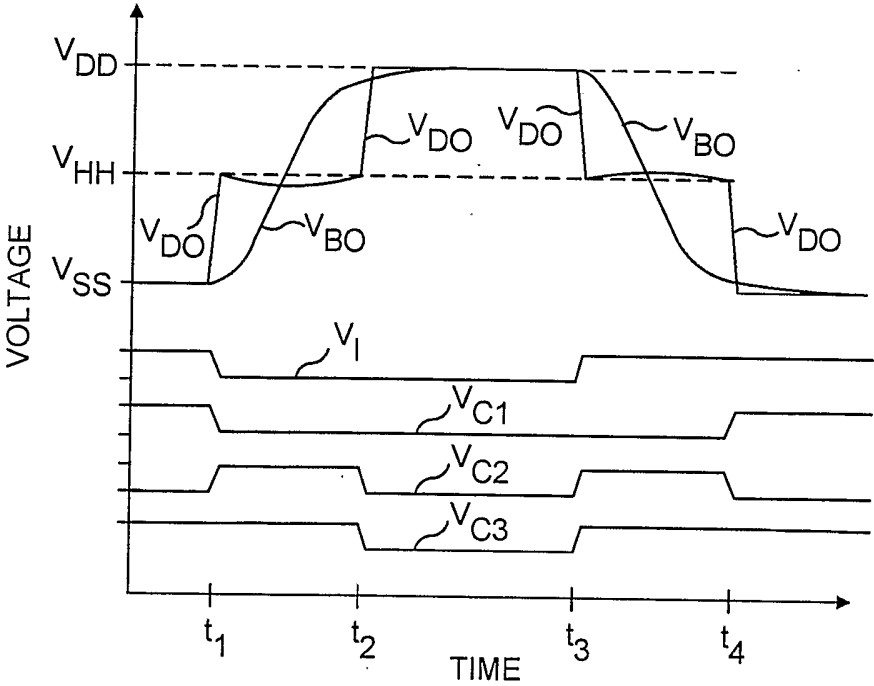


FIG. 4  
PRIOR ART

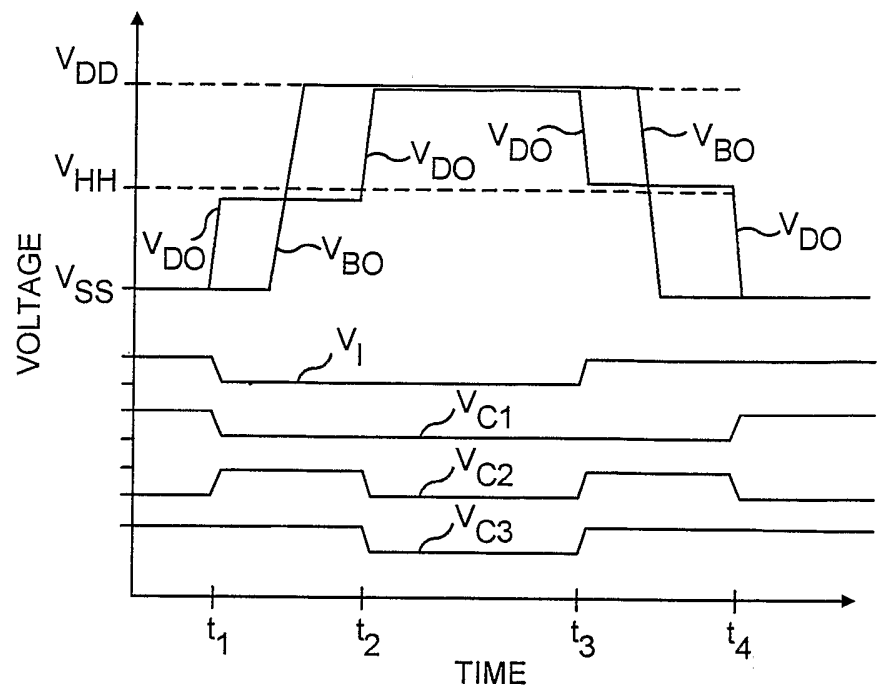


FIG. 5  
PRIOR ART

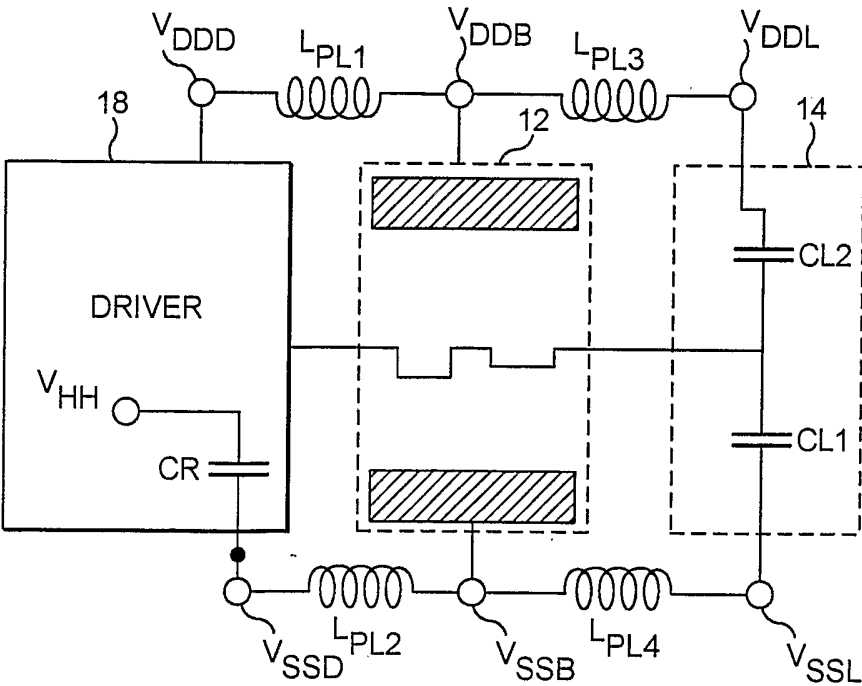


FIG. 6

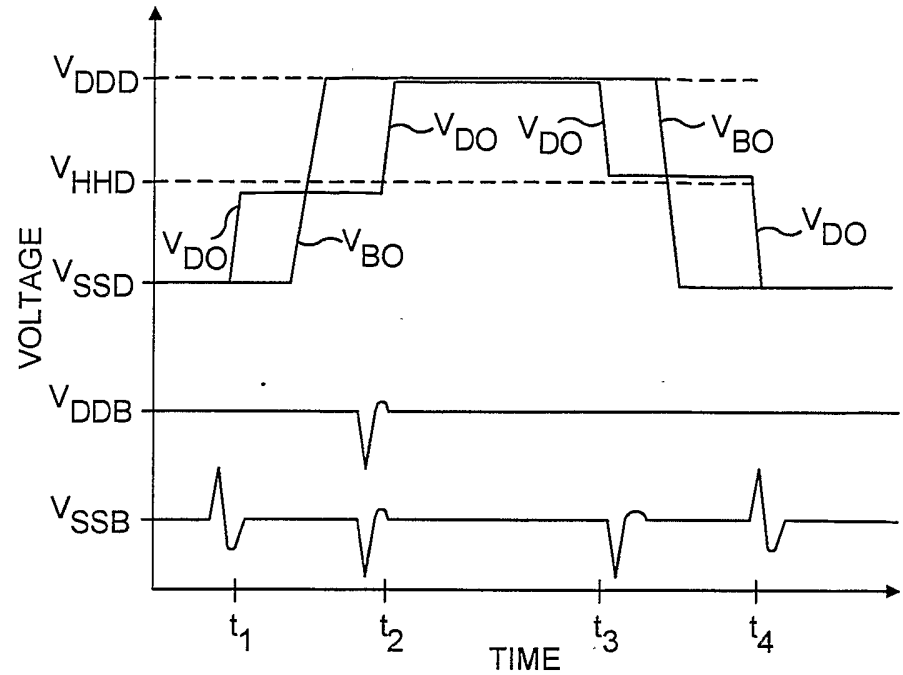


FIG. 7

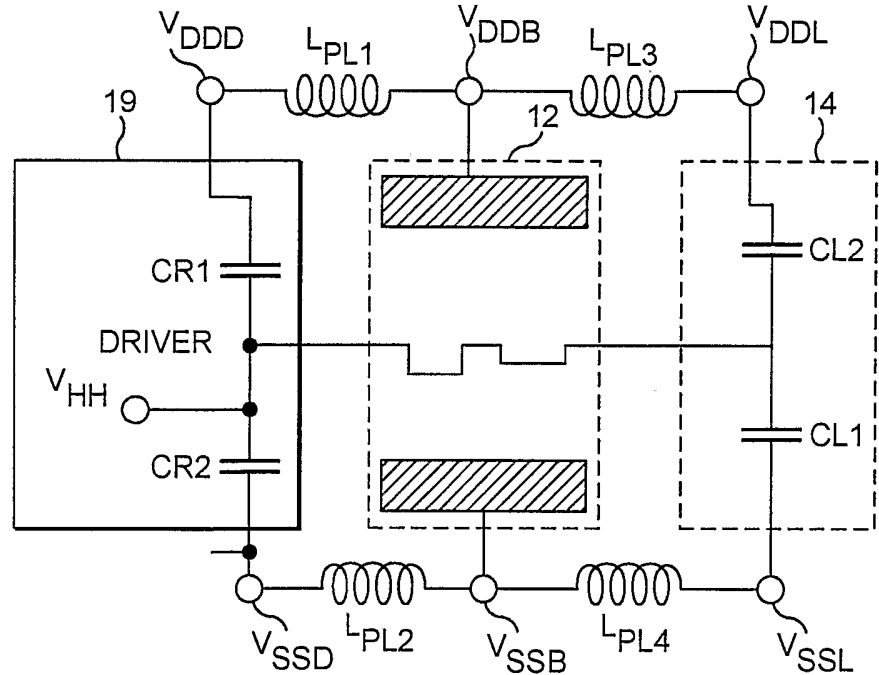


FIG. 8

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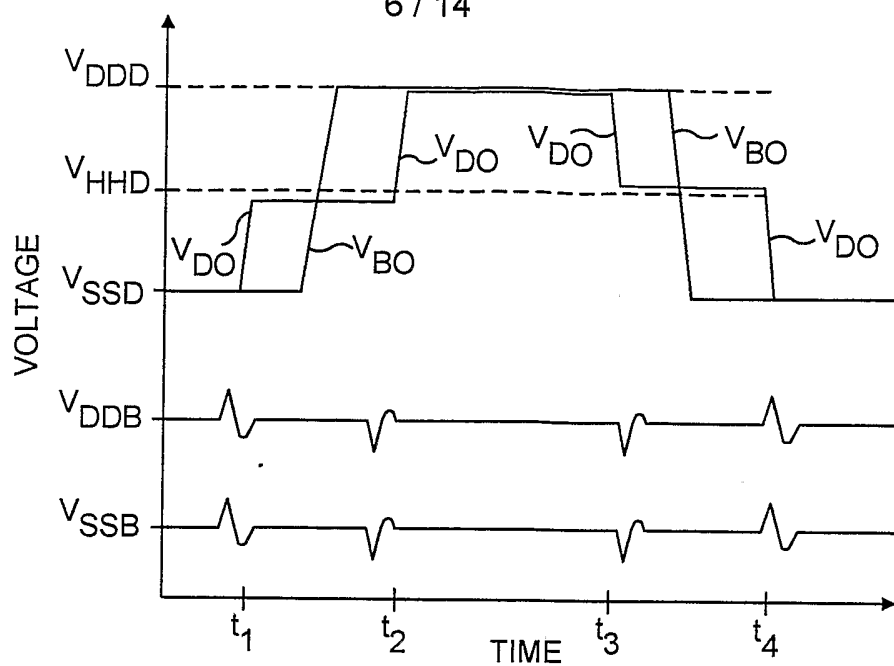


FIG. 9

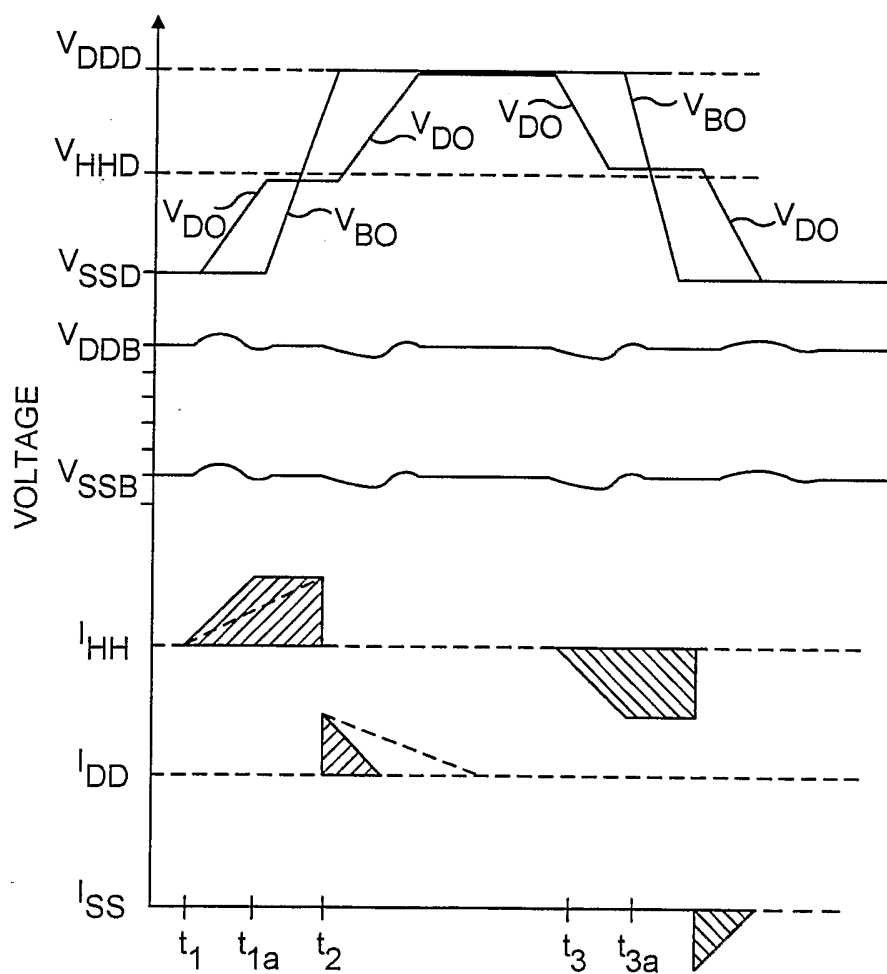


FIG. 10

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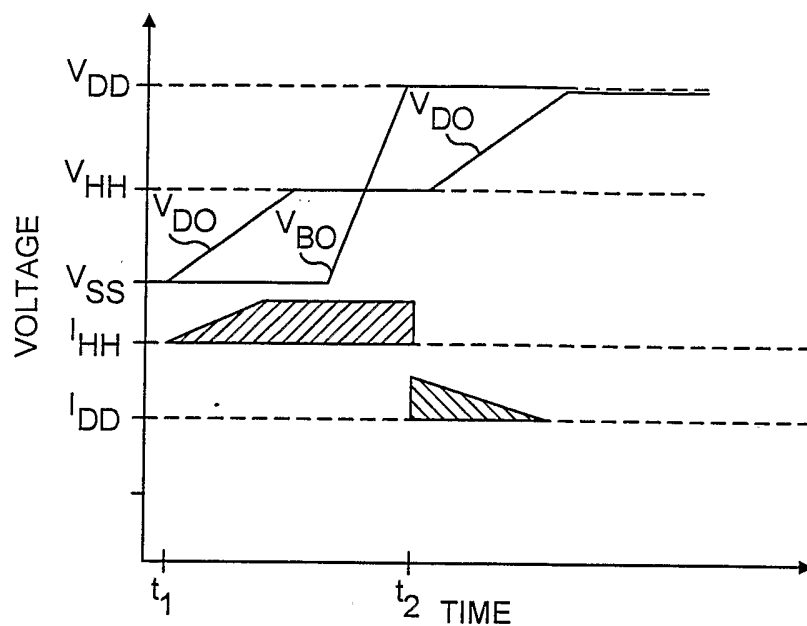


FIG. 11

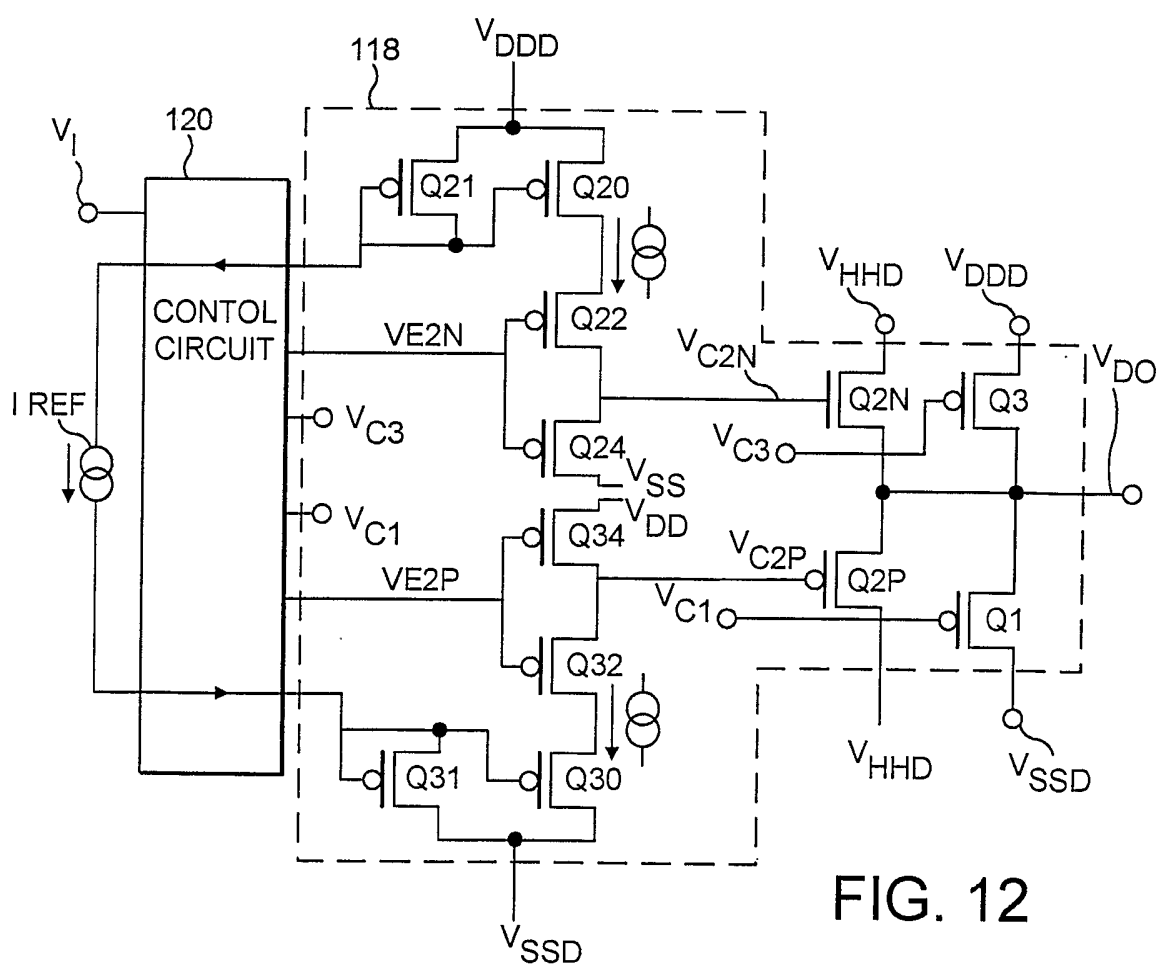
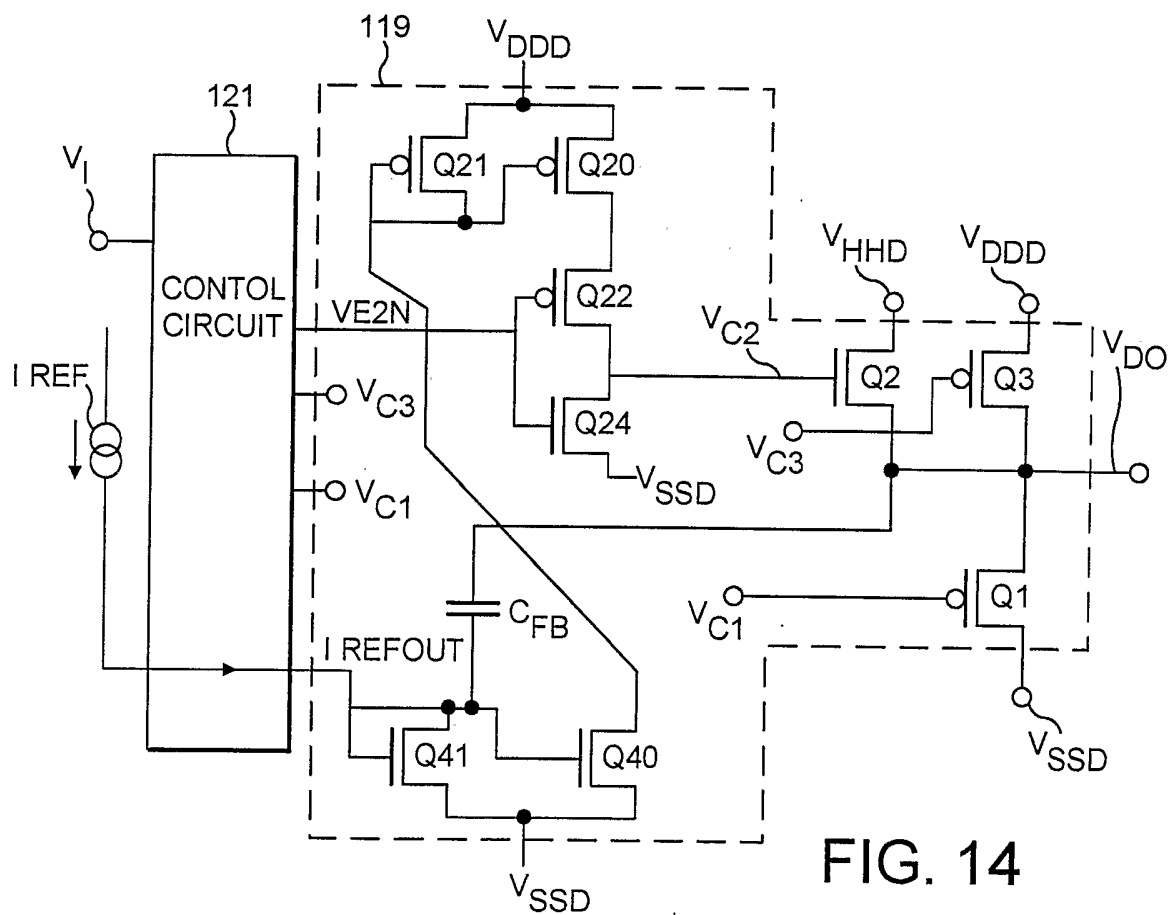
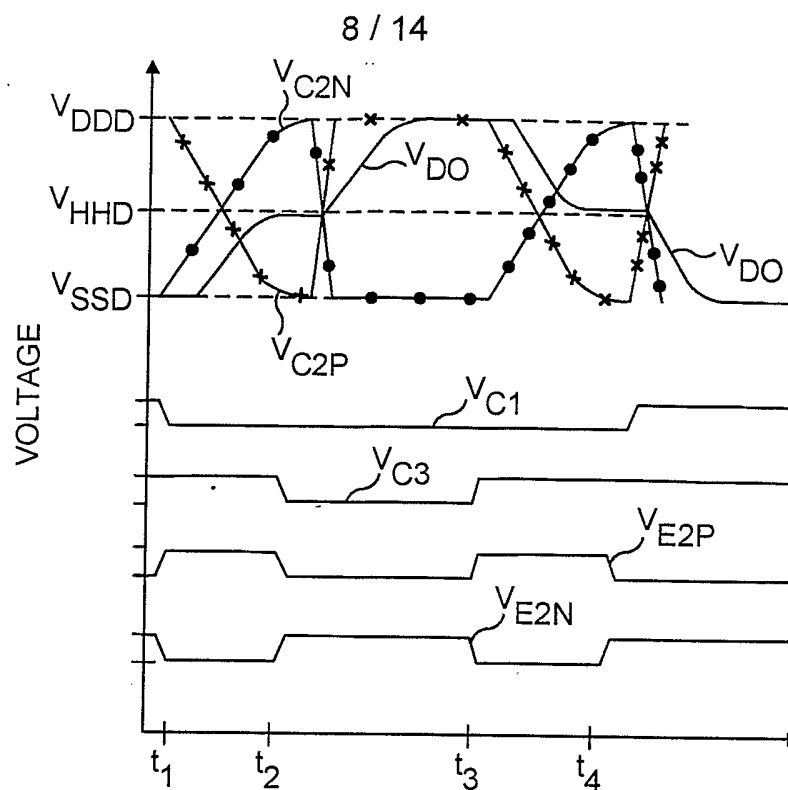


FIG. 12



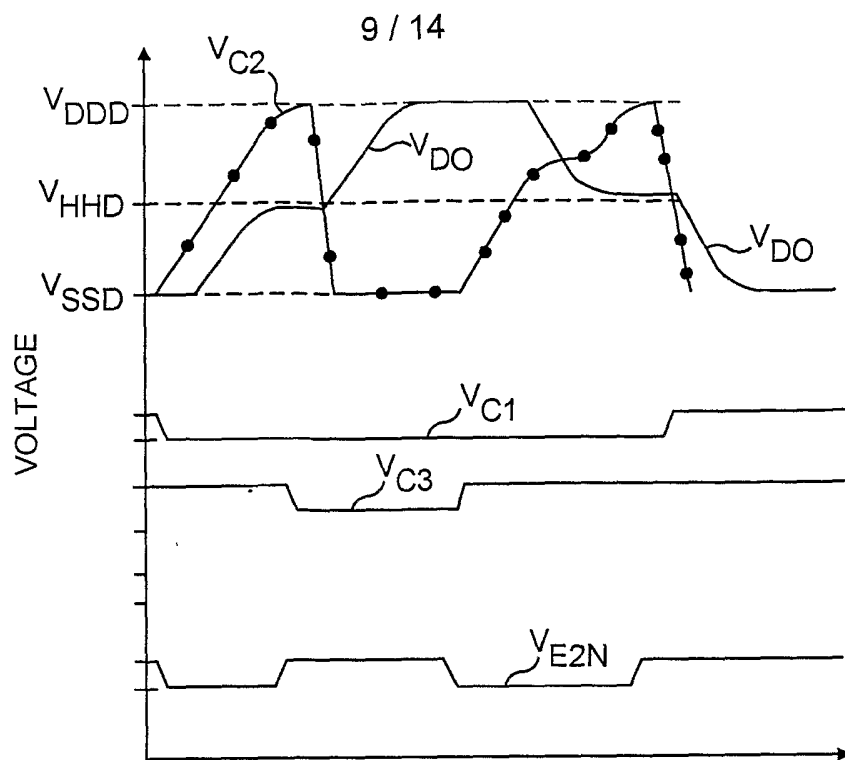


FIG. 15

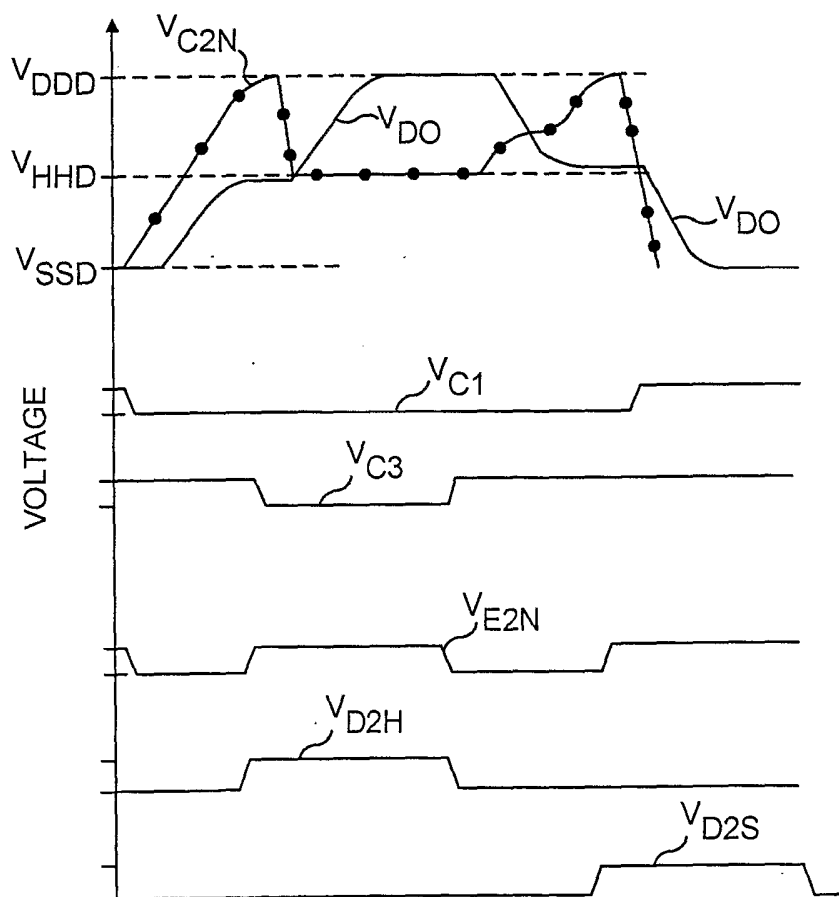


FIG. 16

10 / 14

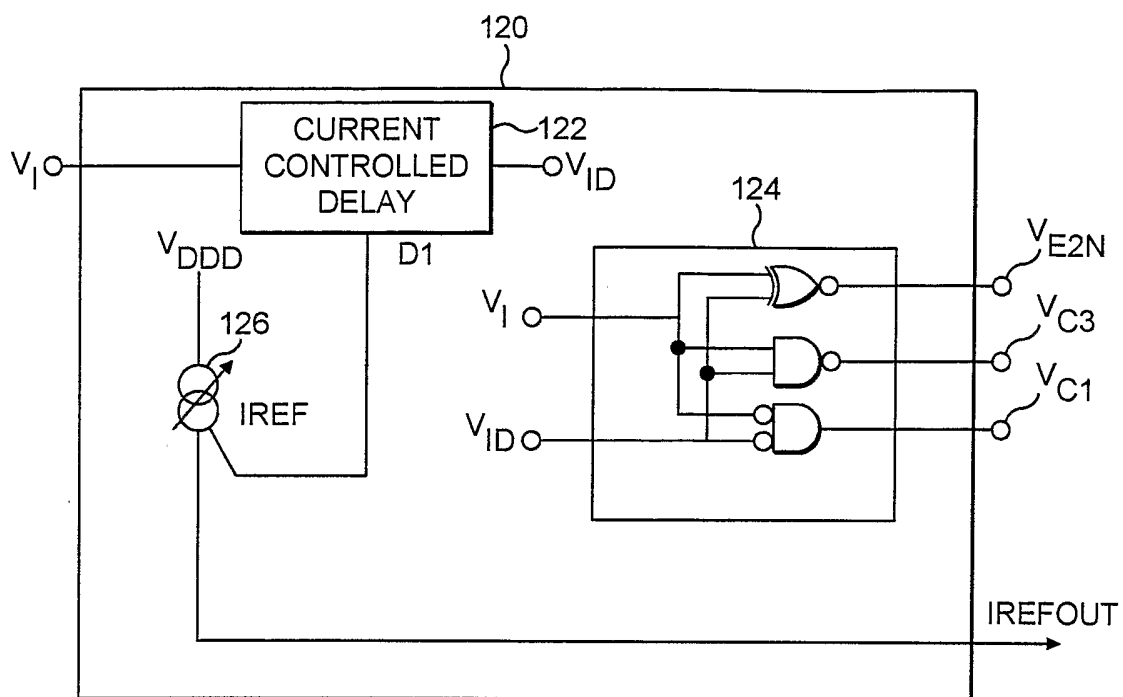
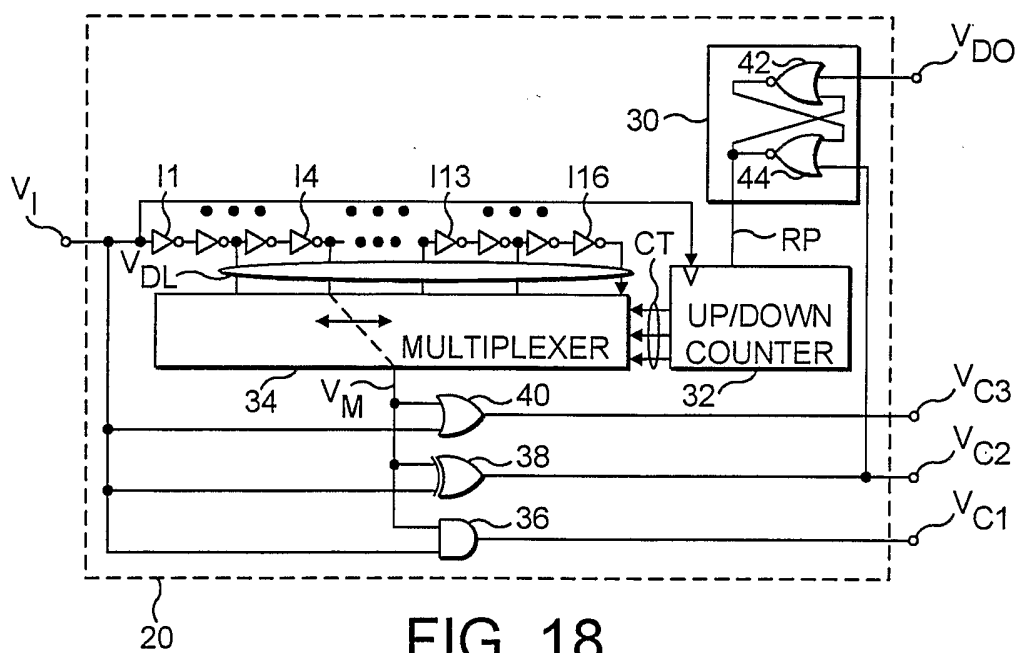


FIG. 17

FIG. 18  
PRIOR ART

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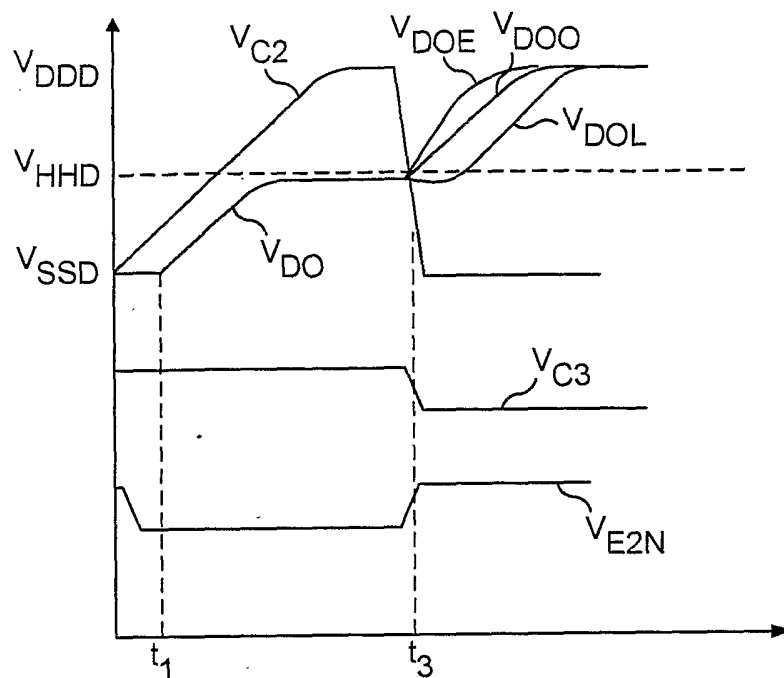


FIG. 19

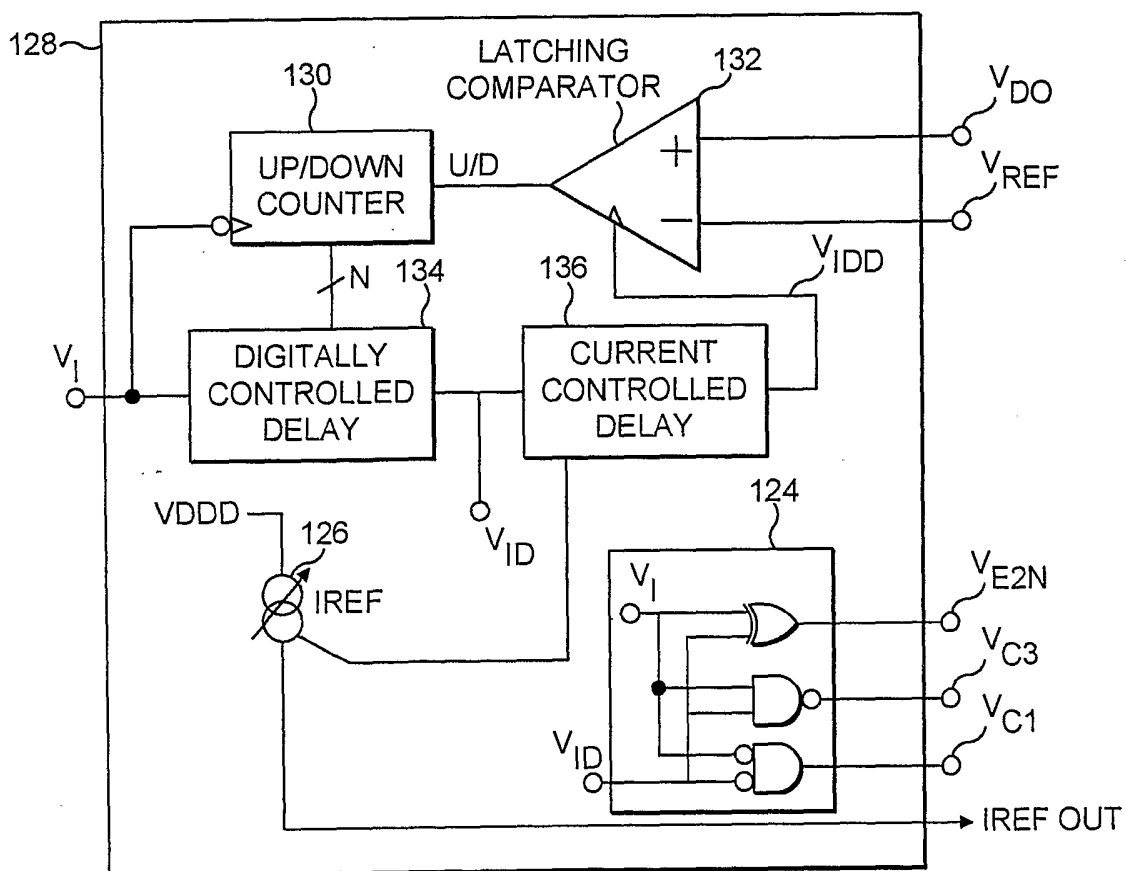


FIG. 20

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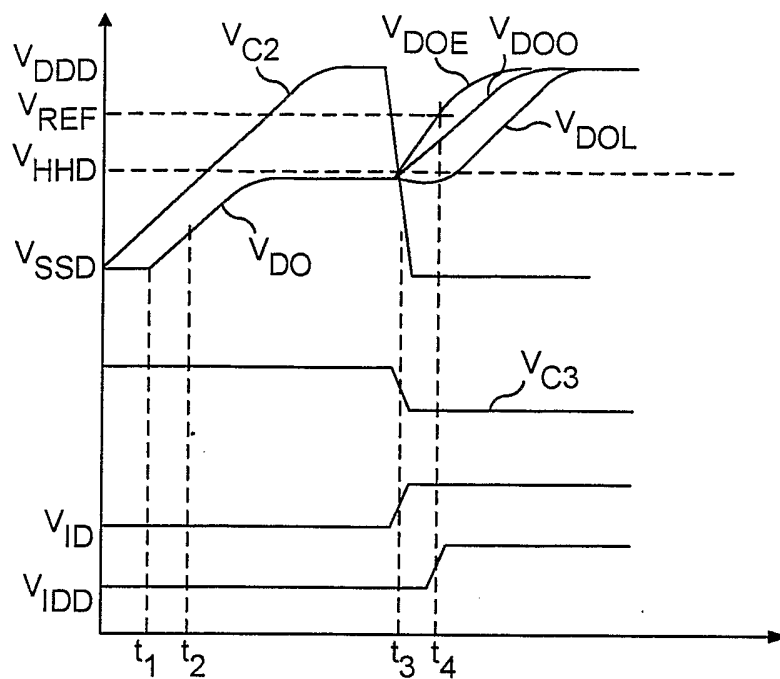


FIG. 21

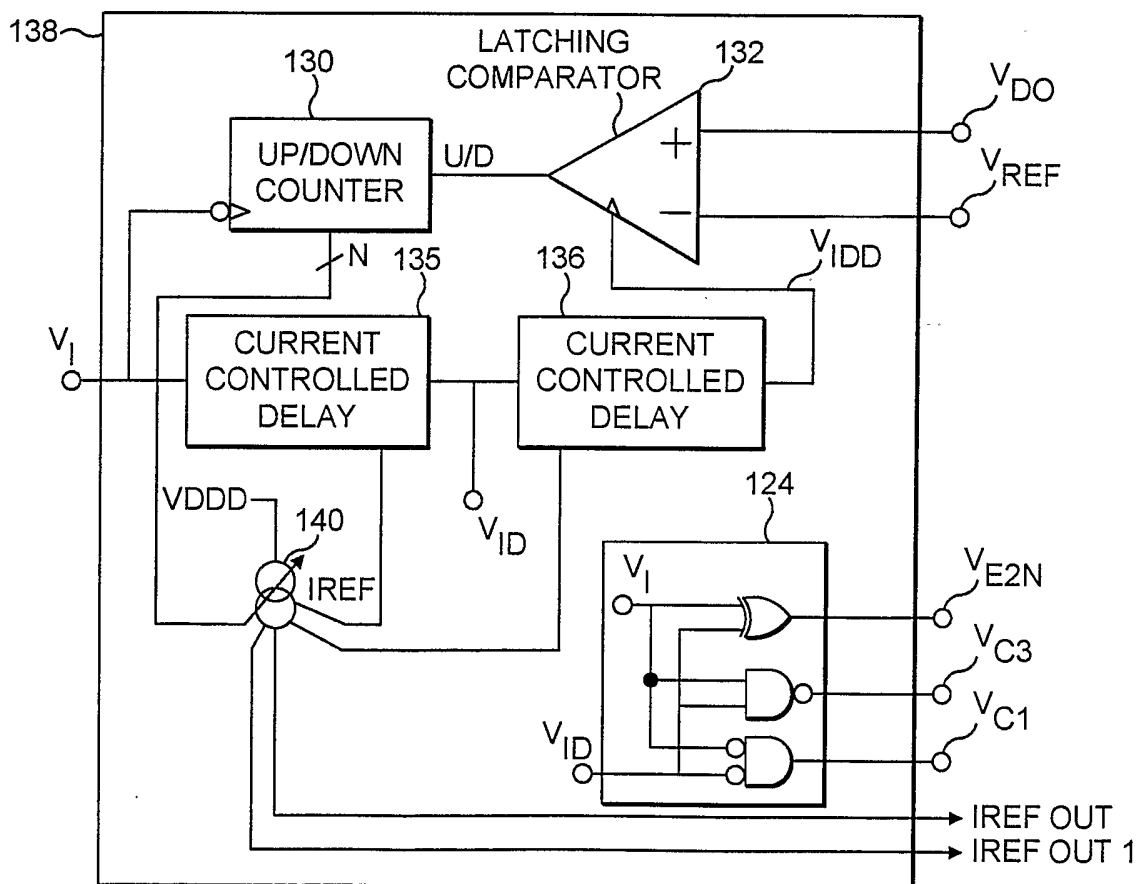


FIG. 22



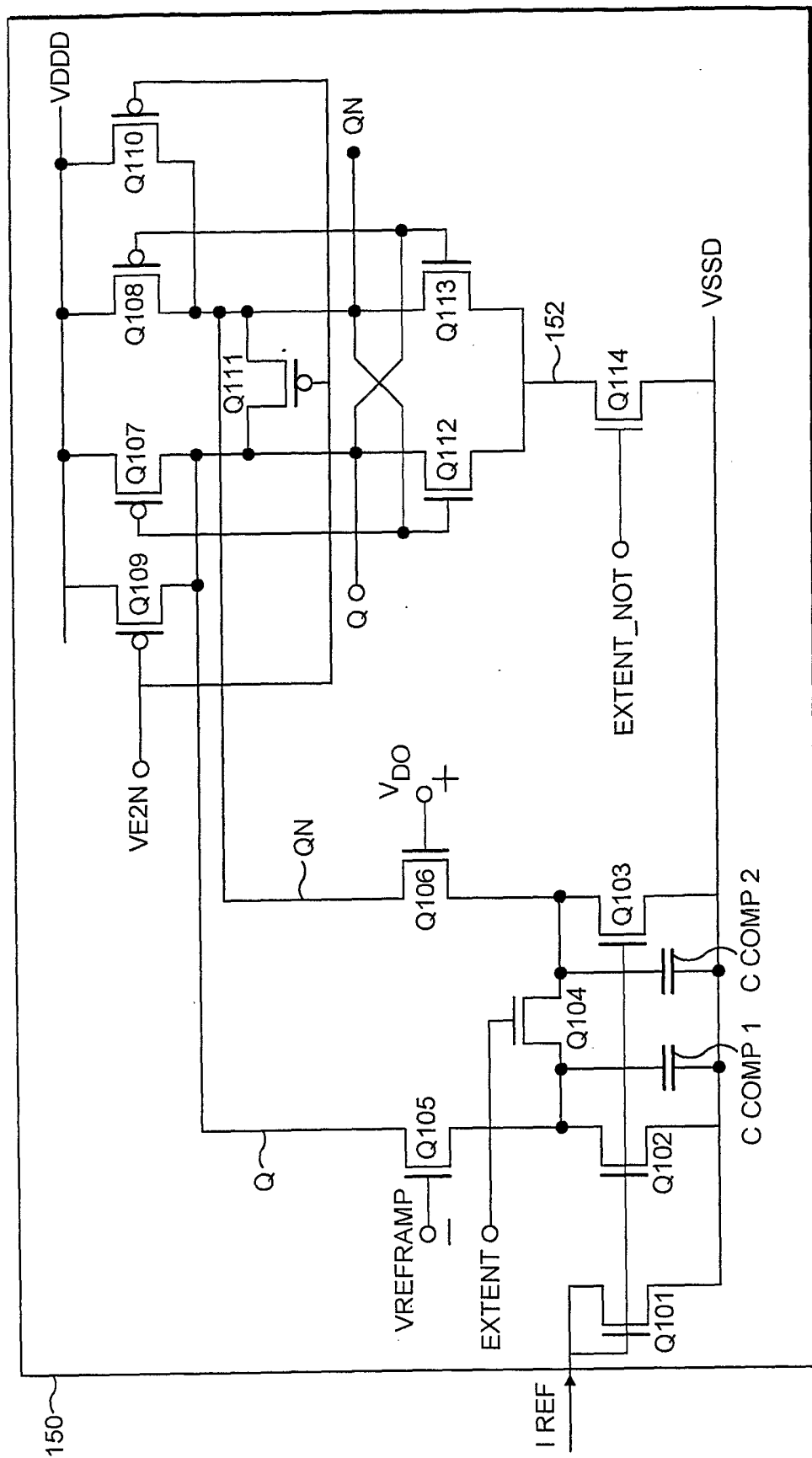


FIG. 25