(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 October 2018 (11.10.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/187263 A1

(51) International Patent Classification:
H03H 11/26 (2006.01)

(21) International Application Number:
PCT/US2018/025794

(22) International Filing Date:
03 April 2018 (03.04.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/481,053 06 April 2017 (06.04.2017) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 15/481,053 (CON)
Filed on 06 April 2017 (06.04.2017)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku Tokyo, 160-8366 (JP).

(72) Inventor: **TOOPS, David, J.**; 1155 Scarlett Drive, Lucas, TX 75002 (US).

(74) Agent: **DAVIS, Michael A, Jr.**; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,

(54) Title: A RESISTOR-CAPACITOR (RC) DELAY CIRCUIT WITH A PRECHARGE MODE

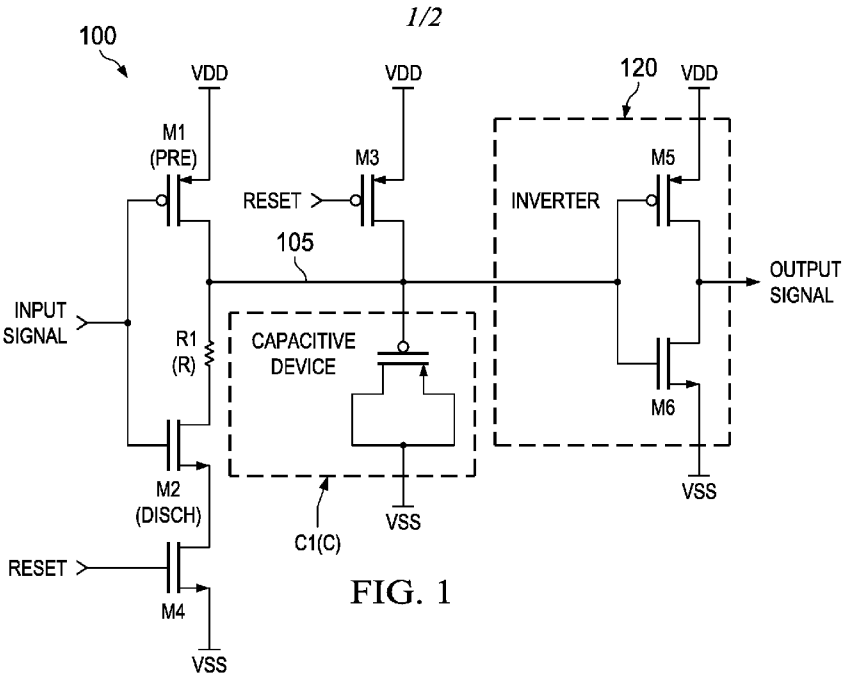

FIG. 1

(57) Abstract: A delay circuit (100) includes precharge and discharge transistors (Ml, M2) configured to receive an input signal. The delay circuit (100) also includes a resistor (Rl) coupled to the precharge transistor (Ml) having a negative temperature coefficient to thereby form a node (105). A capacitive device (CI) and an inverter (120) are coupled to the node (105). The inverter (120) produces an output signal. Responsive to the input signal having a first polarity, the precharge transistor (Ml) is configured to be turned on, and the discharge transistor (M2) is configured to be turned off to thereby cause current to flow through the precharge transistor (Ml) to the capacitive device (CI) to thereby charge the capacitive device (CI). Responsive to the input signal having a second polarity, the precharge and discharge transistors (Ml, M2) are configured to change state to thereby cause charge from the capacitive device (CI) to discharge through the resistor (Rl) and through the discharge transistor (M2). The voltage on the node (105) decays to a level which

WO 2018/187263 A1

[Continued on next page]

HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

A RESISTOR-CAPACITOR (RC) DELAY CIRCUIT WITH A PRECHARGE MODE

BACKGROUND

[0001] Delay circuits are used in wide variety of applications. Responsive to receipt of an input signal, a delay circuit generates an output signal after a predefined period of time. However, the time delay implemented by a given delay circuit may vary over process, voltage and temperature (PVT). Accordingly, to a degree, the length of the time delay may depend on the supply voltage, on the temperature in which the circuit is operating, and on the semiconductor processing used to manufacture the circuit.

SUMMARY

[0002] In at least one example, a delay circuit may include a precharge transistor configured to be coupled to a supply voltage rail and configured to receive an input signal. The delay circuit also may include a resistor, a discharge transistor, a capacitive device, and an inverter. The resistor may be coupled to the precharge transistor to thereby form a node. The resistor may have a negative temperature coefficient. The discharge transistor may be coupled to the resistor and configured to receive the input signal. The capacitive device and the inverter may be coupled to the node. The inverter may be configured to produce an output signal. Responsive to the input signal having a first polarity, the precharge transistor is turned ON, and the discharge transistor is turned OFF to thereby cause current to flow from the supply voltage rail and through the precharge transistor to the capacitive device to thereby charge the capacitive device. Responsive to the input signal having a second polarity, the precharge transistor may be turned OFF, and the discharge transistor may be turned ON to thereby cause charge from the capacitive device to discharge through the resistor and through the discharge transistor.

[0003] In another example, a circuit may include a precharge transistor configured to be coupled to a supply voltage rail and configured to receive an input signal. A resistor may be coupled to the precharge transistor to thereby form a node. A discharge transistor may be coupled to the resistor and configured to receive the input signal. A capacitive device may be coupled to the node. Responsive to the input signal having a first polarity, the precharge transistor may be turned ON, and the discharge transistor may be turned OFF to thereby cause current to flow from the supply

voltage rail and through the precharge transistor to the capacitive device to thereby charge the capacitive device. Further, responsive to the input signal having a second polarity, the precharge transistor may be turned OFF, and the discharge transistor turned ON to thereby cause charge from the capacitive device to discharge through the resistor and through the discharge transistor.

[0004] In yet another example, a delay circuit may include a precharge transistor, a discharge transistor, a resistor, a capacitive device, and an inverter. The precharge transistor may be configured to be coupled to a supply voltage rail and to receive an input signal. The resistor may be coupled to the precharge transistor to thereby form a node. The resistor may have a negative temperature coefficient. The discharge transistor may be coupled to the resistor and configured to receive the input signal. The capacitive device may be coupled to the node. The inverter may be coupled to the node and configured to produce an output signal. A first reset switch also may be included and coupled to the node and configured to receive a reset signal. The precharge transistor may comprise one of a p-channel device or an n-channel device, and the discharge transistor may comprise the other of the p-channel device or the n-channel device.

[0005] In another example, a method may include configuring a delay circuit for a precharge mode of operation in which a capacitive device is charged, thereby forcing a charge node within the delay circuit to be at a logic high level. The method also may include detecting a change in a logic level of an input signal. Responsive to the detected change in the logic level of the input signal, the method may include reconfiguring the delay circuit for a discharge mode of operation in which charge from the capacitive device is discharged through a resistor to a common voltage rail to thereby cause a voltage on the charge node to decrease. Further, responsive to a voltage level of the voltage on the charge node becoming a logic low level, the method may include changing an output signal from a first logic state to a second logic state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 shows a delay circuit in accordance with various examples.

[0007] FIG. 2 shows the operation of the delay circuit in a precharge mode in accordance with various examples.

[0008] FIG. 3A shows the operation of the delay circuit in a discharge mode in accordance with various examples.

[0009] FIG. 3B shows a timing diagram of the delay circuit during the discharge mode of operation in accordance with various examples.

[0010] FIG. 4 shows the operation of the delay circuit in a reset mode in accordance with various examples.

[0011] FIG. 5 shows a method embodiment in accordance with various examples.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0012] A delay circuit is described herein whose time delay has less variation with PVT than other delay circuits. In one example, the delay circuit may include a precharge switch, a discharge switch, a resistor, a capacitive device, and an inverter. One or more additional switches may provide a reset function for the delay circuit. The delay circuit is configured to receive an input signal (e.g., an input signal that transitions from a logic low to a logic high, that is a rising edge), and the output of the inverter replicates the rising edge but following a time delay largely controlled by the component values of the resistor and the capacitive device.

[0013] The precharge switch may be coupled to a supply voltage rail and may be configured to receive the input signal. The resistor couples between the precharge switch and the discharge switch to form an internal node of the delay circuit. In some embodiments, the resistor has a negative temperature coefficient (i.e., its resistance varies inversely with temperature). The discharge switch is also configured to receive the input signal. The precharge switch may comprise a p-channel device, and the discharge switch may comprise an n-channel device, which means that because they receive the same input signal to their gates, the precharge and discharge switches are not both on at the same time (i.e., while one is on, the other is off, and vice versa). Also, the capacitive device and the inverter are coupled to the node.

[0014] During an inactive state of the input signal (e.g., the input signal being at a logic low level and before an active generation of a rising edge), the precharge switch (also termed a precharge transistor) is on, and the discharge switch (also termed a discharge transistor) is off, which thereby causes current to flow from the supply voltage rail and through the precharge switch to the capacitive device to charge the capacitive device. The voltage on the node is thus high. Responsive to the input signal transitioning to a logic high level, the precharge switch turns off, and the discharge switch turns on to cause charge from the capacitive device to discharge through the resistor and the discharge switch to ground. Thus, as the input signal transitions from low to high, the node voltage (i.e., the voltage on the capacitive device) transitions from high (resulting from its precharge state) to low at a rate controlled by the product of the resistance value (R) of the resistor and the capacitance (C) of the capacitive device. The inverter then inverts the node's high

to low transition back to the same polarity as the input signal's low to high transition.

[0015] FIG.1 shows an example of a delay circuit 100 in accordance with various embodiments. The illustrative delay circuit 100 includes transistors M1, M2, M3, M4, M5, and M6, a resistor R1, and a capacitive element C1. The transistors M5 and M6 form an inverter 120. In this example, transistors M1, M3, and M5 are implemented as p-channel devices, and transistors M2, M4 and M6 are implemented as n-channel devices. In other embodiments, the transistors can be implemented as other than the specific channel type devices illustrated in FIG. 1. The voltage node V_{DD} in FIG. 1 may comprise a positive supply voltage rail, and V_{SS} may comprise a common voltage rail (e.g., ground).

[0016] The capacitive device C1 may be implemented as a p-channel transistor as shown, an n-channel transistor, or a capacitor. In the configuration shown, the capacitive device is a p-channel transistor whose source and drain terminals are connected together to form a capacitor. The source and drain terminals are connected to V_{SS}.

[0017] Transistor M1 functions as a precharge transistor to charge capacitive device C1 (and thus is designated in FIG. 1 as a precharge (PRE) transistor) and couples between V_{DD} and a terminal of resistor R1. The opposing resistor terminal is coupled to transistor M2, which functions to discharge the capacitive device C1 (and thus is designated in FIG. 1 as a discharge (DISCH) transistor). The gates of M1 and M2 are connected together in this example and are configured to receive an input signal as shown.

[0018] The illustrative delay circuit 100 also includes a reset capability that is implemented by transistors M3 and M4. The circuit is caused to be reset responsive to a RESET signal provided to the gates of M3 and M4 being low. Resetting the circuit may cause the output signal to transition back to the inactive state (e.g., low). When not actively resetting the circuit, RESET is high. Discharge transistor M2 is coupled to reset transistor M4, which also couples to V_{SS}. The other reset transistor M3 couples between VDD and the capacitive device C1. The node interconnecting M1, M3, R1 and C1 is labeled as 105 in FIG. 1.

[0019] The example delay circuit of FIG. 1 also includes an inverter 120. In this example, the inverter 120 comprises a pair of transistors including transistors M5 and M6. Transistor M5 may comprise a p-channel device, and transistor M6 may comprise an n-channel device. The gates of M5 and M6 are connected together and connected to node 105. Further, the drains of M5 and M6 are connected together to provide an output signal from the delay circuit 100. The inclusion of

inverter 120 causes the delay circuit 100 to function as a non-inverting delay circuit in which the output voltage tracks the input voltage, albeit with a time delay as described herein.

[0020] In operation, an edge of the input signal (e.g., a rising edge) is replicated as the output signal, but after a time delay that is largely caused by the RC time constant implemented by the resistor R1 and capacitive device C1. The delay circuit 100 can be implemented with a variety of time delays through selection of various combinations of resistance R and capacitance C values for resistor R1 and capacitive device C1, respectively. In some embodiments, the resistor R1 has a negative temperature coefficient, which means its resistance R varies inversely with temperature—increases in temperature results in lower R, and vice versa. The negative temperature coefficient for R1 helps to reduce the variation in the delay circuit's time delay with temperature. Accordingly, because other components in the time delay circuit 100 may exhibit a positive correlation with temperature (e.g., switching speeds of the transistors may decrease with increases in temperature, the capacitance C of capacitive device C1 may be positively correlated with temperature, etc.), to a certain extent selection of R1 to have a negative correlation with temperature counteracts the temperature effects of the other components. In some embodiments, the temperature coefficient of R1 may be a value that is equal to or more negative than -50 parts per million (ppm) per degree Celsius. In one example, the negative temperature coefficient of R1 is -234 ppm/C. The capacitive device C1 may have a large size relative to the smallest feature size of the semiconductor process. Accordingly, process variation of the time delay generated by the circuit will be reduced. Using a resistor and a capacitive device (RC) for the delay removes the large variation that a transistor-based time delay would provide. In some examples, the variation of the time delay across PVT may be approximately 1.5:1.

[0021] In operation, the illustrative delay circuit 100 may be capable of multiple modes of operations, such as a precharge mode in which the capacitive device C1 is charged, a discharge mode in which the charge on the capacitive device discharges through the resistor, and a reset mode. These modes of operation are illustrated in FIGS. 2, 3A, 3B and 4, respectively. The transistors in FIGS. 2, 3A, 3B and 4 are depicted conceptually by switch symbols, and the inverter 120 also is shown by an inverter symbol. Further, the capacitive device C1 is shown by a capacitor symbol.

[0022] FIG. 2 illustrates the precharge mode of operation of the delay circuit. The delay circuit is configured for this mode responsive to the input signal being in an inactive state and awaiting an

edge. In the example described herein, the inactive state for the input signal is a logic low (0). The input signal being low causes the precharge transistor M1 to be ON and the discharge transistor M2 to be OFF. Further, the RESET signal for this mode of operation is set a logic high level (1), which results in reset transistors M3 being OFF and M4 being ON. Thus, in the precharge mode, the input signal is low, and the reset signal is high which causes M1 and M4 to be ON and M2 and M3 to be OFF, as shown in FIG. 2.

[0023] In the precharge mode, current from the positive power rail V_{DD} flows through the precharge transistor M1 to the capacitive device C1 as depicted by arrow 150. The capacitive device C1 thus charges, and the voltage on node 105 becomes a positive voltage level and is detected by inverter 120 as a logic high. The inverter 120 inverts the logic high on node 105 to a logic low for the output signal. While the delay circuit remains in the precharge mode (while the input signal is low), the node 105 has a positive voltage (high signal level), and the capacitive device C1 is charged.

[0024] Referring to FIG. 3A, the input signal then may transition from low to high. The input signal being high causes the precharge transistor M1 to be OFF and the discharge transistor M2 to be ON. The RESET signal remains at a logic high level, causing M3 and M4 to remain OFF and ON respectively. The charge current path from V_{DD} to the capacitor is disrupted due to M1 being OFF, but a discharge current path 160 is created from the capacitive device C1 through the resistor R1 to VSS (illustrated in FIG. 3 as a ground potential). The rate at which the capacitor discharges is dictated by the product of R and C.

[0025] The waveforms 161, 162, and 163 in FIG. 3B further illustrate the operation of the delay circuit. Waveform 161 represents the input signal and illustrates the input signal transitioning from a logic low to a logic high at time T1. Waveform 162 represents the voltage on node 105. Up until T1, the node 105 voltage is a logic high. The node 105 voltage begins to decay toward a logic low level when the input signal becomes high and creates the discharge current path 160. The voltage on node 105 decays at a rate dictated by the product of R and C. Waveform 163 represents the voltage of the output signal. The delay circuit 100 is a non-inverting delay circuit, so the output voltage is low while the input voltage is low. The output signal remains at a logic low level despite the input signal becoming high. The voltage on node 105, which is provided as input to the inverter 120, begins to drop as shown. When the node 105 voltage falls to a low enough level to be interpreted as a logic low by the inverter 120, the output of the inverter (i.e., the output signal of

the delay circuit 100) transitions from low to high as shown at time T2. The difference between T2 and T1 is shown in FIG. 3B as DLY and is controlled by the value of RC.

[0026] The output signal will remain at a logic high level as long as the input signal is a logic high level. In some cases, it may be desired to reset the delay circuit to thereby force the output signal to again become a logic low level despite the input signal being at logic high level. FIG. 4 shows the operation of the delay circuit during a reset mode of operation. To reset the output signal, the RESET signal is forced to a logic low level, which causes reset transistor M3 to be ON and reset transistor M4 to be OFF as shown. With M3 being ON, a charge current path 170 forms to provide charge current from the positive supply rail V_{DD} through transistor M3 to the capacitive device C1. As the capacitive device C1 begins to charge, the voltage on node 105 begins to increase to the point at which the inverter 120 detects the node 105 voltage to be at a logic high level. The inverter 120 then inverts the high node 105 voltage, thereby forcing the output signal to be a logic low signal.

[0027] In some implementations, multiple delay circuits 100 may be serially cascaded together, with the output signal from one delay circuit provided as the input signal to the next delay circuit in sequence. As the time delays implemented by each delay circuit aggregate, it causes a larger delay between: the input signal to the first delay circuit in the serial chain; and the output signal from the last delay circuit in the chain.

[0028] FIG. 5 shows a flow chart illustrating a method in accordance with various embodiments. The operations may be performed in the order shown, or in a different order. Further, the operations may be performed sequentially, or two or more of the operations may be performed concurrently.

[0029] At 200, the method may include configuring the delay circuit for the precharge mode of operation. For example, this operation may be implemented by turning various transistor switches ON and OFF based on the logic state of the input signal. In the example described hereinabove, transistors M1 and M4 are turned ON, and transistors M2 and M3 are turned OFF. As a result, current flows to the capacitive device, and the voltage on node 105 (reference in FIG. 5 as charge node) becomes high.

[0030] At 202, the method may include detecting a change in the input signal voltage level from a logic low to a logic high (or vice versa in other embodiments of the delay circuit). Responsive to that detection being made, the delay circuit is reconfigured at 204 for the discharge mode of

operation. While in the discharge mode of operation, the capacitive device begins to discharge, and the voltage on the charge mode begins to drop.

[0031] At 206, the method may include determining when the charge node becomes a logic low level. After a time delay period of time, the charge node voltage will be determined to be a logic low level. As a result, at 208, the method may comprise changing the output signal voltage level from its former state to an opposing polarity (e.g., from logic low to logic high).

[0032] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A delay circuit, comprising:

a precharge transistor coupled to a supply voltage rail and configured to receive an input signal;

a resistor coupled to the precharge transistor to thereby form a node, wherein the resistor has a negative temperature coefficient;

a discharge transistor coupled to the resistor and configured to receive the input signal;

a capacitive device coupled to the node; and

an inverter coupled to the node and configured to produce an output signal;

wherein, responsive to the input signal having a first polarity, the precharge transistor is configured to be turned on and the discharge transistor is configured to be turned off to thereby cause current to flow from the supply voltage rail and through the precharge transistor to the capacitive device to thereby charge the capacitive device; and

wherein, responsive to the input signal having a second polarity, the precharge transistor is configured to be turned off and the discharge transistor is configured to be turned on to thereby cause charge from the capacitive device to discharge through the resistor and through the discharge transistor.

2. The delay circuit of claim 1, wherein the capacitive device comprises a transistor.

3. The delay circuit of claim 1, further comprising:

a first reset switch coupled to the node and to the supply voltage rail, wherein the first reset switch is configured to be controlled by a reset signal; and

a second reset switch coupled to the discharge switch and to a common voltage rail, wherein the second reset switch is configured to be controlled by the reset signal;

wherein the first reset switch is turned on with the reset signal at a first polarity and the second reset switch is turned on with the reset signal at a second polarity; and

wherein, when the first reset switch is turned on by the reset signal, current is caused to flow from the power supply rail through the first reset switch and to the capacitive device to thereby increase the voltage on the node and cause the output signal from the inverter to change logic state.

4. The delay circuit of claim 1, wherein the negative temperature coefficient of the resistor is equal to, or more negative than, –50 parts per million per unit of temperature.

5. The delay circuit of claim 1, wherein the precharge transistor comprises a p-channel metal oxide semiconductor field effect transistor (MOSFET), and the discharge transistor comprises an n-channel MOSFET.

6. A circuit, comprising:

a precharge transistor configured to be coupled to a supply voltage rail and configured to receive an input signal;

a resistor coupled to the precharge transistor to thereby form a node;

a discharge transistor coupled to the resistor and configured to receive the input signal; and

a capacitive device coupled to the node;

wherein, responsive to the input signal having a first polarity, the precharge transistor is configured to be turned on and the discharge transistor is configured to be turned off to thereby cause current to flow from the supply voltage rail and through the precharge switch to the capacitive device to thereby charge the capacitive device; and

wherein, responsive to the input signal having a second polarity, the precharge transistor is configured to be turned off and the discharge transistor is configured to be turned on to thereby cause charge from the capacitive device to discharge through the resistor and through the discharge switch.

7. The circuit of claim 6, wherein the resistor has a negative temperature coefficient.

8. The circuit of claim 6, further comprising an inverter coupled to the node and configured to produce an output signal that is asserted after a time delay from assertion of the input signal.

9. The circuit of claim 6, wherein the capacitive device comprises a transistor.

10. The circuit of claim 6, further comprising:

a first reset switch coupled to the node and to the supply voltage rail, wherein the first reset switch is configured to be controlled by a reset signal; and

a second reset switch coupled to the discharge transistor and to a common voltage rail, wherein the second reset switch is configured to be controlled by the reset signal;

wherein the first reset switch is turned on with the reset signal at a first polarity and the second reset switch is turned on with the reset signal at a second polarity; and

wherein, when the first reset switch is turned on by the reset signal, current is caused to flow from the power supply rail through the first reset switch and to the capacitive device to thereby increase the voltage on the node.

11. A delay circuit, comprising:

a precharge transistor coupled to a supply voltage rail and configured to receive an input signal;

a resistor coupled to the precharge transistor to thereby form a node, wherein the resistor has a negative temperature coefficient;

a discharge transistor coupled to the resistor and configured to receive the input signal;

a capacitive device coupled to the node;

an inverter coupled to the node and configured to produce an output signal; and

a first reset switch coupled to the node and configured to receive a reset signal;

wherein the precharge transistor is one of a p-channel device or an n-channel device and the discharge transistor is the other of the p-channel device or the n-channel device.

12. The delay circuit of claim 11, wherein:

responsive to the input signal having a first polarity, the precharge transistor is configured to be turned on and the discharge transistor is configured to be turned off to thereby cause current to flow from the supply voltage rail and through the precharge switch to the capacitive device to thereby charge the capacitive device; and

responsive to the input signal having a second polarity, the precharge transistor is configured to be turned off and the discharge transistor is configured to be turned on to thereby cause charge from the capacitive device to discharge through the resistor and through the discharge switch.

13. The delay circuit of claim 12, wherein the capacitive device comprises a transistor.

14. The delay circuit of claim 12, further comprising:

a second reset switch coupled to the discharge switch and to a common voltage rail, wherein the second reset switch is configured to be controlled by the reset signal;

wherein the first reset switch is turned on with the reset signal at a first polarity and the second reset switch is turned on with the reset signal at a second polarity; and

wherein, when the first reset switch is turned on by the reset signal, current is caused to flow from the power supply rail through the first reset switch and to the capacitive device to

thereby increase the voltage on the node and cause the output signal from the inverter to change logic state.

15. The delay circuit of claim 12, wherein the negative temperature coefficient of the resistor is equal to, or more negative than, –50 parts per million per unit of temperature.

16. A method, comprising:

configuring a delay circuit for a precharge mode of operation in which a capacitive device is charged thereby forcing a charge node within the delay circuit to be at a logic high level;

detecting a change in a logic level of an input signal;

responsive to the detected change in the logic level of the input signal, reconfiguring the delay circuit for a discharge mode of operation in which charge from the capacitive device is discharged through a resistor to a common voltage rail to thereby cause a voltage on the charge node to decrease; and

responsive to a voltage level of the voltage on the charge node becoming a logic low level, changing an output signal from a first logic state to a second logic state.

17. The method of claim 16, further comprising resetting the delay circuit through operation of a reset transistor coupled to charge the node to thereby force the logic state of the output signal back to the first logic state.

18. The method of claim 16, wherein configuring the delay circuit for the precharge mode comprises:

turning on a precharge transistor coupled between a positive supply voltage rail and the resistor; and

turning off a discharge transistor coupled between the resistor and the common voltage rail.

19. The method of claim 18, wherein reconfiguring the delay circuit for the discharge mode of operation comprises turning off the precharge transistor and turning on the discharge transistor.

20. The method of claim 16, wherein:

detecting the change in the logic level of the input signal comprises detecting a change in the input signal from a logic low to a logic high; and

changing the output signal from a first logic state to a second logic state comprises changing the output signal from a logic low to a logic high.

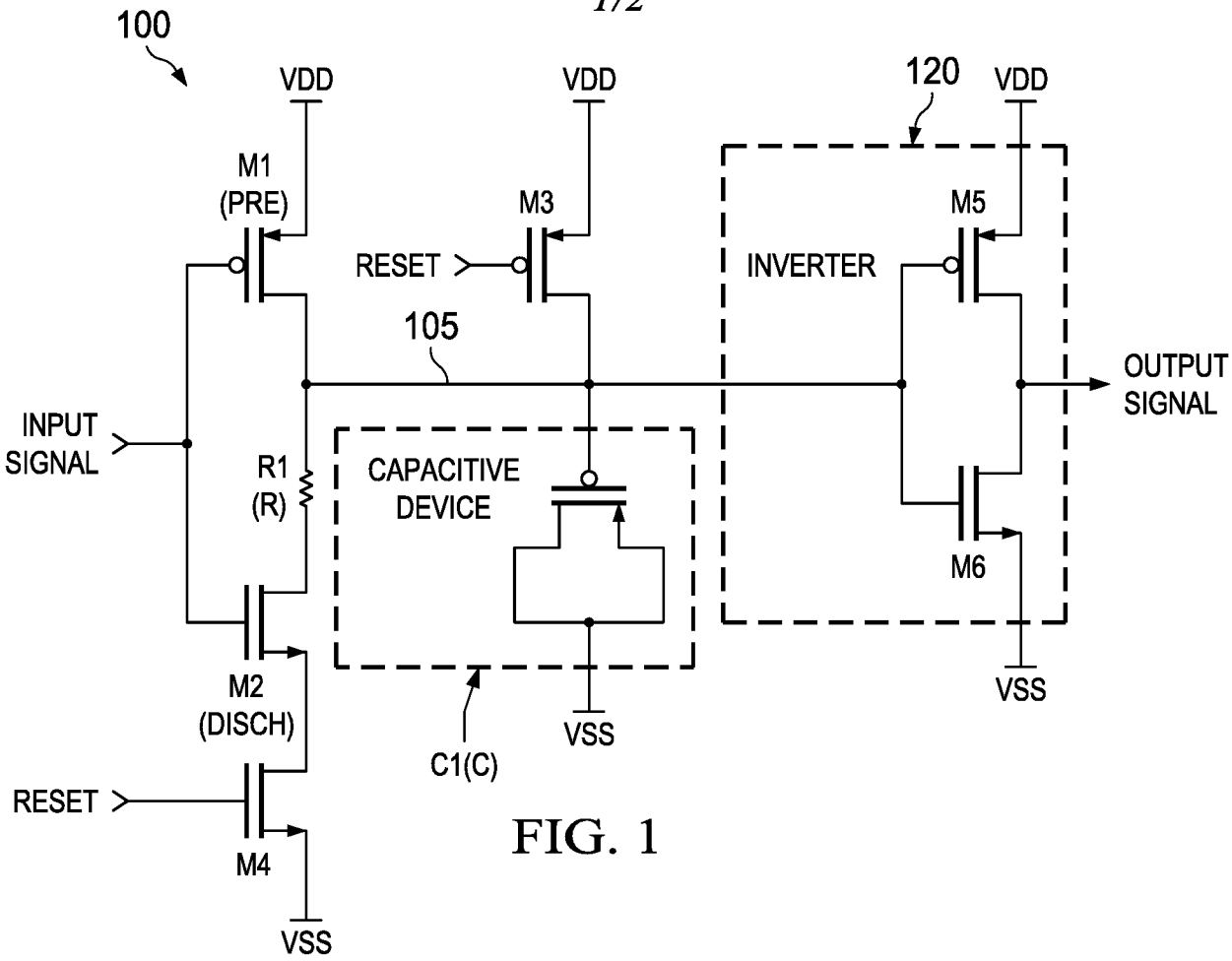
100
VDD
VDD
120
VDD
M1
(PRE)
M3
M5
RESET
INVERTER
105
OUTPUT
SIGNAL
INPUT
SIGNAL
R1
(R)
CAPACITIVE
DEVICE
M6
M2
(DISCH)
VSS
C1(C)
VSS
RESET
M4
VSS

FIG. 1

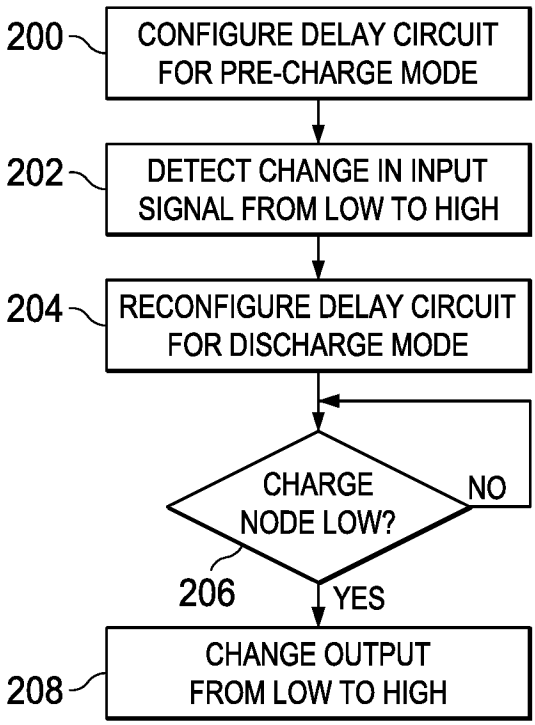
200
CONFIGURE DELAY CIRCUIT FOR PRE-CHARGE MODE
202
DETECT CHANGE IN INPUT SIGNAL FROM LOW TO HIGH
204
RECONFIGURE DELAY CIRCUIT FOR DISCHARGE MODE
CHARGE NODE LOW?
NO
206
YES
208
CHANGE OUTPUT FROM LOW TO HIGH

FIG. 5

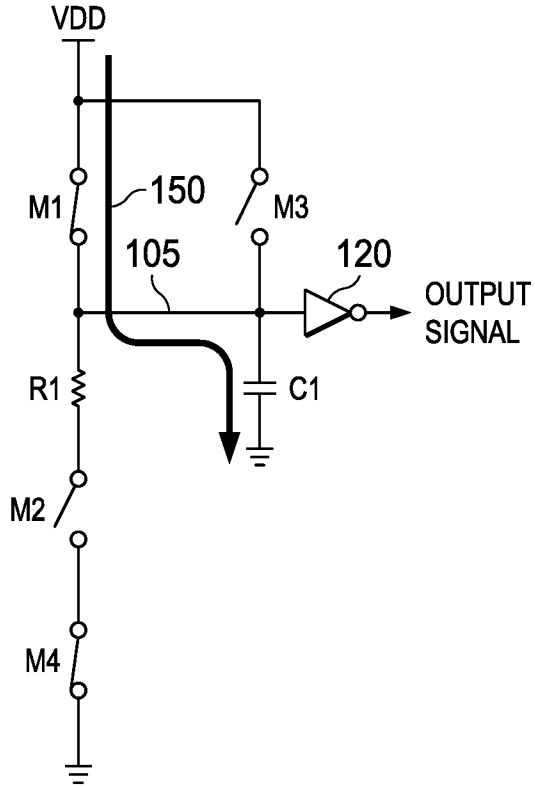

FIG. 2

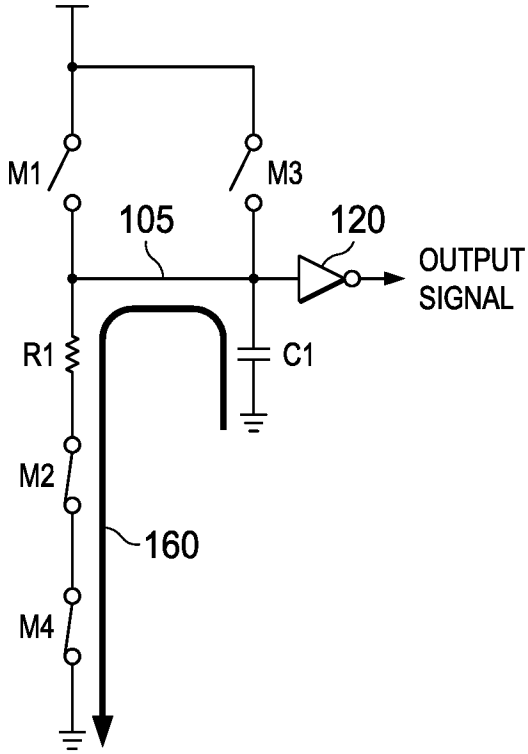

FIG. 3A

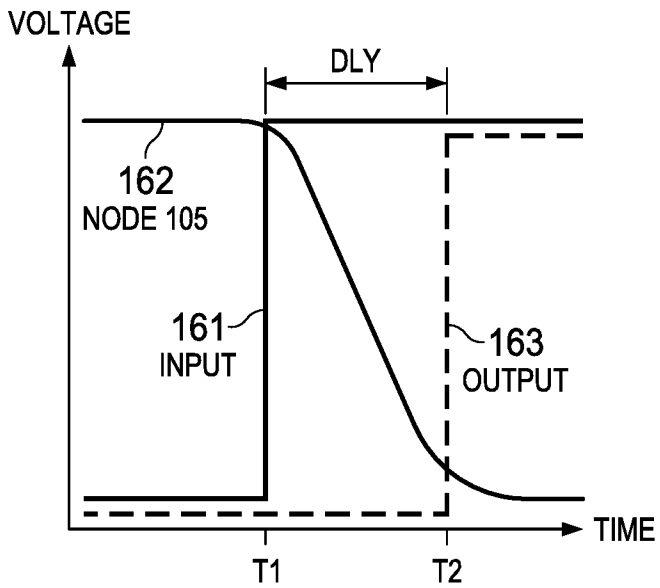

FIG. 3B

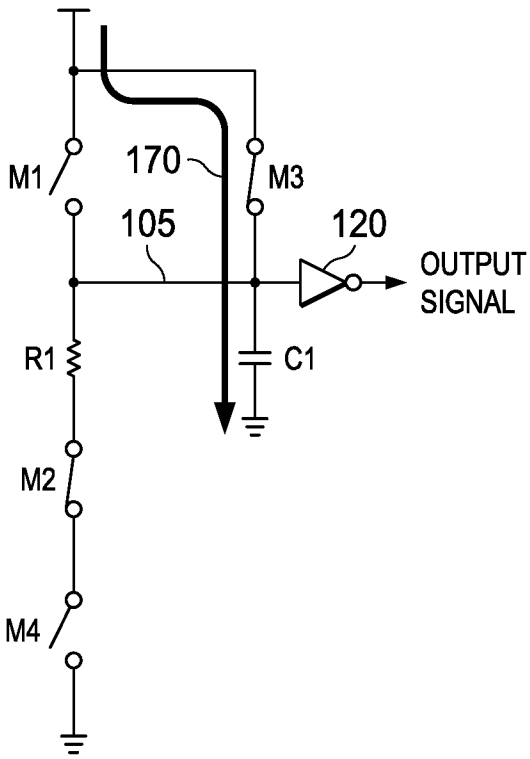

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2018/025794

A. CLASSIFICATION OF SUBJECT MATTER

H03H 11/26 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4797580 A (NORTHERN TELECOM LIMITED) 10.01.1989, col.1, lines 33-41, col.2, lines 20-27, line 43-col.3, line 59, col.4, lines 1-8, line 45-col.5, line 47, col.5, lines 65-67, col.6, lines 24-30,	1, 4-8, 11, 12, 15-20
Y		2, 9, 13
A		3, 10, 14
Y	US 2014/0184299 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY) 03.07.2014, abstract	2, 9, 13
A	US 2011/0279128 A1 (DIALOG SEMICONDUCTOR GMBH) 17.11.2011	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 July 2018 (26.07.2018)	09 August 2018 (09.08.2018)

Name and mailing address of the ISA/RU:
Federal Institute of Industrial Property,
Berezhkovskaya nab., 30-1, Moscow, G-59,
GSP-3, Russia, 125993
Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37

Authorized officer

V. Aleksandrov

Telephone No. (499) 240-25-91