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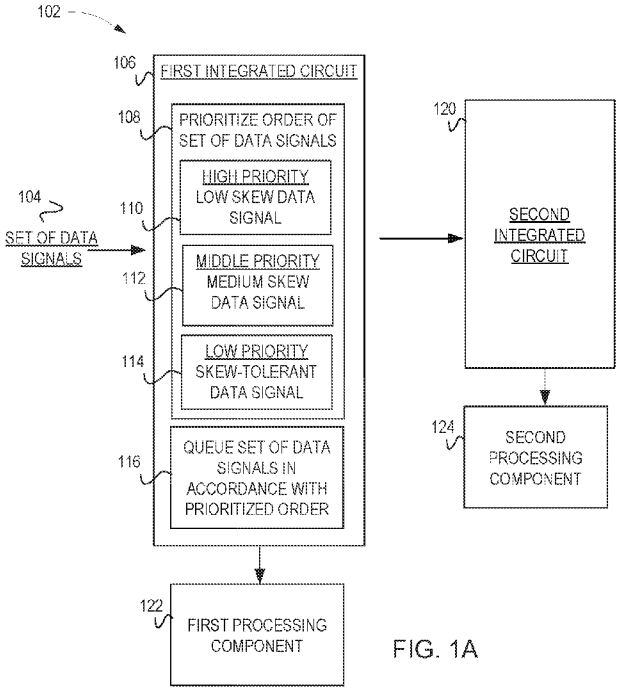

FIG. 1A

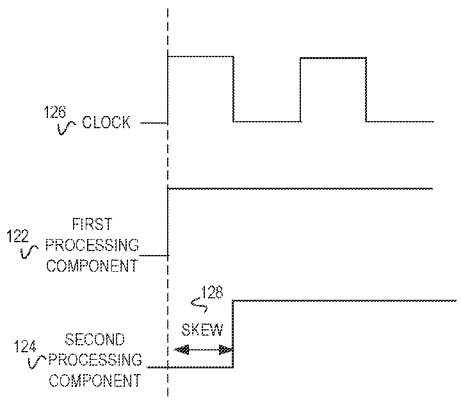

FIG. 1B

(57) Abstract: Examples herein disclose an identification of a set of skew requirements corresponding to a set of data signals. Based on the set of skew requirements, the examples prioritize an order of transmission for the set of data signals. The example queue the set of data signals in accordance with the prioritized order.

[Continued on next page]

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PRIORITIZATION FOR A SET OF DATA SIGNALS BASED ON SKEW REQUIREMENTS

BACKGROUND

[0001] In transmission of data signals, there may be several design considerations to satisfy skew requirements. Data signal skew is a time difference between two different components asserting a data signal. The assertion of data signal is a time it takes for a data signal to go from low to high or vice versa at each component. Each data signal may have a different skew tolerance requirement. For example, some data signals can tolerate trace amounts of skew while other data signals may tolerate a large amount of skew, such as many microseconds.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] In the accompanying drawings, like numerals refer to like components or blocks. The following detailed description references the drawings, wherein:

[0003] FIG. 1A illustrates an example system including a first integrated circuit to prioritize an order of a data signal set for transmission to a second integrated circuit in accordance with the present disclosure;

[0004] FIG. 1B illustrates an example clock signal and corresponding skew for a data signal;

[0005] FIG. 2 illustrates an example bridge system including connections between first integrated circuit and second integrated circuit in accordance with the present disclosure;

[0006] FIG. 3 is a flowchart of an example method to prioritize an order of a set of data signals based on a set of skew requirements in accordance with the present disclosure;

[0007] FIG. 4 is a flowchart of an example method to prioritize an order of a set of data signals for transmission based on a set of skew requirements in accordance with the present disclosure;

[0008] FIG. 5 is a block diagram of an example computing device with a processing resource to execute instructions in a machine-readable storage medium for queuing a set of data signals based on a prioritized order in accordance with the present disclosure; and

[0009] FIG. 6 is a block diagram of an example computing device with a processing resource to execute instructions in a machine-readable storage medium for transmitting a set of data signals based on a prioritized order of the data signal set in accordance with the present disclosure.

DETAILED DESCRIPTION

[0010] To comply with these skew tolerance rates, there are several approaches. In one approach, a connector pin may be wired directly in a point-to-point configuration so that each data signal is immediately transmitted; however the point-to-point configuration increases both board space and connectors. In another approach, data signals may be moved from one location to another over a shift register chain; however this approach may result in unacceptable amounts of skew. For example, as a number of data signals increase, so does the skew in the shift register approach. As such, the size and performance of systems may be limited by signal skew.

[0011] The present disclosure provides a mechanism to reduce an amount of board space and connector pin count while also efficiently managing skew requirements of the data signals. The disclosure is implemented on an integrated circuit to identify a level of skew (e.g., low, medium and skew-tolerant) for each data signal. In turn based on the level of skew in the set of skew requirements, the disclosure prioritizes an order for transmission of the data signals. Based on the prioritized order, the data signal set is queued for transmission. By prioritizing the traffic (e.g., data signals), this allows the data signals corresponding to low skew levels to be transferred ahead of skew-tolerant (high skew) data signals.

[0012] Additionally, separating low skew data signals from medium skew and high skew (e.g, skew-tolerant) data signals allows deterministic timing on the low skew data signals since there are fewer potentially queued messages ahead of these signals. This allows a single bus to be shared from one integrated circuit to another integrated circuit for the signal transmission. Using the single bus reduces an amount of board space and the number of connectors used to transmit the data signals.

[0013] In another example, a type of the data signal may define the level of skew. In this example, some types of data signals are correlated with lower skew rates, while other types of data signals may be correlated with higher skew rates. For example, a data signal related to an interrupt and/or reset may be associated with a lower skew level. The lower skew level may be based on asserting these data signals close in time at the components for synchronization purposes.

[0014] In a further example, the disclosure provides a bridge system including a first integrated circuit and second integrated circuit. Each integrated circuit may transmit data signals with a respective processor for synchronization. Thus each circuit may prioritize the data signal set based

on the level of skew. The bridge system provides a synchronization of data signals using a serial interface to prioritize which traffic may be transferred ahead of other traffic.

[0015] The following detailed description refers to the accompanied figures. Wherever possible, the same reference numbers are used in the figures and the following description to refer to the same or similar parts. It is to be expressly understood, however, that the figures are for the purpose of illustration and description only. While several examples are described throughout, modification, adaptions, and other implementations are possible. Accordingly, the following detailed description is not meant to limit the disclosed examples, rather it is meant to provide proper scope of the disclosed examples and may be defined by the appended claims.

[0016] FIG. 1 is a block diagram of an example system 102 including first integrated circuit 106 and second integrated circuit 120. First integrated circuit 106 receives data signal set 104 and prioritizes an order of data signal set 104 at module 108. At module 108, first integrated circuit 106 identifies a set of skew requirements including various skew requirements 110-114. The set of skew requirements include the various classes of skew a data signal may tolerate. These classes include low skew data signal 110, medium skew data signal 112, and skew-tolerant data signal 114. Based on the classes of the various skew requirements 110-114, first integrated circuit 106 prioritizes the data signal set 104. Based on prioritizing an order for transmission of the data signal set 104 at module 108, first integrated circuit 106 proceeds to queue data signal set 104 for transmission. The data signal set 104 may be transmitted to first processing component 122 for assertion of the data signal and to second integrated circuit 120 for assertion at second processing component 124. Asserting the data signal at both processing components 122 and 124 allows system 102 to synchronize. As such, system 102 as illustrated in FIG. 1 represents a data network in which integrated circuits 106 and 120 operate in conjunction to represent a single overall system. For example, first integrated circuit 106 may operate in one server, while second integrated circuit 120 operates in a different server, thus system 102 illustrates the overall single system with both of these servers operating in conjunction. As such implementations of system 102 include, by way of example, a database server, mail server, file server, domain name system (DNS) server, print server, web server, game server, application server, cartridge server, blade server, catalog server, communication server, home server, media server, proxy server, or other type of computing device(s) capable of operating in conjunction with one another to present an overall single system.

[0017] Set of data signals 104, also referred to as data signal set herein, are signals relaying information to receiving entities. The data signal set 104 relay types of functions in which to synchronize between integrated circuits 106 and 120 and/or processing components 122 and 124. For example, a data signal may include a system reset, thus to get both processing components 122 and 124 to reset within an acceptable skew range, this data signal should be synchronized between components 122 and 124. This ensures both components 122 and 124 are reacting within a tolerable time period. Data signal set 104 represents various data signals which may each include a skew class (e.g., low skew, medium skew, skew-tolerant, etc.) from the set of skew requirements. In one implementation, the format of each data signal include a 16 bit signal format. In this example, bits 0-7 include payload information while bits 8-15 include other identifying information. In this implementation, one of the bits (bits 8-15) may be modified to represent the class of skew (e.g., low skew data signal, skew-tolerant data signal, etc.). Another bit may be used to set a parity bit. In this example, the parity bit is set for the receiving entity (e.g., second integrated circuit 120) to use the parity bit to check whether the transmitted data signal includes an error.

[0018] First integrated circuit 106 is hardware component part of system 102 that prioritizes the order of data signal set 104 based on the set of skew requirements 110-114. First integrated circuit 106 is an electronic circuit formed on semiconductor material to provide electrical connections using conductive tracks, pins, pads, or other features between circuits 106 and 120 and/or processing components 122 and 124. As such implementation of first integrated circuit 106 include, by way of example, a central processing unit (CPU), processor, semiconductor, processing resource, controller, microcontroller, field programmable gate array (FPGA), or other type of hardware component capable of the functionality of first integrated circuit 106.

[0019] Module 108 prioritizes the order for transmitting data signal set 104 based on the set of skew requirement classes (e.g., low, medium, tolerant). Module 108 prioritizes the order of transmission for data signal set 104 such that the prioritization provides a serialization in which to transmit each of the data signals to second integrated circuit 120. In this manner, each data signal in set 104 is prioritized to identify a sequential order of when to transmit to second integrated circuit 120. In this implementation, those data signals which are identified as the class of low skew data signals 110 are given the highest priority and transmitted before other classes 112 and 114. The

medium skew data signals 112 are given middle priority and transmitted on the same bus as low skew data signals 110, but are transmitted after low skew data signals 110 and prior to skew-tolerant data signals 114. The skew-tolerant data signals 114 are given the lowest priority and are the last class of data signals to be transmitted on the same bus as the other skew classes 110-112. The skew class (e.g., low, medium, tolerant) is based on a type of each data signal. For example, data signals related to fault management are considered low-skew data signals and these should be prioritized for initial transmission. Data signals related to power management may be considered skew-tolerant data signals as it takes several milliseconds for second integrated circuit 120 to react to receiving these signals, thus these data signals are in lowest priority for transmission. Module 108 may include, by way of example, instructions (e.g., stored on a machine-readable medium) that, when executed (e.g., by integrated circuit 106 and/or 120), implement the functionality of module 108. Alternatively, or in addition, module 108 may include electronic circuitry (i.e., hardware) that implements the functionality of module 108.

[0020] Set of skew requirements 110-114 represent the various classes or levels of skew corresponding to a given data signal in set 104. In one implementation, the class of skew may be dependent on the type of data signal. This information may be pre-defined by a developer to classify which class of skews should correspond to which type of data signal. For example, those signals which may be highest priority and lowest skew may be related to fault issues, interrupts, etc. Those signals which may be lowest in priority and higher skew (e.g., skew-tolerant) may be related to power management, etc.

[0021] Low skew data signals 110 are given the highest priority as these signals represent those data signals which may tolerate a small amount of skew. To provide context, the skew in this class of data signals may be less than a few nanoseconds (e.g., 2 ns). Low skew data signals 110 may also be referred to as "fast signals" as these signals should transmitted in the highest priority. In a further implementation, low skew data signals 110 also tolerate a lower amount of latency. Latency is the transmission time for the data signal to leave first integrated circuit 106 and arrive at second integrated circuit 120.

[0022] Medium skew data signals 112 are those signals which may tolerate a little more skew than low skew data signals, but less skew than skew-tolerant data signals. To provide context, the skew in this class of data signals is less than a few microseconds (e.g., 2 us). Medium skew data

signals may also be referred to as "fast-sync signals" as these signals should be asserted from integrated circuits 106 and/or 120 for assertion at respective processing component 122 and 124. The fast-sync signals, unlike fast signals, may tolerate a higher amount of latency and should be asserted at the same clock rising edge. For example, fast-sync signals may be related to a reset function and as such, for these signals to be synchronized simultaneously, these signals have be transmitted from integrated circuits 106 and 120 at the same rising clock edge to ensure synchronization at processing components 122 and 124. In other words, by transmitting fast-sync signal at the same clock edge ensures each data signal is asserted at each processing component 122 and 124 at the same time.

[0023] Skew-tolerant data signals 114 are given lowest priority as these signals represent those signals which can tolerate a larger amount of skew than low skew data signals 110 and medium skew data signals 112. Synchronization of these signals at each integrated circuit 106 and 120 and processing components 122 and 124 are less consequential. To provide context, the larger amount of skew may include several microseconds (e.g., 50 us). Skew-tolerant data signals 112 may also be referred to as "slow signals" as the transmission of these signals are lowest in priority. In a further implementation skew-tolerant data signals 114, unlike low skew data signals 110, tolerate a larger amount of latency.

[0024] Module 116 queues the data signal set 104 in accordance with the prioritized order. Those data signals given the highest priority are transmitted initially, followed by middle priority, and then lowest priority. As such, first integrated circuit 106 may additionally include a memory component (not illustrated) which module 116 places or queues the prioritized data signals for transmission. Module 116 may include, by way of example, instructions (e.g., stored on a machine-readable medium) that, when executed (e.g., by first integrated circuit 106), implements the functionality of module 116. Alternatively, or in addition, module 116 may include electronic circuitry (i.e., hardware) that implements the functionality of module 116.

[0025] Second integrated circuit 120 may receive the prioritized data signal set from first integrated circuit 106. Second integrated circuit 120 is an electronic circuit formed on semiconductor material to provide electrical connections using conductive tracks, pins, pads, or other features between circuits 106 and 120 and/or processing components 122 and 124. As explained earlier, second integrated circuit 120 operates in conjunction with first integrated circuit

106 to provide a serial interface for traffic prioritization to synchronize particular data signals at respective processing component 122 and 124. In this example, integrated circuits 106 and 120 operate in conjunction to synchronize functionalities by transmitting data signals to each respective processing component 122 and 124. For example, second integrated circuit 120 may also include additional functionality (not illustrated) capable of prioritizing data signals based on skew requirements to first integrated circuit 106 and second processing component 124. In this example, each integrated circuit 106 and 120 operates independently of each other to send the prioritized set of data signals 104 to the other integrated circuit 106 and 120. Each integrated circuit 106 and 120 may proceed to send transmitted data signals to each respective processing component 122 and 124.

[0026] FIG. 1B illustrates an example clock signal 126 and skew 128 between first processing component 122 and second processing component 124. In this example, the assertion from first processing component 122 is closely synced to the clock 126 rising edge. The assertion from second processing component 124 is further from the clock 126 rising edge. Thus, skew 128 is the time difference between the assertions at first processing component 122 and second processing component 124. The assertion is considered the time it takes for a data signal at the respective processing component 122 and 124 to change state, such as low to high and vice versa. For example, the assertion is the time at each processing component 122 and 124 to go from low to high based on the transmitted data signal. In this example, the assertion for the first processing component 122 occurs prior to the assertion at second processing component 124. Although FIG. 1B illustrates assertion occurring at first processing component 122 prior to assertion at second processing component 124, this was done for illustration purposes as second processing component 124 may assert prior to first processing component 122.

[0027] FIG. 2 illustrates an example bridge system showing connections between first field programmable array (FPGA 1) 206 and second field programmable (FPGA 2) 220. The FPGAs 206 and 220 represent a type of integrated circuit in accordance with the present disclosure. As illustrated with the electrical connections, each FPGA 206 and 220 supports full duplex capabilities. In the full duplex system, each FPGA 206 and 220 can communicate with each other simultaneously. Thus by providing the full duplex system, data signals can be prioritized by FPGA 206 and transmitted to FPGA 220 while data signals can be prioritized by FPGA 220 and transmitted to FPGA 206. In this example, both FPGAs 206 and 220 include the circuitry and/or functionality in which to implement

the prioritization of traffic based on a level of skew. Additionally, each FPGA 206 and 220 are positioned in a different server (Server 1 and Server 2). Server link 232 couples together FPGAS 206 and 220 such that the servers operate together to provide one overall server system. To provide the overall system, clock 230 may be used to provide a timing mechanism for transmitting low skew data signals (e.g., fast signals) and medium skew data signals (e.g., fast-synch signals).

[0028] Clock 230 may include a synchronization clock and is coupled between FPGAs 206 and 220. Clock 230 provides the timing mechanism for each FPGA to transmit the fast data signals and fast-synch data signals. In this example, based on a rising edge from clock 230, FPGA 206 and 220 may push out these data signals. Waiting for the rising edge from clock 230 ensures the fast data signals and fast-sync data signals may be synchronized. In a further example each FPGA 206 and 220 is connected to a respective processing component (not illustrated). In this example, upon clock 230 reaching the rising edge, each FPGA 206 and 220 transmits the data signal to each processing component for synchronizing the transmitted data signal between both processing components.

[0029] Serial bus 236, coupled between both FPGAs 206 and 220, provides the transmission medium for transmitting the prioritized data signals from FPGA 206 to FPGA 220. In turn, FPGA 220 may prioritize another data signal set and transmit the prioritized data signals to FPGA 206 over serial bus 234. Using the serial bus 234 and 236 to transmit the prioritized data signal set from FPGA 206 and FPGA 220 reduces the number of connections and board space within each respective server.

[0030] Pullup resistors 228, coupled to each serial bus 234 and 236, enables each FPGA 206 and 220 to see a rising edge for asserting the data signal to each respective processing component (not illustrated) at the same time. For example, pullup resister 228 coupled to serial bus 234 pulls up the data signal from FPGA 220 to FPGA 206. The other pullup resister 228 coupled to serial bus 236 pulls up the data signal from FPGA 206 to FPGA 220. In this manner, pullup resistors 228 are used to synchronize the prioritized data signal set between FPGAs 206 and 220 and/or processing components.

[0031] Further, although FIG. 2 illustrates eight connections (e.g., pins, solder traces, joints, etc) between each FPGA 206 and 220, implementations are not intended to be so limited as FPGAs 206 and 220 may include fewer connections to implement prioritized data signal set in the bridge

system. As such, based on the example illustrated in FIG. 2, the electrical connections are provided as follows: The SBRIDGE_DIN electrical connection may provide serial data input; SBRIDGE_SCLK_IN may include the serial clock input from clock 230 to transmit low skew and medium skew data signals on the rising clock edge; SBRIDGE_CLS_L_IN may include the chip select input so when low, data signals may be transmitted and may be latched; SBRIDGE_DOUT may include the serial data output; SBRIDGE_CLK_OUT may include the serial clock output; and SBRIDGE_CS_L_OUT may include the chip select output so when low, data signals may be transmitted and latched accordingly.

[0032] Referring now to FIGS. 3 and 4, example flowcharts are illustrated in accordance with various examples of the present disclosure. The flowcharts represent processes that may be utilized in conjunction with various systems and devices as discussed with reference to the preceding figures. While illustrated in a particular order, the flowcharts are not intended to be so limited. Rather, it is expressly contemplated that various processes may occur in different orders and/or simultaneously with other processes than those illustrated.

[0033] FIG. 3 is a flowchart of an example method, executable by an integrated circuit, to prioritize an order of a set of data signals based on a set of identified skew requirements. The integrated circuit receives the set of data signals and proceeds to identify a set of skew requirements corresponding to the data signal set. The set of skew requirements include low skew data signals, medium skew data signals, and/or skew-tolerant data signals. Based on identifying the set of skew requirements corresponding to the data signal set, the integrated circuit prioritizes an order of the data signal set for transmission. Upon prioritizing the order of the data signal set, the integrated circuit queues the data signal set for transmission. In discussing FIG. 3, references may be made to the components in FIGS. 1-2 to provide contextual examples. In one implementation, first integrated circuit 106 works in conjunction with second integrated circuit 120 as in FIG. 1 to execute operations 302-306 to prioritize the order of data signals based on the skew requirements. Further, although FIG. 3 is described as implemented by an integrated circuit, it may be executed on other suitable components. For example, FIG. 3 may be implemented in the form of executable instructions on a machine-readable storage medium 504 and 604 as in FIGS. 5-6. In other implementations, the illustrated flowchart may be executed by a computing device.

[0034] At operation 302, the integrated circuit identifies the set of skew requirements corresponding to the set of data signals. The data signals represent various functionalities to perform on different integrated circuits. The set of skew requirements correspond to the set of data signals and as such may represent the various classes or levels of skew. For example, the levels of skew may include low skew data signals, medium skew data signals, and skew tolerant data signals (e.g., high skew data signals). In one implementation the type of data signal determines the level of skew. Upon identifying the set of skew requirements, the integrated circuit may proceed to prioritize the data signals.

[0035] At operation 304 based on the identified set of skew requirements, the integrated circuit proceeds to prioritize the data signal set in accordance to the skew requirements. In one implementation, the data signal set is prioritized based on the level of skew. The level of skew indicates which data signals should be synchronized across integrated circuits and/or processing components. For example, the low skew data signals may be prioritized highest followed by the medium skew data signals and skew tolerant data signals. Based on obtaining the prioritized data signal set, the integrated circuit may proceed to queue the data signals.

[0036] At operation 306, the integrated circuit queues the set of data signals in accordance with the prioritized order. The prioritized order specifies the sequence in which to transmit each data signal in the data signal set across a serial bus to another integrated circuit. The integrated circuit may place the prioritized data signal set in a memory component corresponding to the transmission order. Thus the highest prioritized data signals are placed closer to the serial bus than the lowest prioritized signals. Upon queuing the prioritized data signal set, the integrated circuit may proceed transmission of the data signals.

[0037] FIG. 4 is a flowchart of an example method, executable by an integrated circuit, to prioritize an order of data signal set for transmission based on a set of skew requirements. The integrated circuit identifies the set of skew requirements corresponding to the data signal set. Upon identifying the set of skew requirements, a bit in each data signal may be modified to represent the identified skew requirement. Additionally, the integrated circuit may proceed to set a parity bit in each data signal prior transmission for an error check by a receiving entity. Based on identifying the skew requirements, the integrated circuit prioritizes an order of the data signal set for transmission. Upon prioritizing the order of the data signal set, the integrated circuit queues the data signal set. In

a further implementation, upon receiving a different data signal set, the integrated circuit proceeds to identify the skew requirements for the different data signal set. The integrated circuit proceeds to queue the low skew data signals in the different data signal set in higher priority for transmission prior to the previously queued skew-tolerant data signals in the data signal set. In discussing FIG. 4, references may be made to the components in FIGS. 1-2 to provide contextual examples. In one implementation, first integrated circuit 106 works in conjunction with second integrated circuit 120 as in FIG. 1 to execute operations 402-418 to prioritize the order of data signals based on the skew requirements. Further, although FIG. 4 is described as implemented by a computing device, it may be executed on other suitable components. For example, FIG. 4 may be implemented in the form of executable instructions on a machine-readable storage medium 504 and 604 as in FIGS. 5-6. In other implementations, the illustrated flowchart may be executed by a computing device.

[0038] At operation 402, the integrated circuit receives the data signal set and proceeds to identify the skew requirements corresponding to the data signals. Operation 402 may be similar in functionality to operation 302 as in FIG. 3.

[0039] At operation 406 based on the skew requirements corresponding to the data signal set, a bit in each data signal may be modified to represent the specific skew requirement. As explained in connection with FIG. 1, each data signal may include 16 bits of information. As such, one of the bits may be modified by to represent which level of skew is tolerated by the given data signal. For example, each class of skew may be represented by a different numbered bit, such as bit nos. 10-13. Modifying the bit to high may indicate to the receiving entity what level of skew is associated with each data signal.

[0040] At operation 408, the integrated circuit may set the parity bit in each data signal in the set of data signals prior to transmission. Although FIG. 4 illustrates setting the parity bit and modifying the representative bit as occurring sequentially, implementations should not be so limited. For example, the parity bit may be set and the bit modification may occur at any operation prior to transmission.

[0041] At operation 410 based on the identification of the set of skew requirements corresponding to each data signal, the integrated circuit proceeds to prioritize the order of data signal set for transmission. In one implementation, the level of skew corresponding to the data

signals indicates to the integrated circuit when to queue and transmit the data signal. Operation 410 may be similar in functionality to operation 304 as in FIG. 3.

[0042] At operation 412, the integrated circuit queues the set of data signals in accordance with prioritized order. Base on queueing the set of data signals, the integrated circuit may proceed to transmit data signals from highest priority to lowest priority to another integrated circuit. In another implementation, the data signals may be transmitted on a serial bus from the integrated circuit. In this implementation, the integrated circuit transmits the data signal set in sequential manner on the serial bus such that data signals highest in priority are transmitted prior to the lowest priority signals. Operation 412 may be similar to operation 306 as in FIG. 3.

[0043] At operation 414, the integrated circuit may receive a different set of data signals. The different set of data signals may include signals corresponding to the various levels of skew. As such, based on receiving the different set of data signals, the integrated circuit may proceed to identify the corresponding set of skew requirements.

[0044] At operation 416, the integrated circuit proceeds to identify the set of skew requirements which correspond to the different set of data signals. Operation 416 maybe similar in functionality to operation 302 and operation 402.

[0045] At operation 418 based on the identified set of skew requirements corresponding to the different set of data signals, the integrated circuit queues the different set of data signal. In this implementation, the queued order of the initial data set is merged with the queuing of the different data signal set. As such, those data signals in the different data set which are highest prioritized (e.g., low skew data signals and/or medium skew data signals) are transmitted than any pending queued skew-tolerant signals. This enables the integrated circuit to continuously receive data signals, while ensuring those data signals corresponding to low skew and medium skew are transmitted prior to any previously queued skew-tolerant signals.

[0046] Referring now to FIGS. 5 and 6, machine-readable instructions are illustrated in accordance with various examples of the present disclosure. While illustrated in a particular order, the machine-readable instructions are not intended to be so limited. Rather, it is expressly contemplated that various machine-readable instructions may occur in different orders and/or simultaneously with other machine-readable instructions.

[0047] FIG. 5 is a block diagram of computing device 500 with a processing resource 502 to execute instructions 506-510 within a machine-readable storage medium 504. Specifically, the computing device 500 with the processing resource 502 is to classify a set of data signals according to a set of skew requirements. Upon the classification of the set of data signals, the processing resource 502 may proceed to prioritize an order for the transmission of the data signals. Although the computing device 500 includes processing resource 502 and machine-readable storage medium 504, it may also include other components that would be suitable to one skilled in the art. For example, the computing device 500 may include first integrated circuit 106 as in FIG. 1. In other examples, the computing device 500 may include a controller, memory storage, or other suitable type of component. The computing device 500 is an electronic device with the processing resource 502 capable of executing instructions 506-510 and as such embodiments of the computing device 500 include a networking device, networking switch, switch, router, computing device, server, or other type of networking component capable of executing instructions 506-510. The instructions 506-510 may be implemented as methods, functions, operations, and other processes implemented as machine-readable instructions stored on the storage medium 504, which may be non-transitory, such as hardware storage devices (e.g., random access memory (RAM), read only memory (ROM), erasable programmable ROM, electrically erasable ROM, hard drives, and flash memory).

[0048] The processing resource 502 may fetch, decode, and execute instructions 506-510 to queue the set of data signals in accordance with the prioritized order. Specifically, the processing resource 502 executes instructions 506-510 to: classify the set of data signals according to the set of skew requirements; upon classification of the set of data signals, prioritize the order of the data signals such that a lower skew data signal ranks higher in priority than a skew-tolerant data signal; and based on the prioritized order, queue the set of data signals for transmission.

[0049] The machine-readable storage medium 504 includes instructions 506-510 for the processing resource 502 to fetch, decode, and execute. In another embodiment, the machine-readable storage medium 504 may be an electronic, magnetic, optical, memory, storage, flash-drive, or other physical device that contains or stores executable instructions. Thus, the machine-readable storage medium 504 may include, for example, Random Access Memory (RAM), an Electrically Erasable Programmable Read-Only Memory (EEPROM), a storage drive, a memory cache, network storage, a Compact Disc Read Only Memory (CDROM) and the like. As such, the machine-readable storage

medium 504 may include an application and/or firmware which can be utilized independently and/or in conjunction with the processing resource 502 to fetch, decode, and/or execute instructions of the machine-readable storage medium 504. The application and/or firmware may be stored on the machine-readable storage medium 504 and/or stored on another location of the computing device 500.

[0050] FIG. 6 is a block diagram of computing device 600 with a processing resource 602 to execute instructions 606-622 within a machine-readable storage medium 604. Specifically, the computing device 600 with the processing resource 602 is to prioritize an order for transmission of a set of data signals. The prioritized order prioritizes low skew data signals over medium skew data signals and skew tolerant data signals. Upon obtaining the prioritized order, the processing resource 602 may proceed to queue and transmit the set of data signals. Although the computing device 600 includes processing resource 602 and machine-readable storage medium 604, it may also include other components that would be suitable to one skilled in the art. For example, the computing device 600 may include first integrated circuit 106 as in FIG. 1. In other examples, the computing device 600 may include a controller, memory storage, or other suitable type of component. The computing device 600 is an electronic device with the processing resource 602 capable of executing instructions 606-622 and as such embodiments of the computing device 600 include a networking device, networking switch, switch, router, computing device, server, or other type of networking component capable of executing instructions 606-622. The instructions 606-622 may be implemented as methods, functions, operations, and other processes implemented as machine-readable instructions stored on the storage medium 604, which may be non-transitory, such as hardware storage devices (e.g., random access memory (RAM), read only memory (ROM), erasable programmable ROM, electrically erasable ROM, hard drives, and flash memory).

[0051] The processing resource 602 may fetch, decode, and execute instructions 606-622 to queue and transmit the set of data signals in accordance with the prioritized order. Specifically, the processing resource 602 executes instructions 606-622 to: identify the specific skew requirement for each data signal in the data signal set including whether the specific skew requirement includes the low skew data signal, medium skew data signal, and/or skew-tolerant data signal; modify a bit in each data signal in the set, the bit modification represents the specific skew requirement; set a parity bit in each data signal prior to transmission, the parity bit may be used by the receiving entity to check for

any errors in the transmission of each data signal; prioritize the order of the set of data signals based on the specific skew requirements such that low skew data signal ranks highest in priority, medium priority for the low skew data signal with high latency, and lowest priority for the skew-tolerant high latency data signals; queue the data signal set in accordance with the prioritized order, the higher ranking or highest prioritized data signals are placed higher in order for transmission; transmit the data signals based on the prioritized order, the higher ranking data signals are transmitted prior to transmission of the medium skew data signals and the skew-tolerant data signals; classify a different set of data signals according to the various skew requirements corresponding to each data signal; and queue the low skew data signals in the different set of data signals in higher priority for transmission prior to the skew-tolerant data signals in the initial set of data signals.

[0052] The machine-readable storage medium 604 includes instructions 606-622 for the processing resource 602 to fetch, decode, and execute. In another embodiment, the machine-readable storage medium 604 may be an electronic, magnetic, optical, memory, storage, flash-drive, or other physical device that contains or stores executable instructions. Thus, the machine-readable storage medium 604 may include, for example, Random Access Memory (RAM), an Electrically Erasable Programmable Read-Only Memory (EEPROM), a storage drive, a memory cache, network storage, a Compact Disc Read Only Memory (CDROM) and the like. As such, the machine-readable storage medium 604 may include an application and/or firmware which can be utilized independently and/or in conjunction with the processing resource 602 to fetch, decode, and/or execute instructions of the machine-readable storage medium 604. The application and/or firmware may be stored on the machine-readable storage medium 604 and/or stored on another location of the computing device 600.

[0053] Although certain implementations have been illustrated and described herein, it will be appreciated that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the implementations shown and described without departing from the scope of this disclosure. Those with skill in the art will readily appreciate that implementations may be implemented in a variety of ways. This application is intended to cover adaptions or variations of the implementations discussed herein. Therefore, it is manifestly intended that implementations be limited only by the claims and equivalents thereof.

CLAIMS

We claim:

1. A method executable by an integrated circuit, the method comprising:

identifying a set of skew requirements corresponding to a set of data signals;

based on the set of skew requirements, prioritizing an order of transmission for the set of data signals; and

queueing the set of data signals in accordance with the prioritized order.

2. The method of claim 1, wherein a data signal corresponding to a lower skew requirement is a higher ordered priority than a skew-tolerant data signal.

3. The method of claim 1, comprising:

transmitting the set of data signals in a serial manner based on the prioritized order.

4. The method of claim 1, comprising:

modifying a bit in the set of data signals corresponding to the set of skew requirements; and

setting a parity bit in the set of data signals prior to transmission.

5. The method of claim 1, comprising:

receiving a different set of data signals;

identifying the set of skew requirements corresponding to the different set of data signals, wherein the set of skew requirements includes a lower skew requirement; and

queuing the different set of data signals in a higher priority than previously queued skew-tolerant signals.

6. The method of claim 1, wherein identifying the set of skew requirements corresponding to the set of data signals comprises:

classifying each data signal in the set of data signals according to the set of skew requirements.

7. A system comprising:

a first integrated circuit to:

prioritize an order to a set of data signals based on a set of skew requirements corresponding to the set of data signals such that a lower skew data signal in the set of data signals is higher in priority than a skew-tolerant data signal;

queue the set of data signals in accordance with the prioritized order; and

a second integrated circuit to receive the set of data signals based on prioritized order.

8. The system of claim 7, comprising:

a synchronization clock, coupled between the first integrated circuit and the second integrated circuit, to provide a timing mechanism for transmission of the lower skew data signal; and

wherein the first integrated circuit transmits the set of data signals based on a rising edge from the synchronization clock.

9. The system of claim 7, comprising:

a serial bus, coupled between the first integrated circuit and the second integrated circuit, to transmit the set of data signals in a serial manner according to the prioritized order.

10. The system of claim 9, comprising:

a pull-up resister, coupled to the serial bus, to synchronize the set of data signals between the first integrated circuit and the second integrated circuit.

11. The system of claim 7, wherein the first integrated circuit and the second integrated circuit are full-duplex capable circuits.

12. A non-transitory machine-readable storage medium comprising instructions that when executed by a processing resource cause a computing device to:

classify a set of data signals according to a level of skew, wherein the set of data signals

includes a low skew data signal, a medium skew data signal, and a skew-tolerant data signals;

prioritize an order of the set of data signals for transmission based on the classification of the set of data signals such that the low skew data signal are higher in priority than the medium skew data signal and the skew-tolerant data signal; and

queue the set of data signals in accordance with the prioritized order.

13. The non-transitory machine-readable storage medium of claim 12, wherein the low skew data signal is a low skew and low latency data signal, the medium skew data signal is a low skew and high latency data signal, and the skew-tolerant signal is a high skew and high latency data signal.

14. The non-transitory machine-readable storage medium of claim 12, comprising instructions that when executed by the processing resource cause the computing device to:

classify a different set of data signals according to the level of skew, wherein the different set of data signals include a second low skew data signal; and

queue the second low skew data signal at a higher priority than previously queued skew-tolerant signals in the set of data signals.

15. The non-transitory machine-readable storage medium of claim 12, comprising instructions that when executed by the processing resource cause the computing device to:

modify a bit in the set of data signals corresponding to the level of skew prior to transmission; and

set a parity bit in the set of data signals prior to transmission.

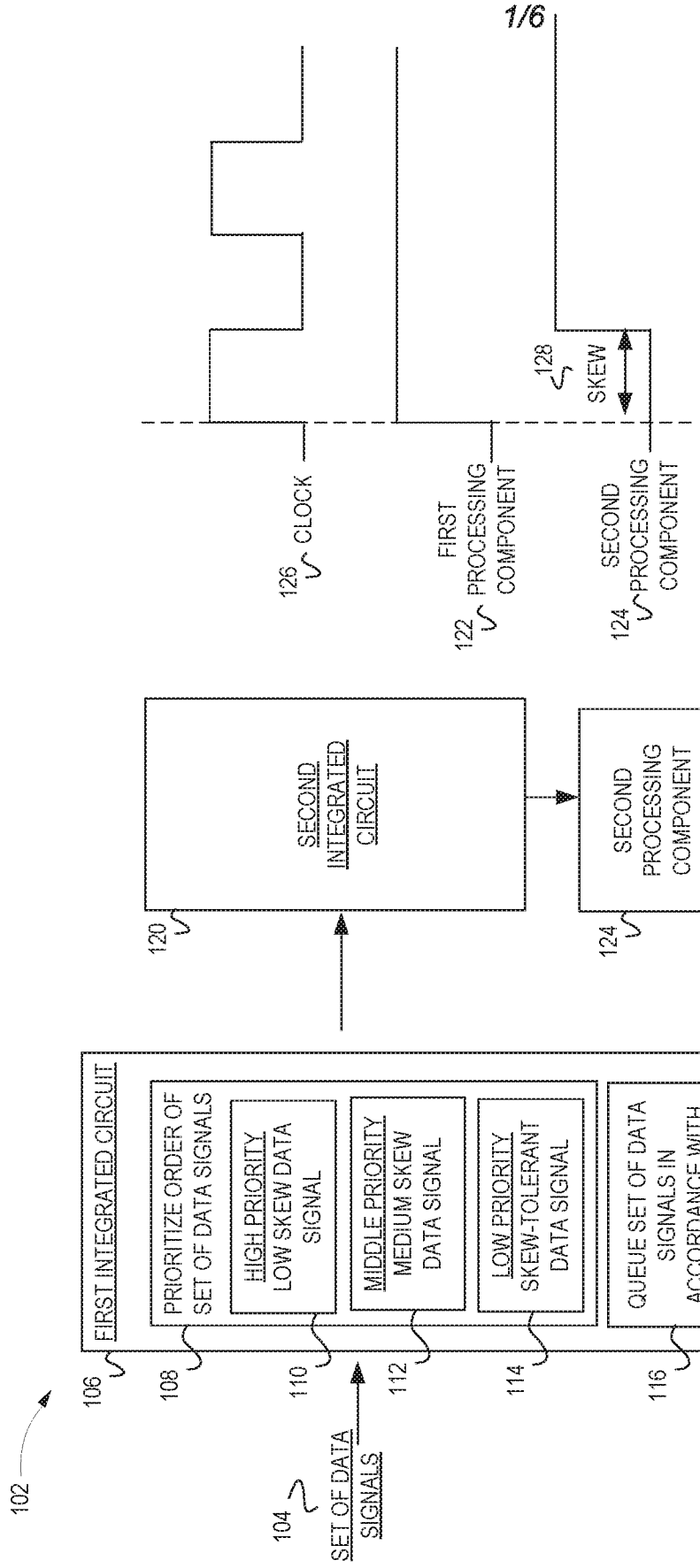

102
104
SET OF DATA SIGNALS
106
FIRST INTEGRATED CIRCUIT
108
PRIORITIZE ORDER OF SET OF DATA SIGNALS
110
HIGH PRIORITY LOW SKEW DATA SIGNAL
112
MIDDLE PRIORITY MEDIUM SKEW DATA SIGNAL
114
LOW PRIORITY SKEW-TOLERANT DATA SIGNAL
116
QUEUE SET OF DATA SIGNALS IN ACCORDANCE WITH PRIORITIZED ORDER
122
FIRST PROCESSING COMPONENT
120
SECOND INTEGRATED CIRCUIT
124
SECOND PROCESSING COMPONENT

FIG. 1A

126
CLOCK
122
FIRST PROCESSING COMPONENT
124
SECOND PROCESSING COMPONENT
128
SKEW

FIG. 1B

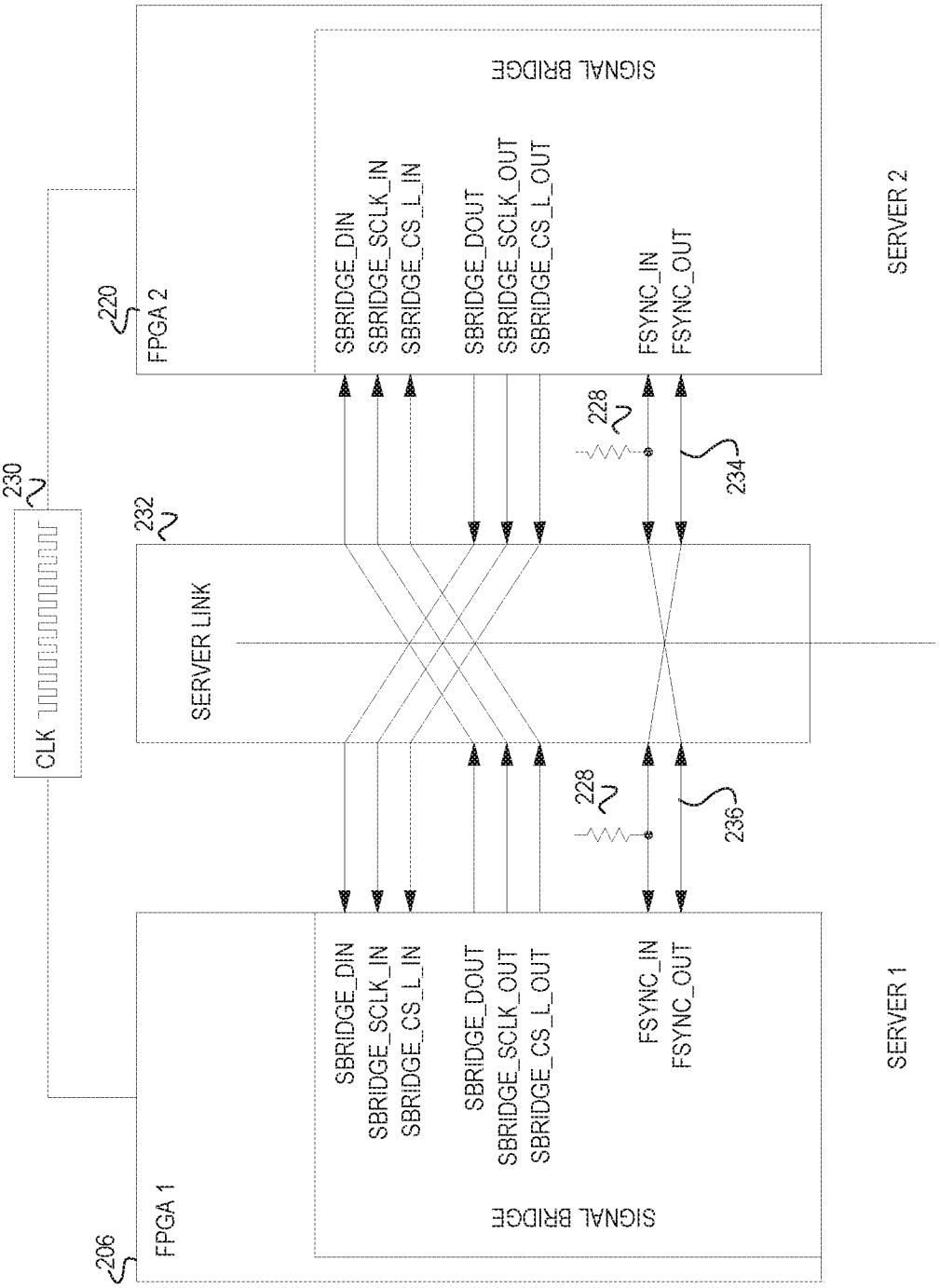

206
FPGA 1
SIGNAL BRIDGE
SBRIDGE_DIN
SBRIDGE_SCLK_IN
SBRIDGE_CS_L_IN
SBRIDGE_DOUT
SBRIDGE_SCLK_OUT
SBRIDGE_CS_L_OUT
FSYNC_IN
FSYNC_OUT
SERVER 1
220
FPGA 2
SIGNAL BRIDGE
SBRIDGE_DIN
SBRIDGE_SCLK_IN
SBRIDGE_CS_L_IN
SBRIDGE_DOUT
SBRIDGE_SCLK_OUT
SBRIDGE_CS_L_OUT
FSYNC_IN
FSYNC_OUT
SERVER 2
228
228
234
236
230
CLK
232
SERVER LINK

FIG. 2

FIG. 3

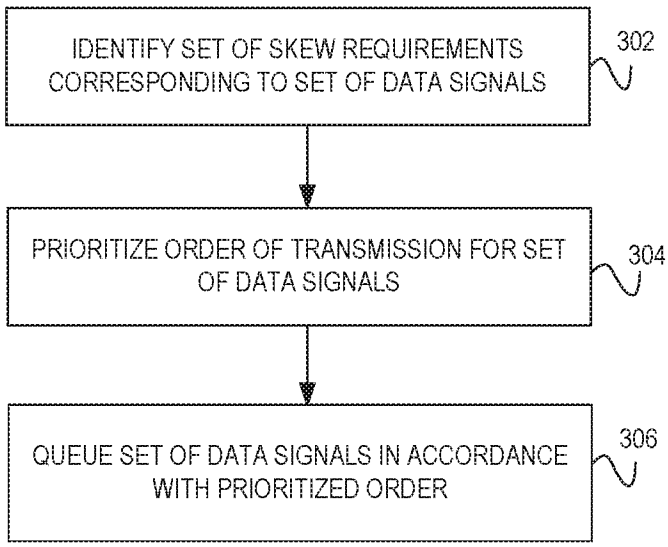

IDENTIFY SET OF SKEW REQUIREMENTS CORRESPONDING TO SET OF DATA SIGNALS
302
PRIORITIZE ORDER OF TRANSMISSION FOR SET OF DATA SIGNALS
304
QUEUE SET OF DATA SIGNALS IN ACCORDANCE WITH PRIORITIZED ORDER
306

FIG. 4

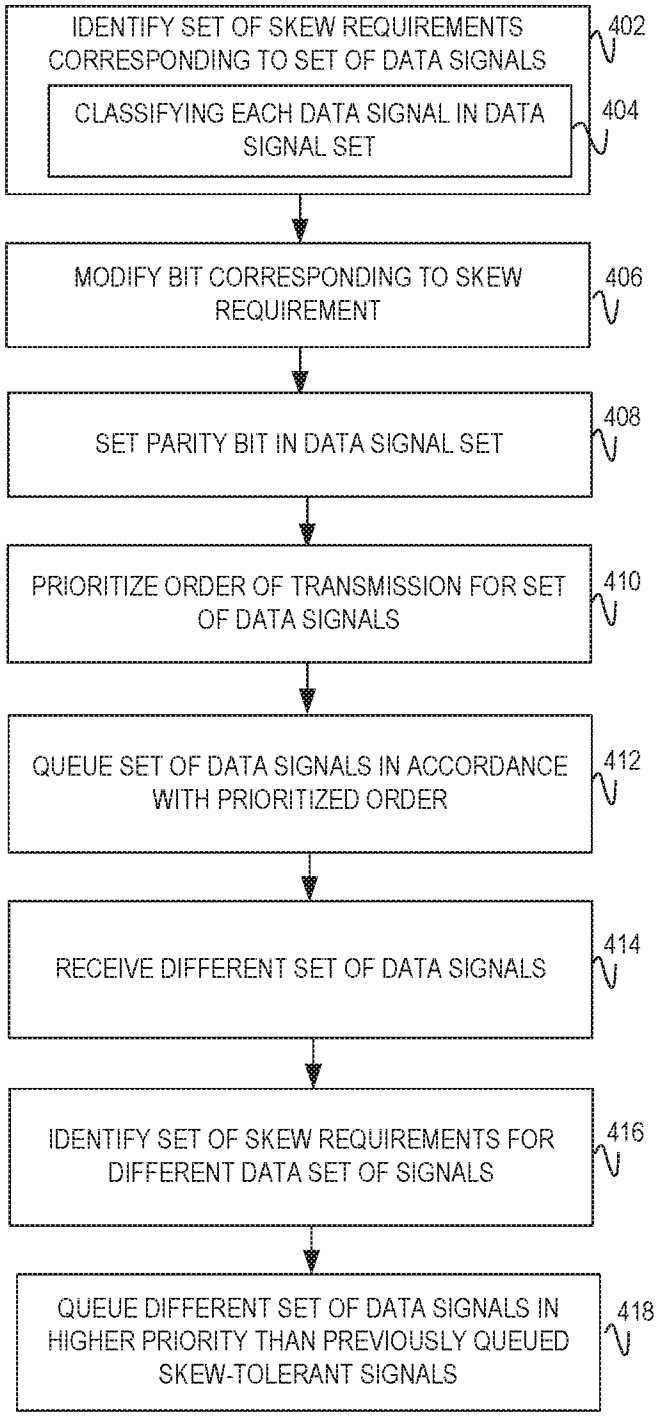

IDENTIFY SET OF SKEW REQUIREMENTS CORRESPONDING TO SET OF DATA SIGNALS
402
CLASSIFYING EACH DATA SIGNAL IN DATA SIGNAL SET
404
MODIFY BIT CORRESPONDING TO SKEW REQUIREMENT
406
SET PARITY BIT IN DATA SIGNAL SET
408
PRIORITIZE ORDER OF TRANSMISSION FOR SET OF DATA SIGNALS
410
QUEUE SET OF DATA SIGNALS IN ACCORDANCE WITH PRIORITIZED ORDER
412
RECEIVE DIFFERENT SET OF DATA SIGNALS
414
IDENTIFY SET OF SKEW REQUIREMENTS FOR DIFFERENT DATA SET OF SIGNALS
416
QUEUE DIFFERENT SET OF DATA SIGNALS IN HIGHER PRIORITY THAN PREVIOUSLY QUEUED SKEW-TOLERANT SIGNALS
418

FIG. 5

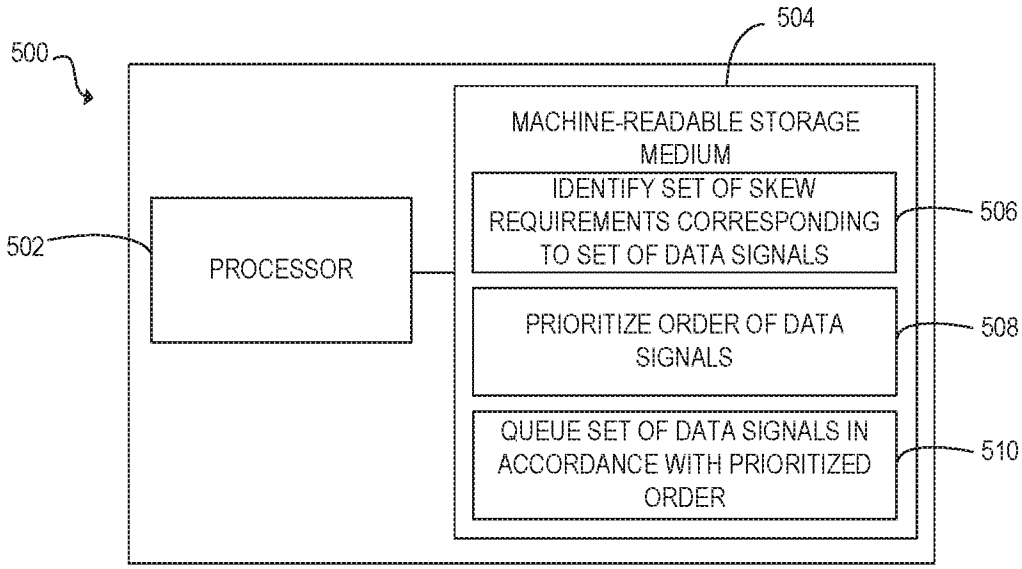
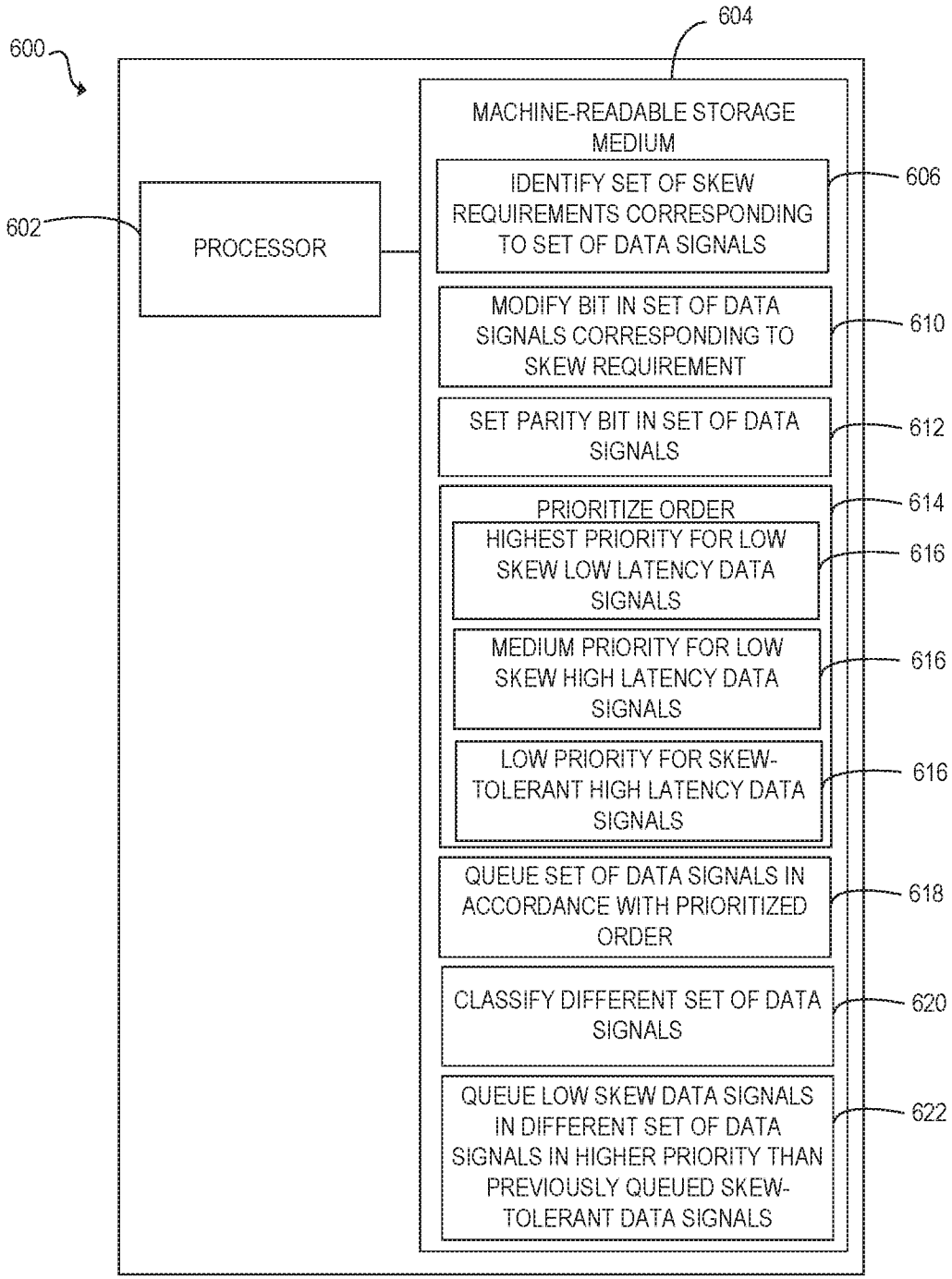

500
504
MACHINE-READABLE STORAGE MEDIUM
IDENTIFY SET OF SKEW REQUIREMENTS CORRESPONDING TO SET OF DATA SIGNALS
506
PRIORITIZE ORDER OF DATA SIGNALS
508
QUEUE SET OF DATA SIGNALS IN ACCORDANCE WITH PRIORITIZED ORDER
510
502
PROCESSOR

FIG. 6


600
602
PROCESSOR
604
MACHINE-READABLE STORAGE MEDIUM
IDENTIFY SET OF SKEW REQUIREMENTS CORRESPONDING TO SET OF DATA SIGNALS
606
MODIFY BIT IN SET OF DATA SIGNALS CORRESPONDING TO SKEW REQUIREMENT
610
SET PARITY BIT IN SET OF DATA SIGNALS
612
PRIORITIZE ORDER
614
HIGHEST PRIORITY FOR LOW SKEW LOW LATENCY DATA SIGNALS
616
MEDIUM PRIORITY FOR LOW SKEW HIGH LATENCY DATA SIGNALS
616
LOW PRIORITY FOR SKEW-TOLERANT HIGH LATENCY DATA SIGNALS
616
QUEUE SET OF DATA SIGNALS IN ACCORDANCE WITH PRIORITIZED ORDER
618
CLASSIFY DIFFERENT SET OF DATA SIGNALS
620
QUEUE LOW SKEW DATA SIGNALS IN DIFFERENT SET OF DATA SIGNALS IN HIGHER PRIORITY THAN PREVIOUSLY QUEUED SKEW-TOLERANT DATA SIGNALS
622

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/029138

A. CLASSIFICATION OF SUBJECT MATTER

H04L 7/02(2006.01)i, G06F 17/50(2006.01)i, H04L 12/54(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L 7/02; G01R 31/3177; G06F 11/25; H03L 7/00; G11B 20/20; G06F 3/06; H03H 11/26; H04L 12/56; G06F 17/50; H04L 12/54

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: integrated circuit, skew, priority, order, queue

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011-0185241 A1 (ROBERT ERICKSON) 28 July 2011 See paragraphs [0042]-[0052] and figures 2, 3.	1-15
Y	US 2013-0201996 A1 (CAHYA MASPUTRA et al.) 08 August 2013 See paragraphs [0076]-[0089], claims 1, 5, 6 and figures 5-7.	1-15
A	US 2008-0126888 A1 (WALLY HAAS et al.) 29 May 2008 See paragraphs [0022]-[0035], claims 1-7 and figure 1.	1-15
A	US 2011-0221497 A1 (YAN CHONG et al.) 15 September 2011 See abstract, paragraphs [0055]-[0064] and figures 4A-5.	1-15
A	US 2015-0067273 A1 (MICROSOFT CORPORATION) 05 March 2015 See abstract, claims 1-9 and figures 2, 5.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 January 2017 (11.01.2017)	**17 January 2017 (17.01.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/029138

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