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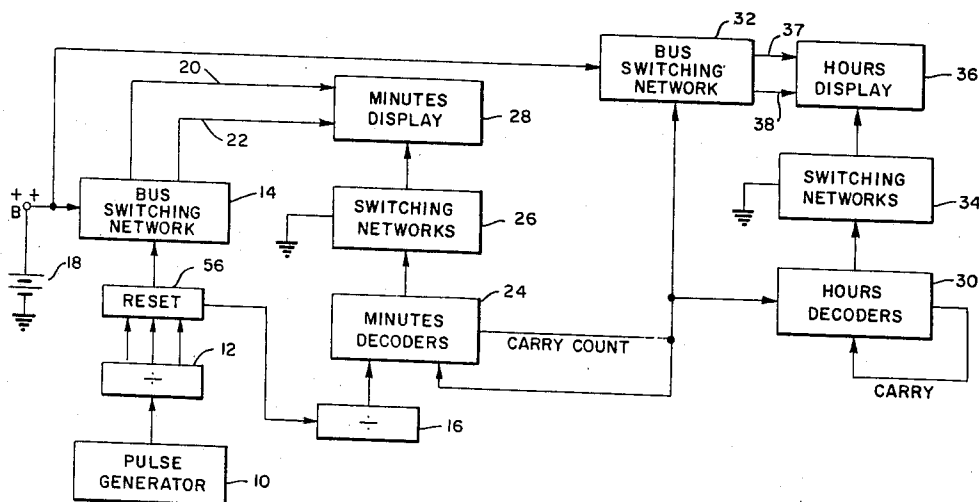
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[56] **References Cited**
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[54] **ELECTRONIC TIMEPIECE**
6 Claims, 4 Drawing Figs.

[52] U.S. Cl. **58/50,**
340/309.1
 [51] Int. Cl. **G04b 19/32**
 [50] Field of Search **58/23, 50;**
340/309.1, 309.3, 309.4, 309.5, 309.6, 332-334

ABSTRACT: A miniaturized electronic timepiece employing an electroluminescent display is disclosed. The indicia on the display are energized in the proper sequence through the use of logic circuitry and electronic switches controlled thereby.



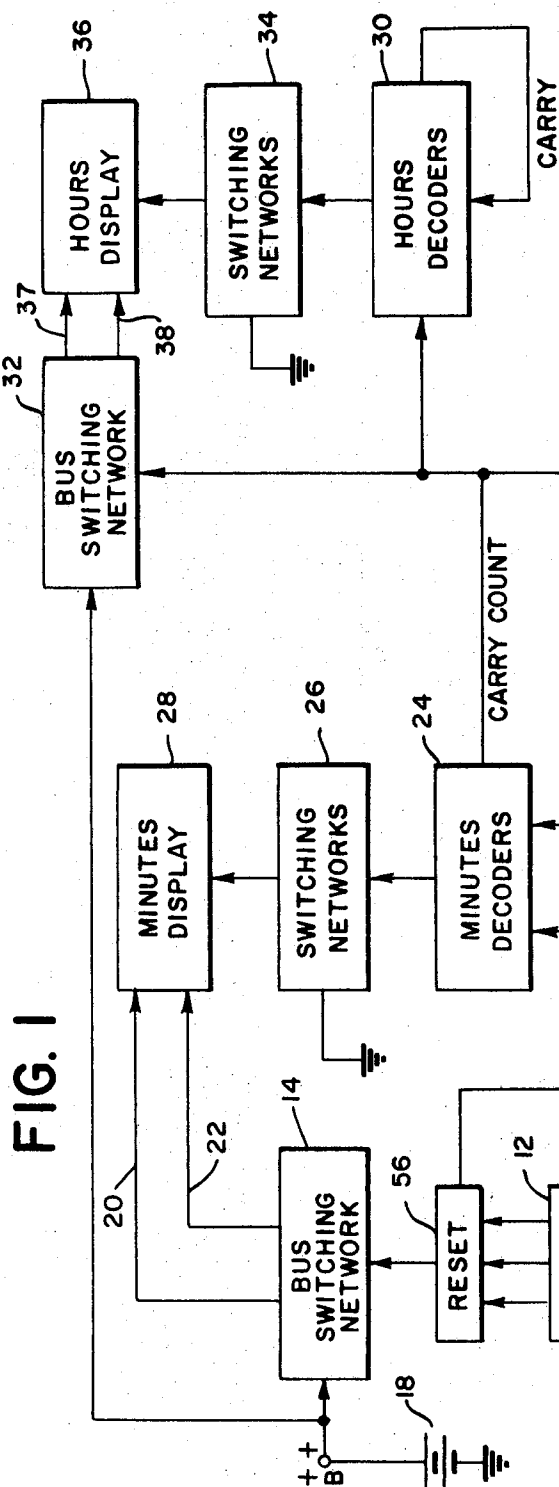


FIG. 1

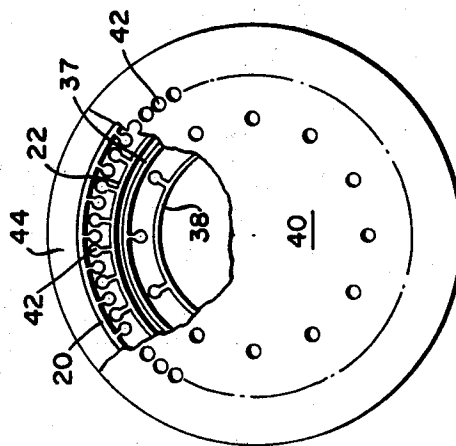
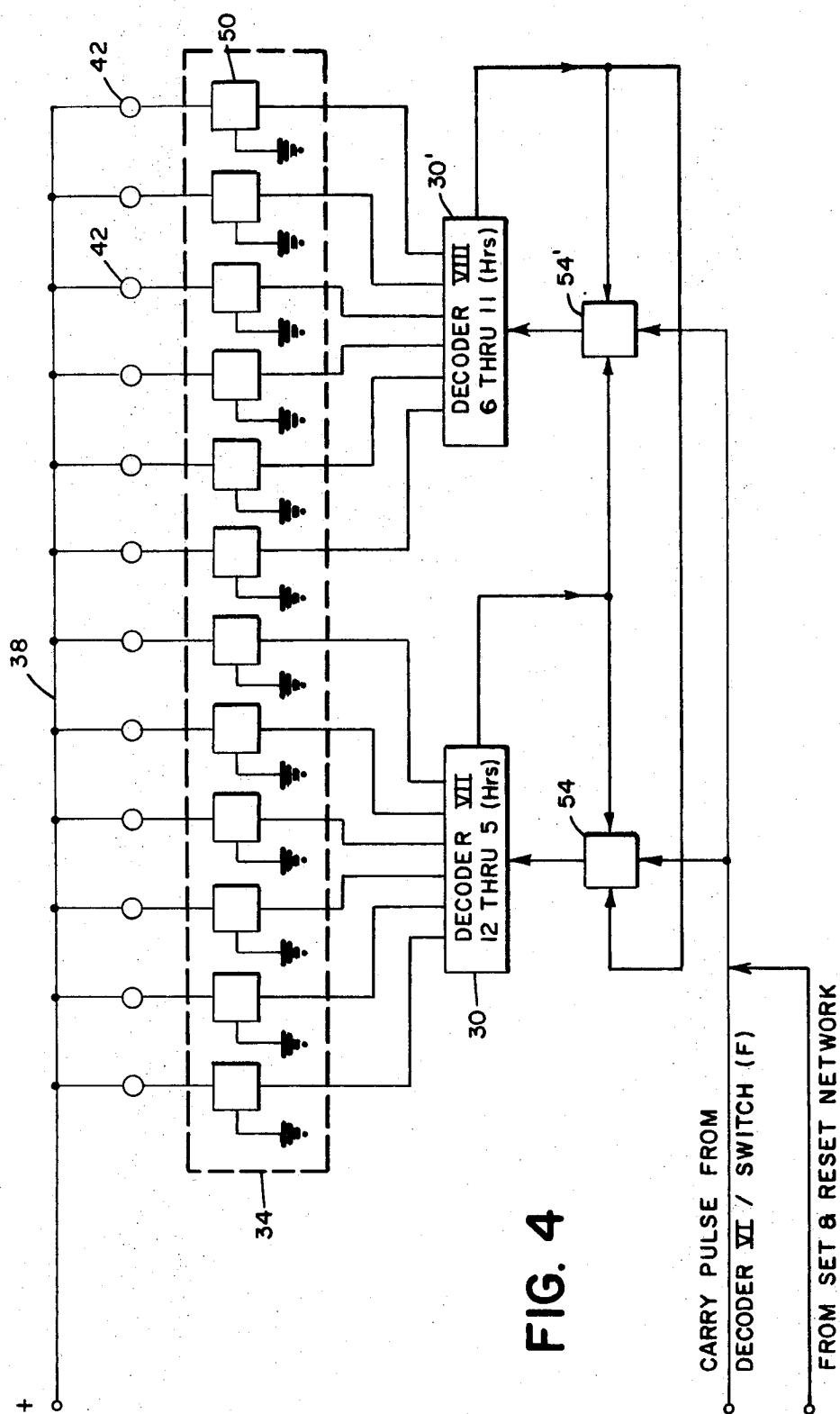


FIG. 2

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ELECTRONIC TIMEPIECE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to horology. More specifically, the present invention is directed to electronic timepieces which are susceptible to microminiaturization. Accordingly, the general objects of the present invention are to provide novel and improved methods and apparatus of such character.

2. Description of the Prior Art

Electrically operated timepieces have, of course, long been available. While most prior art electric time keeping apparatus have been electromechanical in nature, there have been attempts to produce electronic timepieces. These previous electronic timepieces have been characterized by a high degree of accuracy but, as an incident to obtaining this accuracy, considerable size, complexity and cost. Accordingly, prior art timepieces of the electronic-type have found utility largely in commercial establishments such as laboratories.

The prior art electrically operated watch is a typical electromechanical device in that it converts power supplied from a self-contained direct current source to mechanical energy which drives a moving display. Thus, while prior art "electric" watches have included some solid-state electronic circuitry, the purpose of such circuitry has been to control the application of power to an electric motor which drives the hands of the timepiece. The disadvantages inherent in the necessity to convert electrical energy to torque within a timepiece are many and are well known in the art. Suffice it to say that among the foremost of said disadvantages is the inability to employ state-of-the-art electronic manufacturing technology to the entire assembly procedure with the result that a number of manual assembly operations must be performed to both mount the indicia driving motor and to connect the motor into the remainder of the circuitry. These manual assembly techniques coupled with the relatively high cost of small precision motors adds substantially to the price of present "electric" watches.

SUMMARY OF THE INVENTION

The present invention overcomes the above-discussed and other disadvantages of the prior art by providing an electronic timepiece having no moving parts. The timepiece of the present invention is particularly well suited to miniaturization to the point where it could be included within a standard watch casing.

In accordance with the present invention, a static display energized through electronic logic and switching circuitry is employed. In a preferred embodiment the display employs discrete areas of electroluminescent material as the timepiece indicia providing medium. The various electroluminescent indicia are energized in the proper sequence by means of solid-state logic circuitry and electronic switches operated thereby. The logic and switching circuitry, in the proper sequence, establishes current paths through the areas of electroluminescent indicia defining material so as to cause the areas to fluoresce. The switching and logic circuitry is responsive to clock pulses provided by a precision oscillator. In the interest of minimizing switching circuitry, a plurality of bus bars are each associated with a group of indicia defining electroluminescent material areas whereby the indicia in each group will be enabled. The conduction of selected indicia within each of said groups will thereafter be achieved by selectively exercising control over electronic switches and thereby completing a current path through individual areas of the electroluminescent material in the proper sequence.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be better understood and its numerous objects and advantages will become apparent to those skilled in the art by reference to the accompanying drawing wherein like reference numerals refer to like elements in the several FIGS. and in which:

FIG. 1 is a block diagram of a preferred embodiment of the present invention;

FIG. 2 depicts, partly in section, the face of a timepiece which may be associated with the embodiment shown in block form in FIG. 1;

FIG. 3 is a block diagram showing a portion of the circuitry of the embodiment of FIG. 1 in greater detail; and

FIG. 4 is a block diagram showing alternative circuitry which may be employed in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference now to FIG. 1, the present invention includes a clock pulse generator 10. Pulse generator 10 may, for example, be a crystal controlled oscillator with associated pulse shaping circuitry. The oscillator will typically have an output frequency of 120 kHz. The clock pulses from generator 10 are applied to a first frequency divider circuit 12. In the embodiment of FIG. 1, which displays only minutes and hours, it is desired that the output of frequency divider 12 be at 60 cycles per hour. The input frequency to frequency divider 12, which is state-of-the-art equipment, determines the circuitry of the frequency divider.

The output pulses from frequency divider 12 are applied to a bus switching network 14 and to a second frequency divider 16. Bus switching network 14 may comprise a single-pole double-throw electronic switch of a type well known in the art. Switch 14 will connect a first polarity terminal of a current source 18 alternately to bus bars 20 and 22. Switch 14 may, for example, comprise a pair of switching transistors operating under the control of a bistable multivibrator circuit which is responsive to the output of frequency divider 12. Alternatively, switching circuit 14 may comprise a single-pole double-throw FET switch such as AMELCO Type 2126 BG available from the AMELCO Semiconductor Division of Teledyne Corporation which would similarly be controlled by a bistable multivibrator circuit.

As previously noted, the output of frequency divider 12 is also applied to a second frequency divider circuit 16. Frequency divider circuit 16 may, for example, comprise a bistable multivibrator circuit which divides the output frequency of frequency divider 12 by a factor of 2.

The output pulses provided by frequency divider 16 are applied to a minutes decoder network 24. As will be explained in greater detail below, decoder network 24 will comprise six individual decoder circuits. Each of the individual decoders will apply switching control signals to an associated switching circuit in switching network 26. The switch control signals provided by decoder 24 are applied to individual normally open switches in the switching network in sequence and at a rate which is one-half the frequency at which the source is alternately connected to bus bars 20 and 22. The switches which comprise the switching networks 26 each have first terminals which are connected to pairs of indicia defining areas of electroluminescent material within the minutes display 28. The second terminals of the switches in switching network 26 are connected to the second polarity terminal of current source 18. As will be described below, the gating on (closing) of each individual switch in the switching networks 26 will enable a pair of the indicia and the indicia of each pair will be alternately caused to fluoresce by the switching of bus switching network 14.

As previously noted, the decoder network 24 comprises six individual decoder circuits. The decoder circuits will be connected in cascade. The last stage of the decoder network provides an hourly carry pulse which is applied to an hours decoder network 30. This carry count from minutes decoder network 24 is, in the embodiment of FIG. 1, also applied to a second bus switching network 32 which, like bus switching network 14, is connected to the first polarity terminal of current source 18. The carry count from minutes decoder network 24 is further fed back to the input of the minutes decoder network so as to reset this circuitry in the manner to be described below.

The hours decoder network 30 and bus switching network 32 will respectively employ circuitry identical to that employed in minutes decoder network 24 and the bus switching network 14. The bus switching circuit 32 alternately applies voltage to bus bars 37 and 38. The hours decoder 30 will employ only a pair of individual decoder circuits. As in the case of minutes decoder network 24, hours decoder network 30 will apply switch control signals to a switching network 34. Switching network 34 may alternately employ either the same switching circuitry as utilized in switching network 26 or a separate switch may be employed for each hours indicia. If a separate switch is employed for each hours indicia, the bus switching network 32 may, as will be seen from FIG. 4, be eliminated. An hours display 36 employing 12 electroluminescent areas will be controlled, in the same manner as control is exercised over minutes display 28, by switching network 34 operating either alone or in combination with bus switching network 32. The carry output of hours decoder network 30 will be applied back to the input of this circuit for resetting purposes.

An example of a display in accordance with the present invention is shown in FIG. 2. While various light emitting devices may be employed as indicia in the present invention, an electroluminescent display is preferred. Alternatively, thin film photodiodes may be employed. In FIG. 2, the display comprises concentric rings having discrete light producing areas therein with the outer ring providing the minutes indication and the inner ring providing the hours indication. A suitable glass or plastic cover 40 will permit observation of the discrete areas 42 of electroluminescent material. Cover 40 may be translucent or may be opaque in all regions except those in registration with the areas 42; the cover being transparent in such areas. If desired, numerals or other design may be painted on the cover 40.

In the fabrication of the actual luminescent display panel, the areas 42 of material which are to provide the actual display will be either deposited through a mask on a suitable support or alternatively will be deposited as an area film and the separate areas 42 thereafter formed by conventional photofabrication (etching) techniques. In practice, the supporting substrate for the display, indicated at 44, may be a ceramic wafer. The first step in the fabrication of the display in accordance with the present invention comprises the production, on the surface of wafer 44, of circuitry which will be connected to the switching networks 26 and 34. This circuitry will typically comprise conductive terminal pads, which will be commensurate in size and shape with the electroluminescent areas 42, and conductors which extend from the terminal pads to the rear side of the wafer 44. The conductive pads and conductors will typically be thin film circuitry formed by etching an area film and the through connection to the back of wafer 44 may be accomplished about the periphery of an aperture at the center of wafer 44. After the thin film circuitry has been formed, the electroluminescent material will be deposited thereover to provide the areas 42 which overlap the conductive pads. As noted above, areas 42 may be formed either by depositing the electroluminescent material through a mask or by forming an area film of material and thereafter employing standard photofabrication techniques and an etchant, which will not affect the thin film circuitry, to remove the electroluminescent material in the areas which are not to form a part of the display. Next, the underlying thin film circuitry which has not been covered by electroluminescent material will be protected by the depositing of a layer of insulating material thereover and the bus bars 20, 22, 37 and 38 will be formed, typically by vacuum deposition through a mask, in such manner as to be in electrical contact with portions of the upper surface of each of the electroluminescent areas 42. In the embodiment of FIG. 2, the pairs of bus bars will be arcuate in shape and will bracket the rings of electroluminescent areas with which they are to be associated whereby the outer and inner bus bars will be electrically connected to top surfaces of alternate areas 42 in each ring.

Referring now to FIG. 3, the manner in which the individual electroluminescent areas 42 may be caused to fluoresce in desired sequence will be explained. FIG. 3 discloses a portion of the control circuitry for the minutes display 28. However, it is to be understood that substantially identical circuitry can be employed for the hours display 36. As previously noted, the electroluminescent areas 42 are connected at their top surfaces to either of bus bars 20 or 22. The opposite sides of the electroluminescent areas, that is the terminal pads underlying the areas are interconnected into pairs. That is, the terminal pads are electrically connected in pairs and the electroluminescent area overlying the terminal pads of each pair are connected to respective of bus bars 20 and 22.

The thus interconnected pairs of electroluminescent areas 42 (underlying terminal pads) are connected to individual switches 50 in the switching network 26. Each switching circuit of network 26 will include five of switches 50 and there will be six switching circuits 27a-27f associated with the minutes display. When operated by an output from a minutes decoder circuit in decoder network 24, the switches 50 will complete the current path from the energized one of bus bars 20 and 22 to the other side of the current source 18 whereby the electroluminescent panels may fluoresce. In the embodiment being described, the positive terminal of source 18 is applied alternately to bus bars 20 and 22 and the negative terminal of source 18 and one terminal of each of switches 50 is connected to a ground bus. The other terminal of each of switches 50 is, as noted above, connected to one side of a pair of electroluminescent areas 42. The switches 50 may comprise transistors and all of the switching circuits 27 can be formed as an integrated circuit. The control signals for switches 50 of switching circuits 27 are provided by six associated decoder circuits 25a-25f. The decoder circuits 25 may, for example, each comprise a five stage ring counter having its stages individually connected to respective of switches 50. Each of the individual decoder circuits has a double-pole double-throw solid-state switch as an input circuit. The decoder circuits 25 are themselves connected in cascade in a ring counter arrangement and the input switches 52 are closed by a carry pulse from the preceding circuit and are disabled by the carry pulse from the decoder circuit associated with the switch.

The operation of the minute display and control circuitry of FIG. 3 is as follows: The positive terminal of source 18 is alternately connected to bus bars 20 and 22 by switch 14, which operates under the control of frequency divider 12, at a frequency of 60 cycles per hour. Through the action of frequency divider 12, frequency divider 16, and the decoder network 24, switches 50 in the switching networks 27 are serially closed at a frequency of 30 cycles per hour. Accordingly, a separate one of electroluminescent areas 42 will have current passed therethrough and thus will be caused to fluoresce each time switch 14 is connected to one of bus bars 20 and 22. Accordingly, one of areas 42 will be in an activated state for each minute of operation of the circuit. The individual decoder circuit 25 and associated switching circuits 27 will each control the indicia for a 10 minute period. At the end of each 10 minute period a carry pulse will be provided at the output of a decoder circuit 25 and this output pulse will cause the closing of switch 52 in the next serially connected decoder circuit and the opening of the switch 52 in the previously operating decoder circuit. The next pulse from frequency divider 16 will therefore energize the first of switches 50 in the next switching circuit. This operation will continue with the carry pulse from the sixth decoder circuit 25f being delivered back to switch 52 of decoder circuit 25a to reclose this switch. The carry pulse from decoder circuit 25f will also be applied to the input switch of a first decoder circuit in the hours decoder network 30 whereby the hours display will be advanced by one of electroluminescent areas 42.

As noted above, the circuitry for controlling the electroluminescent hours readout 36 may be identical to that described above with respect to FIG. 3. An alternative hours readout circuit is depicted in FIG. 4. The FIG. 4 circuit employs a single

input bus 38 which is permanently connected to the positive terminal of source 18. The use of a single hours bus eliminates the need for bus switching network 32 of FIG. 1 while doubling the requirement for switches 50 in the switching network 34. This may be an economical approach since the entire switching network 34 may be comprised of a single integrated circuit. The hours display circuit will employ a pair of six stage decoder circuits 31a and 31b which operate in the same manner as minutes decoder circuits 25. The hours decoder circuits 31a and 31b, as is the case with the corresponding minutes decoder circuits, have input switches 54. The operation of the hours display control circuit is sufficiently similar to that of the minutes readout circuit so that the operation thereof will not be described herein.

It is also to be noted that, as may be seen from FIG. 1, a set and reset circuit 56 is incorporated in the timepiece. Circuit 56 may comprise merely a small spring loaded-type switch which may be used to apply relatively high frequency pulses tapped off frequency divider 12 to the input of bus switching network 14 and to frequency divider 16. Accordingly, by means of closing switch 56, the display may be set to the proper time by rapidly operating the various switches. Switch 56 will, of course, also interrupt the application of the normal 60 cycles per hour output of frequency divider 12 to switching circuit 14 and frequency divider 16.

While a preferred embodiment has been shown and described various modifications and substitutions may be made thereto without departing from the spirit and scope of the present invention. Accordingly, it is to be understood that the present invention has been described by way of illustration and not limitation.

I claim:

1. An electronic timepiece comprising:
 - a solid-state display, said display comprising a plurality of discrete areas of material capable of being stimulated to a light emissive condition by application of electrical energy;
 - at least a pair of bus bars, said bus bars being electrically

connected to respective groups of said discrete areas;
means electrically interconnecting pairs of said discrete areas, one area of each pair being connected to a different one of said bus bars;

a source of electrical power;

first switch means for alternately connecting a first terminal of said power source to said bus bars;

a source of control pulses;

means connecting said control pulse source to said first switch means;

second switch means for serially connecting said pairs of interconnected areas to a second terminal of said power source; and

means responsive to said control pulses for operating said second switch means at a frequency lower than the frequency of operation of said first switch means.

2. The apparatus of claim 1 wherein said display comprises discrete areas of electroluminescent material.

3. The apparatus of claim 1 wherein said means for operating said second switch means comprises:

frequency divider means responsive to said control pulses for generating lower frequency pulses; and

means responsive to said lower frequency pulses for generating switching control signals in serial fashion.

4. The apparatus of claim 3 wherein said second switch means comprises a plurality of normally open electronic switches, each of said switches having a first terminal connected to one of said pairs of interconnected areas, the other terminal of each of said switches being connected to the second terminal of said power source, said switches being serially closed by said switching control signals.

5. The apparatus of claim 4 further comprising means for applying pulses at a frequency higher than the frequency of said control pulses to said first switch means and to said frequency divider means whereby said timepiece may be rapidly set to the desired state.

6. The apparatus of claim 5 wherein said first switch means comprises a single-pole, double-throw solid-state switch.