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(54) Title: LASER, PLASMA ETCH, AND BACKSIDE GRIND PROCESS FOR WAFER DICING

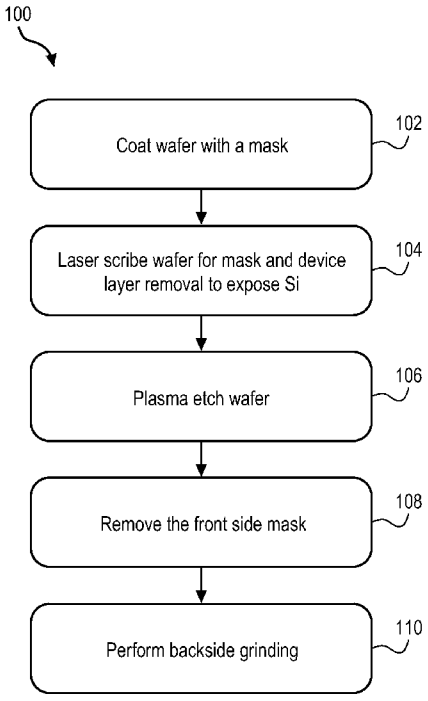


FIG. 1

(57) Abstract: Front side laser scribing and plasma etch are performed followed by back side grind to singulate integrated circuit chips (ICs). A mask is formed covering ICs formed on the wafer, as well as any bumps providing an interface to the ICs. The mask is patterned by laser scribing to provide a patterned mask with gaps. The patterning exposes regions of the semiconductor wafer, below thin film layers from which the ICs are formed. The semiconductor wafer is then etched through the gaps in the patterned mask to advance a front of an etched trench partially through the semiconductor wafer thickness. The front side mask is removed, a backside grind tape applied to the front side, and a back side grind performed to reach the etched trench, thereby singulating the ICs.

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LASER, PLASMA ETCH, AND BACKSIDE GRIND PROCESS FOR WAFER DICING

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority to U.S. Provisional Application No. 61/790,976 filed on March 15, 2013, titled "LASER, PLASMA ETCH, AND BACKSIDE GRIND PROCESS FOR WAFER DICING," and U.S. Provisional Application No. 61/671,617 filed on July 13, 2012, titled "LASER, PLASMA ETCH, AND BACKSIDE GRIND PROCESS FOR WAFER DICING," the entire contents of which are hereby incorporated by reference in their entirety for all purposes.

BACKGROUND

1) FIELD

[0002] Embodiments of the present invention pertain to the field of semiconductor processing and, in particular, to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

2) DESCRIPTION OF RELATED ART

[0003] In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as a substrate) composed of silicon or other semiconductor material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. These materials are doped, deposited and etched using various well-known processes to form integrated circuits. Each wafer is processed to form a large number of individual regions containing integrated circuits known as dice or dies.

[0004] Following the integrated circuit formation process, the wafer is "diced" to separate the individual die from one another for packaging or for use in an unpackaged form within larger circuits. The two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These scribe lines extend along the spaces between the dies. These spaces are commonly referred to as "streets." The diamond scribe forms shallow scratches in the wafer surface along the streets. Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines. The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker wafers, sawing is presently the preferred method for dicing.

[0005] With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer surface and saws the wafer along the streets. The wafer is mounted on a supporting member such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both the vertical and horizontal streets. One problem with either scribing or

sawing is that chips and gouges can form along the severed edges of the dies. In addition, cracks can form and propagate from the edges of the dies into the substrate and render the integrated circuit inoperative. Chipping and cracking are particularly a problem with scribing because only one side of a square or rectangular die can be scribed in the direction of the crystalline structure. Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dies on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the actual integrated circuits. As a result of the spacing requirements, not as many dies can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximate 15 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits; three to five hundred microns often must separate the circuitry of each of the dies. Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

[0006] Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma processing of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

[0007] One or more embodiments of the invention are directed to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

[0008] According to one embodiment, a method of dicing a semiconductor wafer including a plurality of integrated circuits involves forming a mask above the semiconductor wafer. The mask covers and protects the integrated circuits. The method involves patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The method also includes etching the semiconductor wafer through the gaps in the patterned mask to advance a trench partially through the semiconductor wafer. The method also includes back side grinding the semiconductor wafer to reach the etched trench.

[0009] According to one embodiment, a system for dicing a substrate including a plurality of integrated circuits (ICs) includes a laser scribe module to pattern a multi-layered mask disposed above a substrate to form a trench exposing regions of a substrate between the

ICs. The system also includes a plasma etch module physically coupled to the laser scribe module to plasma etch the substrate. The system also includes a back side grinding module to perform back side grinding of the substrate to reach the etched trench. The system also includes a robotic transfer chamber to transfer a laser scribed substrate from the laser scribe module to the plasma etch module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Embodiments of the present invention are illustrated by way of example, and not by way of limitation, and can be more fully understood with reference to the following detailed description when considered in connection with the figures in which:

[0011] Figure 1 is a flowchart representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention;

[0012] Figures 2A, 2B, 2C, and 2D illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performance of a method of dicing the semiconductor wafer, corresponding to operations of Figure 1, in accordance with embodiments of the present invention;

[0013] Figure 3 illustrates a cross-sectional view of a stack of materials that may be present in a street region of a semiconductor wafer or substrate, in accordance with embodiments of the present invention;

[0014] Figure 4 illustrates a block diagram of a tool layout for laser and plasma dicing of substrates with an integrated deposition module for in-situ application of a multi-layered mask, in accordance with an embodiment of the present invention; and

[0015] Figure 5 illustrates a block diagram of an exemplary computer system which controls automated performance of one or more operation in the masking, laser scribing, plasma dicing methods described herein, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0016] Methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon, are described. In the following description, numerous specific details are set forth, such as laser and plasma etch wafer dicing approaches with UV-curable adhesive films, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn

to scale.

[0017] When dicing wafers that are 300μm or thicker, the wafers are rigid enough to be directly placed on mounting tapes without die attach film (DAF). In circumstances where wafers are placed on mounting tapes without DAF, no DAF cutting process is involved. Embodiments described herein address the dicing applications of integrated circuit (IC) wafers (e.g., integrated wafers with processor chips) that have a thickness of 300μm to 800μm, but preferably in the range of 300μm to 600μm thickness. Furthermore, embodiments address dicing applications of integrated circuit wafers with an acceptable dicing kerf width of 50μm to 200μm width, preferably 50μm to 100μm measured on the wafer front surface. A kerf width of 50μm to 100μm measured on the wafer front surface corresponds to a typical kerf width measured from the back side of the wafer of 30-50μm in a laser/saw hybrid process.

[0018] In embodiments, a hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch is implemented for die singulation. The laser scribe process may be used to cleanly remove a mask layer, organic and inorganic dielectric layers, and device layers. The laser etch process may then be terminated upon exposure of, or partial etch of, the wafer or substrate. The plasma etch portion of the dicing process may then be employed to etch through the bulk of the wafer or substrate, such as through bulk single crystalline silicon, to yield die or chip singulation or dicing.

[0019] In embodiments, a method uses a hybrid approach employing laser scribing, plasma etching, and wafer back side grinding to dice the wafers with thickness' ranging from 250μm to 750μm. The laser scribing removes difficult-to-etch passivation layers, dielectric layers, and metal layers until the underlying silicon substrate is exposed. Plasma etching generates trenches of a depth to the target die thickness. Finally, backside grinding removes the remaining silicon thickness until the etched trenches are reached to realize die singulation. An advantage of an embodiment employing this hybrid singulation technique is a well-balanced dicing quality due to laser scribing and plasma etch, and increased throughput through further incorporation of backside grinding. The use of laser and plasma etch can be an advantageous extension of the dicing before grinding (DBG) approach to thick die singulation, where typically a laser or blade saw first cuts trenches into the semiconductor wafer to the desired die thickness, immediately followed by the backside grinding. According to one embodiment, the proposed approach uses both laser scribing and plasma etching instead of only laser scribing or blade sawing to generate trenches in a semiconductor wafer. In one embodiment, a method using laser scribing and plasma etching dices wafers that are 250μm or thicker. Embodiments of the invention fit into current production flow easily and have improved throughput over techniques lacking plasma etching.

[0020] Figure 1 illustrates operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention. Figures 2A-2D illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performance of the methods.

[0021] During the first operation 102 of the method 100 of Figure 1, and corresponding to Figure 2A, a front side mask 202 is formed above a semiconductor wafer or substrate 204. According to one embodiment, the semiconductor wafer or substrate 204 has a diameter of at least 300 mm and has a thickness prior to back side grinding of 300μm to 800μm. As illustrated, in an embodiment, the mask is a conformal mask. Conformal mask embodiments advantageously ensure sufficient thickness of the mask over an underlying topography (e.g., 20 μm bumps, not shown) to survive the duration of a plasma etch dicing operation. In alternative embodiments, however, the mask is a non-conformal, planarized mask (e.g., thickness of the mask over a bump is less than thickness of the mask in a valley). Formation of a conformal mask may be by CVD, for example, or by any other process known in the art. In one embodiment, the mask 202 covers and protects integrated circuits (ICs) formed on the surface of semiconductor wafer and also protects bump projecting or protruding up 10-20μm from the surface of the semiconductor wafer. The mask 202 also covers intervening streets formed between adjacent ones of the integrated circuits.

[0022] In accordance with an embodiment of the present invention, forming the mask 202 includes forming a layer such as, but not limited to, a water-soluble layer (PVA, etc.), and/or a photo-resist layer, and/or an I-line patterning layer. For example, a polymer layer such as a photo-resist layer may be composed of a material otherwise suitable for use in a lithographic process. In embodiments with multiple mask layers, a water-soluble base coat may be disposed below a non-water-soluble overcoat. The basecoat then provides a means of stripping the overcoat while the overcoat provides plasma etch resistance and/or for good mask ablation by the laser scribing process. It has been found for example, that mask materials transparent to the laser wavelength employed in the scribing process contribute to low die edge strength. Hence, a water-soluble base coat, of PVA, for example, as the first mask material layer, may function as a means of undercutting a plasma-resistant/laser energy absorbing overcoat layer of the mask so that the entire mask may be removed/lifted off from the underlying integrated circuit (IC) thin film layer. The water-soluble base coat may further serve as a barrier protecting the IC thin film layer from the process used to strip the energy absorbing mask layer. In embodiments, the laser energy absorbing mask layer is UV-curable and/or UV absorbing, and/or green-band (500-540 nm) absorbing. Exemplary materials include many photo-resists and polyimide (PI) materials conventionally employed for passivation layers of IC chips. In one embodiment, the photo-resist

layer is composed of a positive photo-resist material such as, but not limited to, a 248 nanometer (nm) resist, a 193 nm resist, a 157 nm resist, an extreme ultra-violet (EUV) resist, or a phenolic resin matrix with a diazonaphthoquinone sensitizer. In another embodiment, the photo-resist layer is composed of a negative photo-resist material such as, but not limited to, poly-cis-isoprene and poly-vinyl-cinnamate.

[0023] Referring again to Figure 2A, the semiconductor wafer or substrate 204 has disposed thereon or therein, as a portion of the integrated circuits 206, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits. Conductive bumps and passivation layers 208 may be formed above the interconnect layers. Materials making up the streets may be similar to or the same as those materials used to form the integrated circuits. For example, streets may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets includes test devices similar to the actual devices of the integrated circuits.

[0024] Returning to Figure 1, and turning to corresponding Figure 2B, the method 100 proceeds with bulk target layer material removal at operation 104. To minimize dielectric delamination and cracking, a femtosecond laser is preferred. However, depending on the device structure, an ultraviolet (UV), picosecond, or nanosecond laser source can also be applied. The laser has a pulse repetition frequency in the range of 80kHz to 1MHz, ideally in the range of 100kHz to 500kHz.

[0025] Referring again to Figure 2B, the laser scribing process is performed generally to remove the material of the streets present between the integrated circuits 206. In accordance with an embodiment of the present invention, patterning the mask 202 with the laser scribing process includes forming trenches 210 partially into the regions of the semiconductor wafer between the integrated circuits. In an embodiment, patterning the mask with the laser scribing process includes direct writing a pattern using a laser having a pulse width in the femtosecond range. Specifically, a laser with a wavelength in the visible spectrum (e.g., green band, or 500-540 nm) or the ultra-violet (UV, or 300-400 nm band) or infra-red (IR) band (the three totaling a broadband optical spectrum) may be used to provide a femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for complex films such as films of the mask, the streets and, possibly, a portion of the semiconductor wafer or substrate.

[0026] Laser parameters selection, such as pulse width, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

[0027] A street between individual integrated circuits disposed on a wafer or substrate may include the similar or same layers as the integrated circuits themselves. For example, Figure 3 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present invention. Referring to Figure 3, a street region 300 includes the top portion 302 of a silicon substrate, a first silicon dioxide layer 304, a first etch stop layer 306, a first low K dielectric layer 308 (e.g., having a dielectric constant of less than the dielectric constant of 4.0 for silicon dioxide), a second etch stop layer 310, a second low K dielectric layer 312, a third etch stop layer 314, an undoped silica glass (USG) layer 316, a second silicon dioxide layer 318, and a layer of photo-resist 320 or some other mask. Copper metallization 322 is disposed between the first and third etch stop layers 306 and 314 and through the second etch stop layer 310. In a specific embodiment, the first, second and third etch stop layers 306, 310 and 314 are composed of silicon nitride, while low K dielectric layers 308 and 312 are composed of a carbon-doped silicon oxide material.

[0028] Under conventional laser irradiation (such as nanosecond-based or picosecond-based laser irradiation), the materials of street 300 may behave quite differently in terms of optical absorption and ablation mechanisms. For example, dielectrics layers such as silicon dioxide, is essentially transparent to all commercially available laser wavelengths under normal conditions. By contrast, metals, organics (e.g., low K materials) and silicon can couple photons very easily, particularly in response to nanosecond-based or picosecond-based laser irradiation. In an embodiment, however, a femtosecond-based laser process is used to pattern a layer of silicon dioxide, a layer of low K material, and a layer of copper by ablating the layer of silicon dioxide prior to ablating the layer of low K material and the layer of copper. In a specific embodiment, pulses of approximately less than or equal to 400 femtoseconds are used in a femtosecond-based laser irradiation process to remove a mask, a street, and a portion of a silicon substrate. In another embodiment, pulses of approximately less than or equal to 500 femtoseconds are used.

[0029] In accordance with an embodiment of the present invention, suitable femtosecond-based laser processes are characterized by a high peak intensity (irradiance) that usually leads to nonlinear interactions in various materials. In one such embodiment, the femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500 femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns.

[0030] The spacial beam profile at the work surface may be a single mode (Gaussian) or have a shaped top-hat profile. In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500kHz to 5MHz. In an embodiment, the laser source delivers pulse energy at the work surface approximately in the range of 0.5 μJ to 100 μJ, although preferably approximately in the range of 1μJ to 5μJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500mm/sec to 5m/sec, although preferably approximately in the range of 600mm/sec to 2m/sec.

[0031] The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. The laser may be applied either in a train of single pulses at a given pulse repetition rate or a train of pulse bursts. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

[0032] Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf width) and depth. As described above, a femtosecond-based laser is far more suitable to providing such advantages, as compared with picosecond-based and nanosecond-based laser ablation processes. However, even in the spectrum of femtosecond-based laser ablation, certain wavelengths may provide better performance than others. For example, in one embodiment, a femtosecond-based

laser process having a wavelength close to (e.g., 500-540 nm), or in the UV range (e.g., 300-400 nm) provides a cleaner ablation process than a femtosecond-based laser process having a wavelength close to or in the IR range. In a specific such embodiment, a femtosecond-based laser process suitable for semiconductor wafer or substrate scribing is based on a laser having a wavelength of approximately less than or equal to 540 nanometers. In a particular such embodiment, pulses of approximately less than or equal to 400 femtoseconds of the laser having the wavelength of approximately less than or equal to 540 nanometers are used. However, in an alternative embodiment, dual laser wavelengths (e.g., a combination of an IR laser and a UV laser) are used.

[0033] Returning to Figure 1, and turning to corresponding Figure 2C, the semiconductor wafer is next plasma etched at operation 106. As illustrated in Figure 2C, the plasma etch front proceeds through the gaps in the patterned mask 202. In accordance with an embodiment of the present invention, etching the semiconductor wafer includes etching the trenches formed with the laser scribing process so as to not etch entirely through semiconductor wafer. In one embodiment, the plasma etching operation employs a through-silicon via type etch process.

[0034] In a specific embodiment, during the etch process the etch rate of the material of the silicon of the semiconductor wafer 204 is greater than 25 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, CA, USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling, which gives more independent control of the ion density and ion energy than is possible with capacitive coupling only, even with the improvements provided by magnetic enhancement. This combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. Multi-RF source configurations also results in an exceptionally wide process window. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer 204 at an etch rate greater than approximately 40% of conventional silicon etch rates (e.g., 40 μm, or more) while maintaining essentially precise profile control and virtually scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally is a fluorine-based gas such as SF_6, C_4F_6, C_4F_8, CF_4, CHF_3, XeF_2, or any other reactant gas capable of etching silicon at a relatively fast etch rate.

[0035] Returning to Figure 1, and turning to Figure 2D, following the plasma etch at

operation 106, the integrated circuits remain coupled together by the substrate 204. According to one embodiment, a backside grinding operation 110 is then performed to polish through the substrate to reach the plasma etched trench and singulate the IC chips. In the exemplary embodiment of method 100, the front side mask is first removed at operation 108. According to one embodiment, the backside tape 209 is removed, and tape 211 (e.g., back side grinding (BSG) tape or other protection tape) is applied to the front side. Any conventional BSG process is then performed at operation 110.

[0036] Turning to Figure 4, a single integrated platform 400 may be configured to perform many or all of the operations in the hybrid laser ablation-plasma etch singulation process 100. For example, Figure 4 illustrates a block diagram of a cluster tool 406 coupled with laser scribe apparatus 410 for laser and plasma dicing of substrates, in accordance with an embodiment of the present invention. Referring to Figure 4, the cluster tool 406 is coupled to a factory interface 402 (FI) having a plurality of load locks 404. The factory interface 402 may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus 410 and cluster tool 406. The factory interface 402 may include robots with arms or blades for transferring substrates (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool 406 or laser scribe apparatus 410, or both.

[0037] A laser scribe apparatus 410 is also coupled to the FI 402. In an embodiment, the laser scribe apparatus 410 includes a femtosecond laser operating in the 300-540nm band. The femtosecond laser to performing the laser ablation portion of the hybrid laser and etch singulation process 100. In one embodiment, a moveable stage is also included in laser scribe apparatus 410, the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the femtosecond-based laser. In a specific embodiment, the femtosecond laser is also moveable.

[0038] The cluster tool 406 includes one or more plasma etch chambers 408 coupled to the FI by a robotic transfer chamber 450 housing a robotic arm for in-vaccuo transfer of substrates. The plasma etch chambers 408 is suitable for performing a plasma etch portion of the hybrid laser and etch singulation process 100. In one exemplary embodiment, the plasma etch chamber 408 is further coupled to an SF_6 gas source and at least one of a C_4F_8 and C_4F_6 source. In one embodiment, the plasma etch chamber 408 is coupled to an SF_6 gas source and at least one of a C_4F_8, CF_4, and C_4F_6 source. In a specific embodiment, the one or more plasma etch chambers 408 is an Applied Centura® SilviaTM Etch system, available from Applied Materials of Sunnyvale, CA, USA, although other suitable etch systems are also available commercially. In an embodiment, more than one etch chamber 408 is included in the cluster tool 406 portion of integrated platform 400 to enable high manufacturing throughput of the singulation or dicing

process.

[0039] The cluster tool 406 may include other chambers suitable for performing functions in the hybrid laser ablation-plasma etch singulation process 100. In the exemplary embodiment illustrated in Figure 4, the cluster tool 406 includes both a mask formation module 412 and a wet station 414, though either may be provided in absence of the other. The mask formation module 412 may be a spin coating module. As a spin coating module, a rotatable chuck is configured to clamp by vacuum, or otherwise, a thinned substrate mounted on a carrier such as backing tape mounted on a frame. In further embodiments, the spin coating module is fluidly coupled to an aqueous solution source.

[0040] Embodiments of the wet station 414 are to dissolve the water-soluble mask material layer after plasma etching the substrate. The wet station 414 may include for example a pressurized spray jet to dispense water other solvent.

[0041] Figure 5 illustrates a computer system 500 within which a set of instructions, for causing the machine to execute one or more of the scribing methods discussed herein may be executed. The exemplary computer system 500 includes a processor 502, a main memory 504 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 506 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 518 (e.g., a data storage device), which communicate with each other via a bus 530.

[0042] Processor 502 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 502 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, etc. Processor 502 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 502 is configured to execute the processing logic 526 for performing the operations and steps discussed herein.

[0043] The computer system 500 may further include a network interface device 508. The computer system 500 also may include a video display unit 510 (e.g., a liquid crystal display (LCD) or a cathode ray tube (CRT)), an alphanumeric input device 512 (e.g., a keyboard), a cursor control device 514 (e.g., a mouse), and a signal generation device 516 (e.g., a speaker).

[0044] The secondary memory 518 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 531 on which is stored one or more sets of instructions (e.g., software 522) embodying any one or more of the methodologies or functions described herein. The software 522 may also reside, completely or at least partially,

within the main memory 504 and/or within the processor 502 during execution thereof by the computer system 500, the main memory 504 and the processor 502 also constituting machine-readable storage media. The software 522 may further be transmitted or received over a network 520 via the network interface device 508.

[0045] While the machine-accessible storage medium 531 is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media, and other non-transitory machine-readable storage medium.

[0046] It is to be understood that the above description is intended to be illustrative, and not restrictive. For example, while flow diagrams in the figures show a particular order of operations performed by certain embodiments of the invention, it should be understood that such order is not required (e.g., alternative embodiments may perform the operations in a different order, combine certain operations, overlap certain operations, etc.). Furthermore, many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. Although the present invention has been described with reference to specific exemplary embodiments, it will be recognized that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask covering and protecting the integrated circuits;

patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits;

etching the semiconductor wafer through the gaps in the patterned mask to advance a trench partially through the semiconductor wafer; and

back side grinding the semiconductor wafer to reach the etched trench.

2. The method of claim 1, further comprising removing the mask following the plasma etch and prior to the back side grinding.

3. The method of claim 1, wherein the back side grinding further comprises applying a protection tape on a front side of the semiconductor wafer prior to the back side grinding.

4. The method of claim 3, further comprising removing the protection tape from a backside of the semiconductor wafer after the plasma etch.

5. The method of claim 1, wherein the semiconductor wafer has a diameter of at least 300 mm and has a thickness prior to the back side grinding of 300μm to 800μm.

6. The method of claim 1, wherein patterning the mask further comprises direct writing a pattern with a femtosecond laser having a wavelength less than or equal to 540 nanometers and a laser pulse width less than or equal to 400 femtoseconds.

7. The method of claim 1, wherein forming the mask further comprises depositing a water-soluble mask layer on the semiconductor wafer.

8. The method of claim 7, wherein the water-soluble mask layer comprises PVA.

9. The method of claim 8, wherein forming the mask further comprises depositing a multi-layered mask comprising the water-soluble mask layer as a base coat and a non-water-soluble

mask layer as an overcoat on top of the base coat.

10. The method of claim 9, wherein the non-water-soluble mask layer is a photo-resist or a polyimide (PI).

11. A system for dicing a substrate comprising a plurality of integrated circuits (ICs), the system comprising:

a laser scribe module to pattern a multi-layered mask disposed above a substrate to form a trench exposing regions of a substrate between the ICs;

a plasma etch module physically coupled to the laser scribe module to plasma etch the substrate to advance the trench partially through the substrate;

a back side grinding module to perform back side grinding of the substrate to reach the etched trench; and

a robotic transfer chamber to transfer a laser scribed substrate from the laser scribe module to the plasma etch module.

12. The system of claim 11, wherein the laser scribe module comprises a femtosecond laser having a wavelength less than or equal to 540 nanometers and a pulse width of less than or equal to 400 femtoseconds.

13. The system of claim 11, wherein the plasma etch module uses SF_6 and at least one of C_4F_8 and C_4F_6.

14. The system of claim 11, wherein the laser scribe module is to further remove the mask following the plasma etch and prior to the back side grinding.

15. The system of claim 11, further comprising a tape applicator to apply a protection tape on a front side of the substrate prior to the back side grinding.

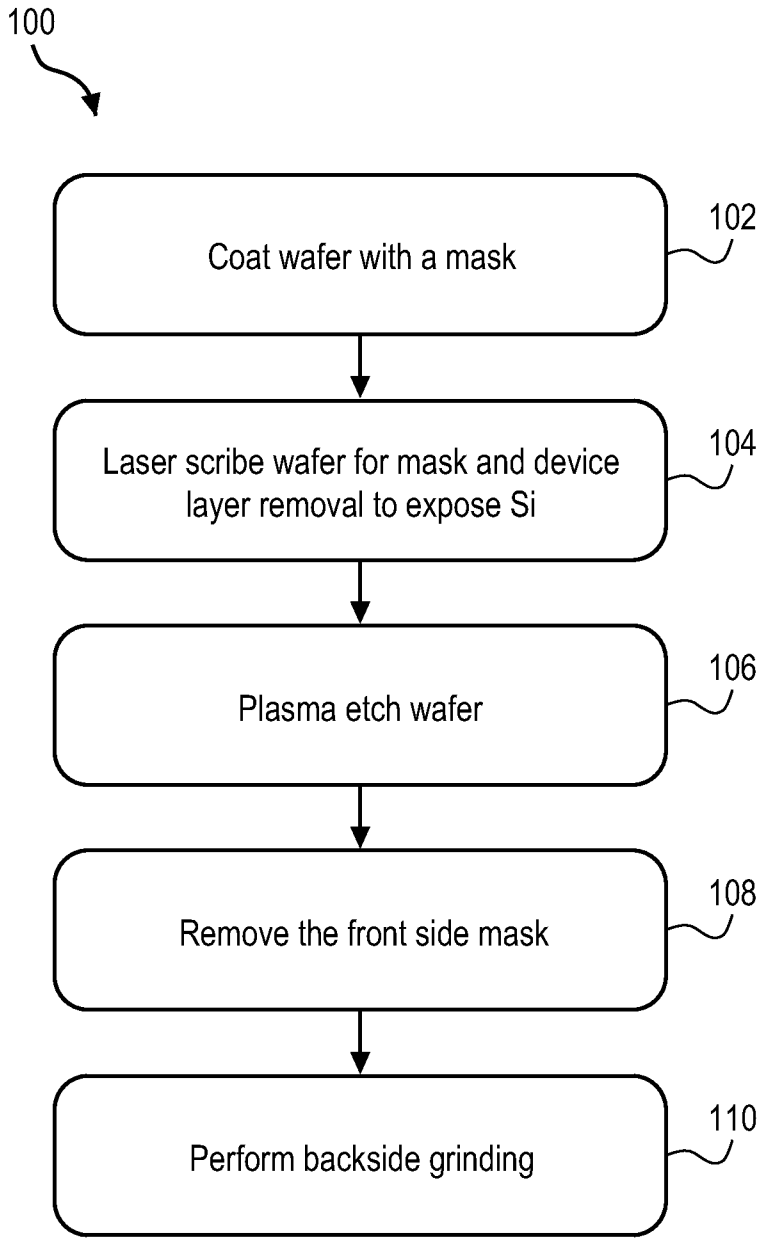

100
Coat wafer with a mask
102
Laser scribe wafer for mask and device layer removal to expose Si
104
Plasma etch wafer
106
Remove the front side mask
108
Perform backside grinding
110

FIG. 1

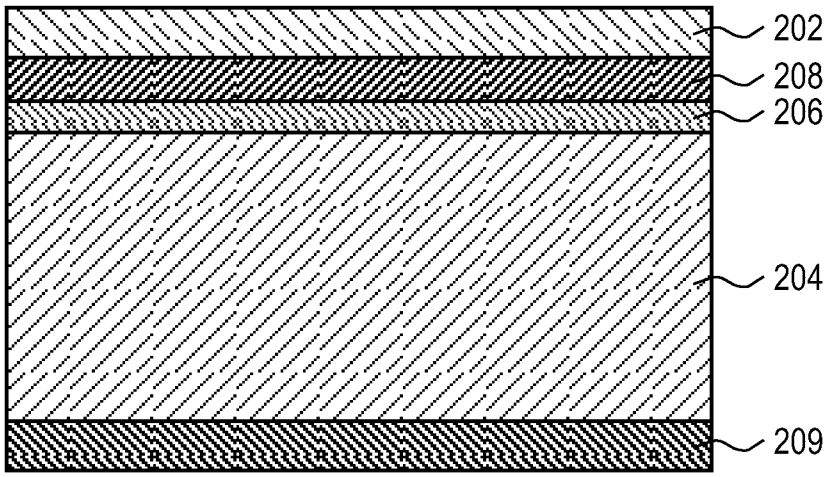


FIG. 2A

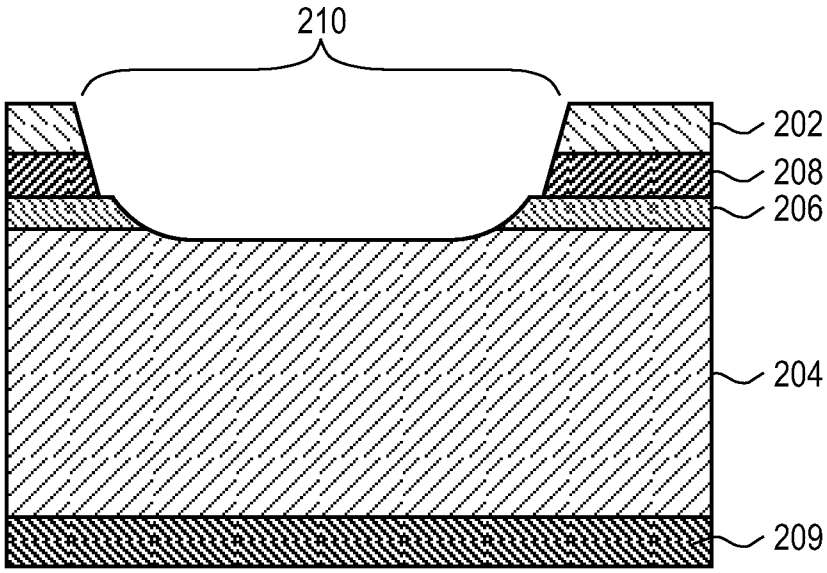


FIG. 2B

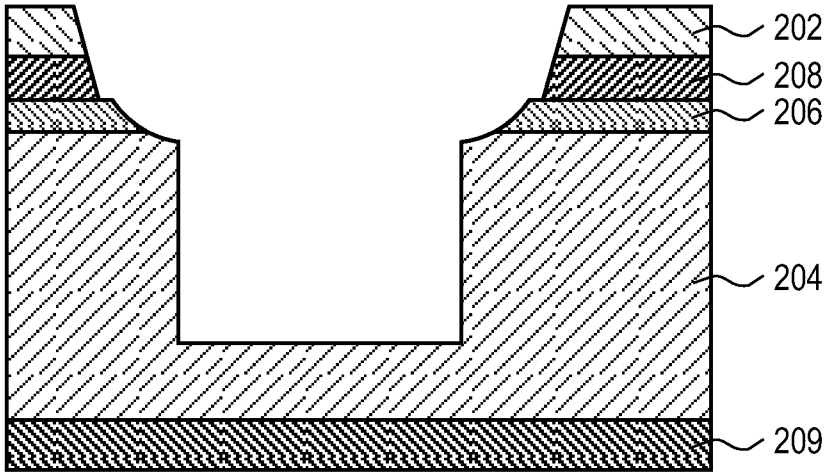


FIG. 2C

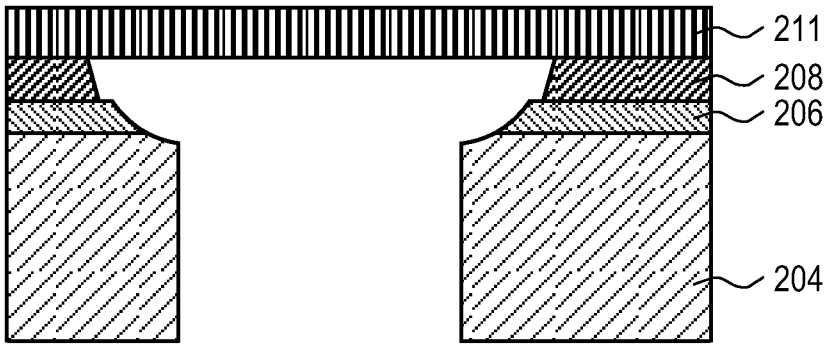


FIG. 2D

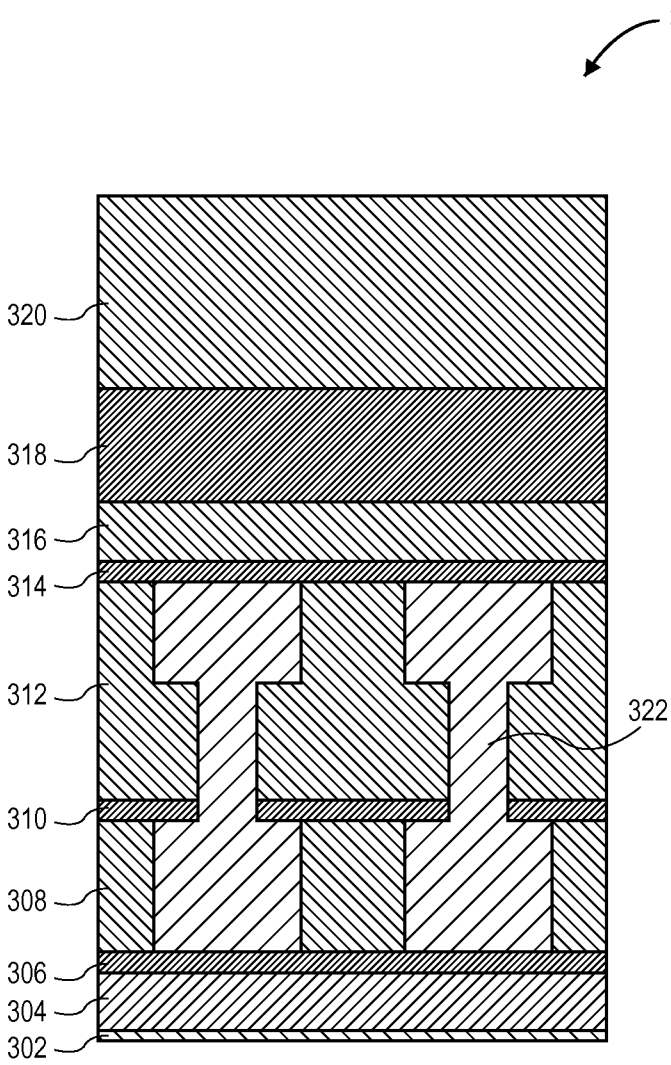


FIG. 3

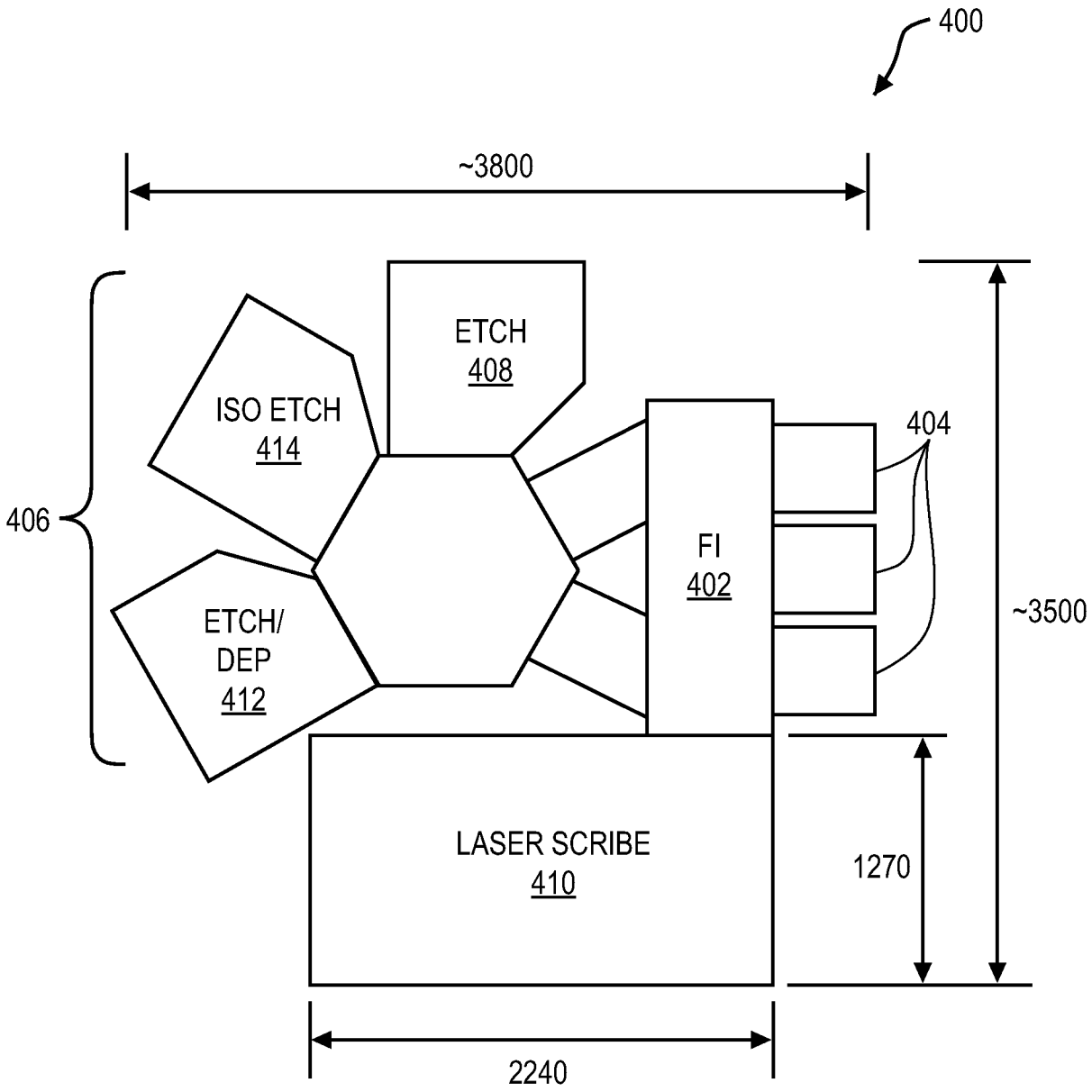
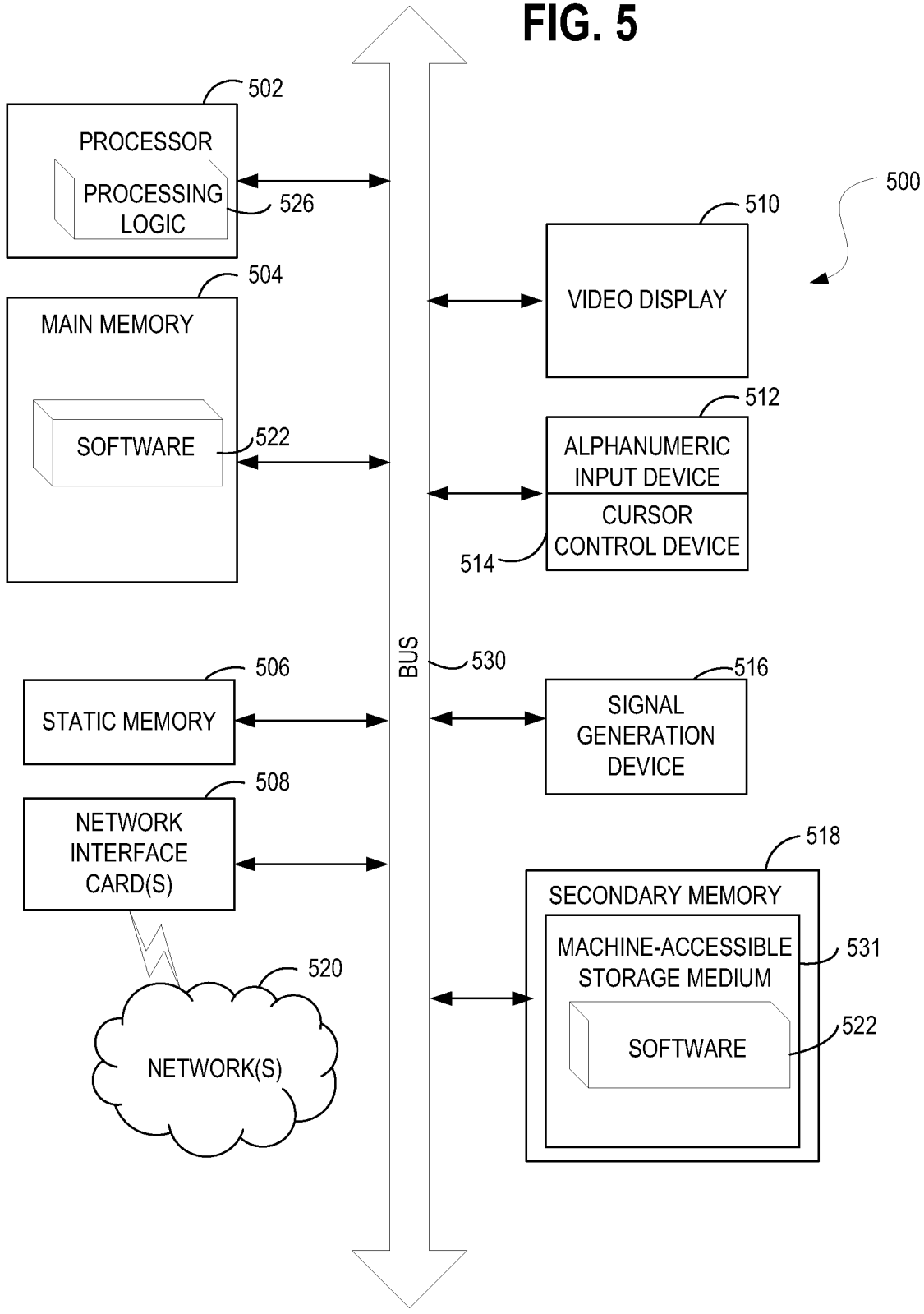

400
~3800
ETCH
408
ISO ETCH
414
406
ETCH/
DEP
412
FI
402
404
~3500
LASER SCRIBE
410
1270
2240

FIG. 4

FIG. 5


502
PROCESSOR
PROCESSING LOGIC
526
504
MAIN MEMORY
SOFTWARE
522
506
STATIC MEMORY
508
NETWORK INTERFACE CARD(S)
520
NETWORK(S)
BUS
530
500
510
VIDEO DISPLAY
512
ALPHANUMERIC INPUT DEVICE
CURSOR CONTROL DEVICE
514
516
SIGNAL GENERATION DEVICE
518
SECONDARY MEMORY
MACHINE-ACCESSIBLE STORAGE MEDIUM
531
SOFTWARE
522

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/050123

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/301(2006.01)i, H01L 21/3065(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/301; H01L 21/3065; H01L 21/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: mask, forming, etching, grinding, patterning, tape.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KR 10-2012-0020944 A (AURUM SEMICONDUCTOR et al.) 08 March 2012 See claims 1-2, 8, 10 and figure 7.	1-15
A	KR 10-2008-0015771 A (MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.) 20 February 2008 See claims 1-2, paragraphs [0014]-[0026] and figure 1.	1-15
A	US 2012-0040510 A1 (HOSEUNG YOO) 16 February 2012 See claim 1 and paragraphs [0010]-[0018].	1-15
A	JP 2009-123987 A (PANASONIC CORP.) 04 June 2009 See claim 1 and figures 2-3.	1-15
A	KR 10-2002-0068608 A (AMKOR TECHNOLOGY KOREA, INC.) 28 August 2002 See claims 1, 4, pages 2-3 and figures 1a-1e.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2013 (25.10.2013)	**28 October 2013 (28.10.2013)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	Authorized officer CHOI, Sang Won Telephone No. +82-42-481-8291

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/050123

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2012-0020944 A	08/03/2012	None	
KR 10-2008-0015771 A	20/02/2008	CN 100456449 C0	28/01/2009
		CN 101044613 A	26/09/2007
		EP 1797589 A1	20/06/2007
		JP 2007-019386 A	25/01/2007
		JP 4285455 B2	24/06/2009
		US 2009-0209087 A1	20/08/2009
		US 7923351 B2	12/04/2011
		WO 2007-007883 A1	18/01/2007
US 2012-0040510 A1	16/02/2012	JP 2012-525010 A	18/10/2012
		KR 10-2012-0007524 A	20/01/2012
		TW 201104736 A	01/02/2011
		WO 2010-124179 A2	28/10/2010
		WO 2010-124179 A3	20/01/2011
JP 2009-123987 A	04/06/2009	JP 2009-123988 A	04/06/2009
		JP 4882970 B2	22/02/2012
		JP 4882971 B2	22/02/2012
		KR 10-1097682 B1	22/12/2011
		TW 200935506 A	16/08/2009
		US 2010-0048001 A1	25/02/2010
		US 7994026 B2	09/08/2011
		WO 2009-063620 A1	22/05/2009
KR 10-2002-0068608 A	28/08/2002	None	