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T918,008

INTEGRATED CIRCUIT STRUCTURE ELECTRICALLY ISOLATED BY A COMBINATION OF AMORPHOUS SILICON WALLS AND ISOLATING PN JUNCTION

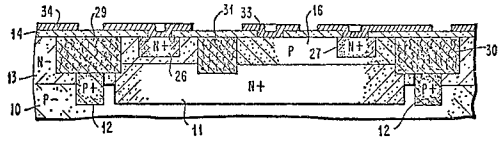
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U.S. Cl. 317—235 R

1 Sheet Drawing. 15 Pages Specification



A planar monocrystalline silicon integrated circuit structure having a plurality of electrically isolated pockets extending from the silicon substrate surface. Each pocket is isolated by sidewalls of amorphous silicon, formed by the bombardment of the silicon substrate with silicon ions, laterally enclosing an upper portion of the pocket and an isolating junction continuous with said sidewalls enclosing the lower portion of the pocket.

Each isolated pocket is silicon of one conductivity type, and said isolating junction is formed by a silicon region of opposite conductivity type abutting the pocket. The pockets contain regions of only said opposite conductivity type extending from the surface into the pocket but spaced from said sidewalls and isolating junctions. The structure avoids the problem of parasitic capacitances which tend to occur in completely junction isolated integrated circuits along vertical junctions. By limiting the structure to only regions of opposite conductivity type diffused into pockets of said one conductivity type, the structure avoids vertical PN junctions which are adjacent to each other and, thus, are subject to parasitic capacitance effects.

Jan. 1, 1974 K. BRACK ET AL T918,008

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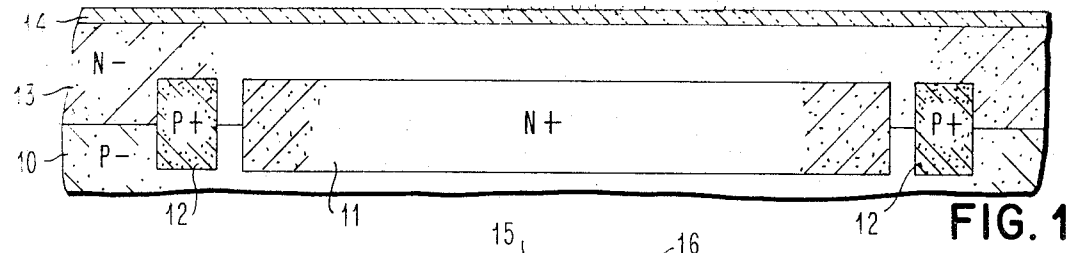


FIG. 1

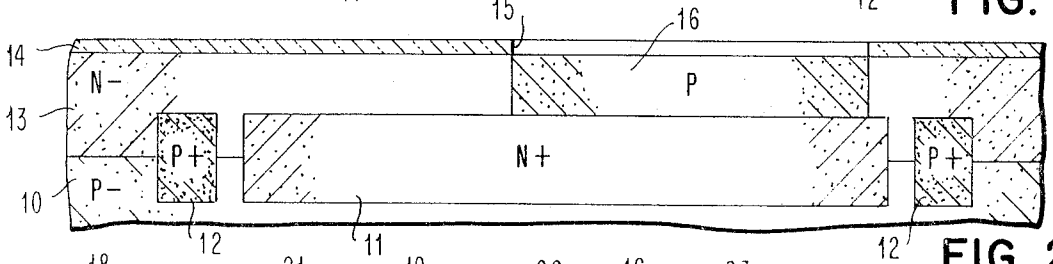


FIG. 2

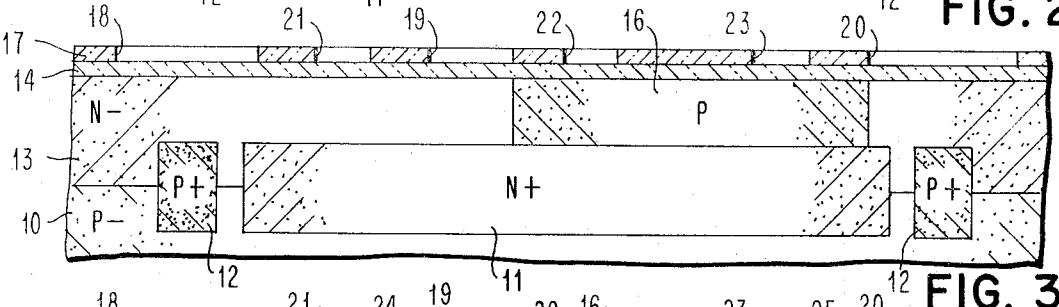


FIG. 3

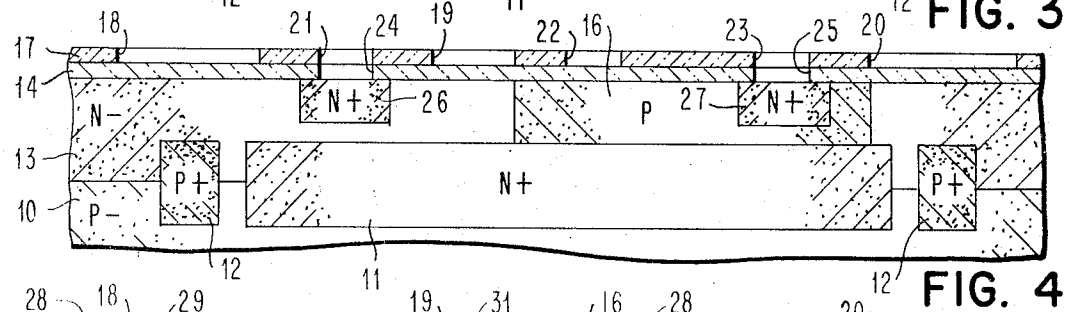


FIG. 4

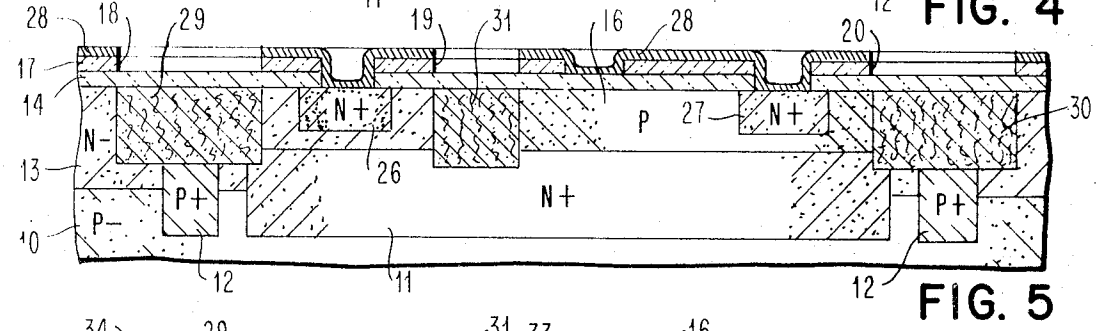


FIG. 5

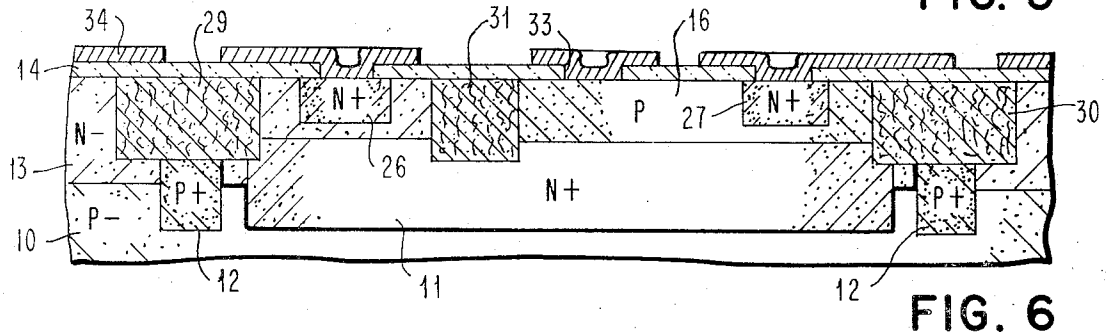


FIG. 6