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[54] **NOISE REJECTION CIRCUITRY**

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[51] **Int. Cl.** **G08b 13/24**

[58] **Field of Search** ..... 340/258 C, 280, 152 T; 343/6.5 R, 6.5 SS

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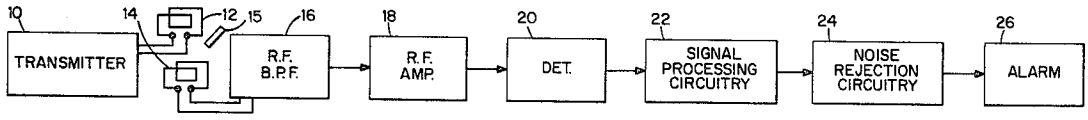
[57] **ABSTRACT**

Noise rejection circuitry sutable for detection of a resonant tag in an electronic security system especially adapted for use in retail stores. True signals are distinguished from noise by sensing the absence of one or more pulses in an expected chain of pulses produced by the resonant tag. A parallel noise inhibit function is provided by a staircase generator and comparator which prevent an alarm indication in response to received fast pulse noise.

14 Claims, 6 Drawing Figures



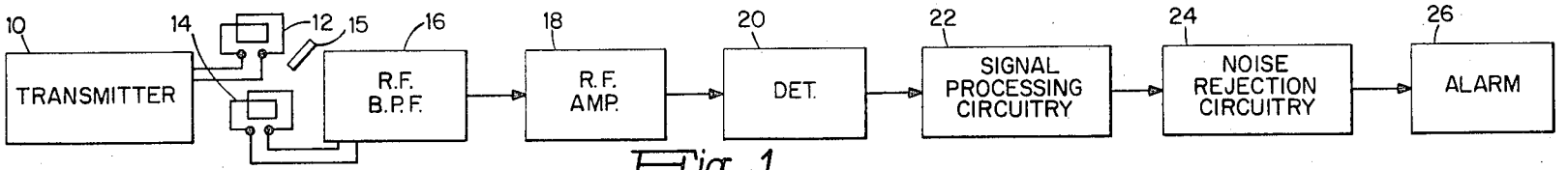


Fig. 1.

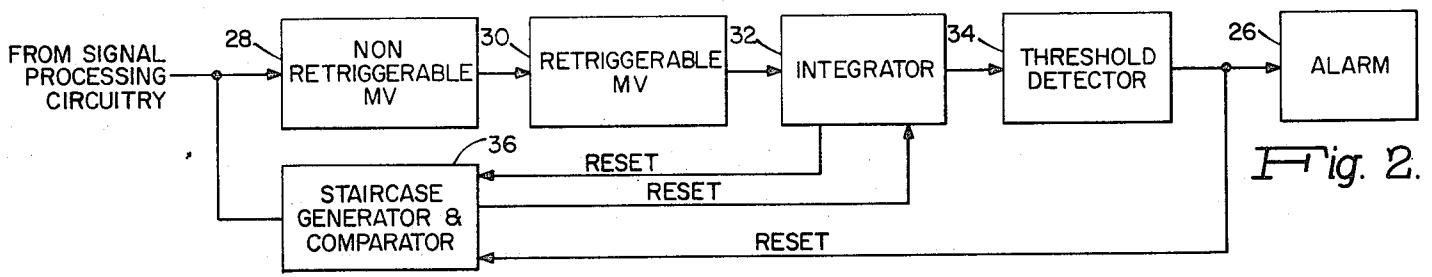


Fig. 2.

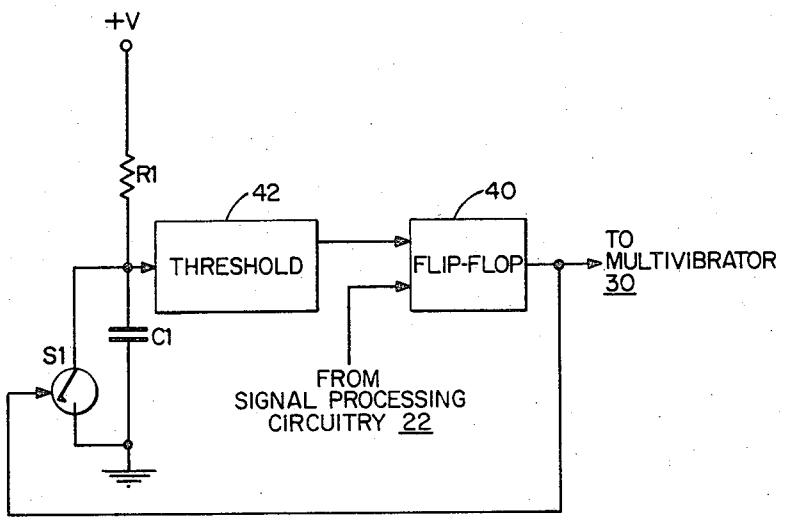


Fig. 3.

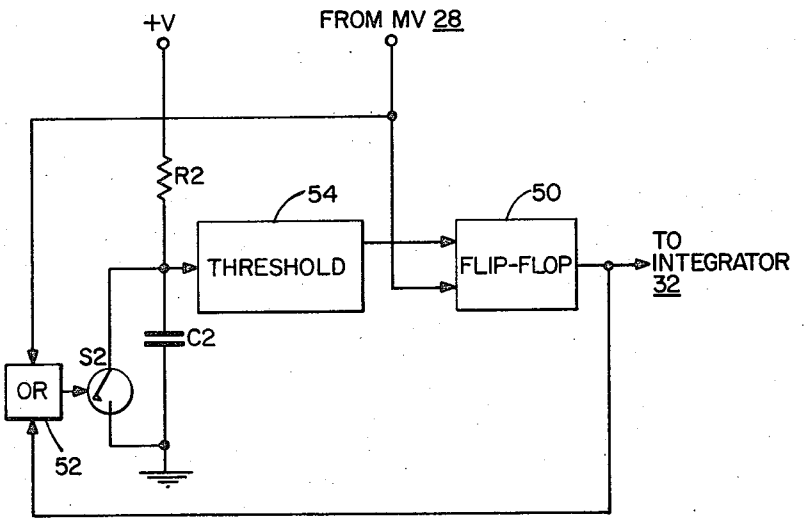


Fig. 4.

RELATIVE AMPLITUDE
A
B
C
D
E
T1
T2
T3
T2 THRESHOLD
T3 THRESHOLD

Fig. 6.

+V
R5
OUTPUT
Q2
R6
R3
C3
D1
Q1
R4
FROM MV 30
RESET

Fig. 5.

NOISE REJECTION CIRCUITRY

FIELD OF THE INVENTION

This invention relates to noise rejection circuitry and more particularly to circuitry for the reliable and rapid detection of a resonant tag circuit within a controlled area.

BACKGROUND OF THE INVENTION

Electronic security systems are known for preventing unauthorized removal of articles from an area under protection. Such systems are especially suitable for use in retail stores to prevent the theft of articles from the store and to minimize considerable losses occasioned by shoplifting. A particularly effective system is described in copending application Serial No. 214,361 wherein a multi-frequency resonant tag is provided having different frequencies for detection and deactivation. The resonant tag circuit is operative at a first frequency to permit detection by electromagnetic interrogation thereof, and is operative at a second frequency to permit deactivation thereof by an applied electromagnetic field which destroys the resonant property of the circuit at its detection frequency. The system of the copending application includes noise rejection circuitry for discriminating true signals produced by a resonant tag in the detection zone from spurious signal conditions caused by noise. This circuitry determines whether a predetermined number of pulses of selected periodicity are received within a selected time interval. If the requisite pulses are not received by the end of this interval, the circuitry is then reset to prevent false alarm actuation and to renew the detection cycle.

SUMMARY OF THE INVENTION

In accordance with the present invention, improved noise rejection circuitry is provided for an electronic security system in which an expected train of pulses of predetermined periodicity is sensed to provide an alarm indication, the circuitry being reset immediately upon detection of a missed pulse in the expected train. Pulses are derived from signals produced by a resonant tag circuit in the detection zone, and such pulses are applied to a nonretriggerable gating circuit which inhibits pulses having other than the predetermined periodicity. The output of this gating circuit is applied to a retriggerable circuit such as a multivibrator which acts as a missing pulse detector for resetting an associated integrator circuit. A staircase generator and comparator also receives the pulses derived from the tag circuit and is operative to reset the integrator in response to noise pulses occurring at rates faster than the periodicity of expected pulses. The noise rejection circuitry of the invention thus provides faster true pulse detection by resetting the integrator as soon as a missing pulse is detected, rather than awaiting termination of a timing cycle.

DESCRIPTION OF THE DRAWING

The invention will be more fully understood from the following detailed description taken in conjunction with the accompanying drawing in which:

FIG. 1 is a block diagram representation of an electronic security system in which the invention may be advantageously employed;

FIG. 2 is a block diagram representation of noise discrimination circuitry according to the invention;

FIG. 3 is a block diagram representation of the nonretriggerable monostable multivibrator of FIG. 2;

FIG. 4 is a block diagram representation of the retriggerable monostable multivibrator of FIG. 2;

FIG. 5 is a schematic representation of the integrator and threshold of FIG. 2; and

FIG. 6 is a plot of signal diagrams useful in illustrating the operation of the circuitry of FIG. 2.

DETAILED DESCRIPTION OF THE INVENTION

The noise discrimination circuit of the invention may be advantageously employed in an electronic security system such as that illustrated in FIG. 1 and which includes a transmitter 10 coupled to an antenna 12, typically a loop antenna, operative to provide an electromagnetic field within a predetermined area to be controlled. A receiving antenna 14, also typically a loop antenna, receives energy radiated by antenna 12 and is arranged for sensing of a resonant tag circuit 15 at the controlled area, coupling the received energy to an RF front-end which includes an RF band pass filter 16 and an RF amplifier 18. The output of amplifier 18 is applied to a detector 20, the output of which is, in turn, coupled to signal processing circuitry 22. The signal processing circuitry 22 can include analog noise limiting circuits such as filters to define the band of received signals to be subsequently processed. Output signals from circuitry 22 are processed by noise rejection circuitry 24 which is the subject of the present invention. The output of the noise rejection circuitry is operative to actuate an alarm 26 or other output utilization apparatus.

The noise rejection circuitry of the invention is depicted in block diagram form in FIG. 2 and includes a nonretriggerable monostable multivibrator 28 receiving pulses from signal processing circuitry 22 and which triggers a retriggerable monostable multivibrator 30. The output of multivibrator 30 is integrated by an integrator 32, this integrated output signal being applied to a threshold detector 34. If the threshold level provided by detector 34 is exceeded by the output signal from integrator 32, detector 34 provides an output signal to alarm 26 for actuation thereof. A staircase generator and comparator 36 may additionally be employed to receive pulses from signal processing circuitry 22 and to provide a reset signal to integrator 32 in response to high frequency noise, as will be described.

The nonretriggerable multivibrator 28 is illustrated more particularly in FIG. 3 and includes a flip flop 40 receiving a signal from signal processing circuitry 22 which is operative to set the flip flop in one of its operative states. The flip flop 40 also receives a reset signal from a threshold detector 42 which is driven by an input signal derived from an RC integrator comprising a resistor R1 and series connected capacitor C1 connected between a source of potential +V and a source of reference potential, typically ground. A switch S1 is connected across capacitor C1 and is operative in response to the output signal from flip flop 40 to shunt the capacitor to the reference potential.

When switch S1 is in its open condition, a voltage derived from source +V is effective to charge capacitor C1, the capacitor voltage being operative upon exceedance of a predetermined threshold voltage of thresh-

old detector 42 to cause application of a reset signal to flip flop 40. When switch S1 is in its closed condition, capacitor C1 is discharged to prevent exceedance of the threshold of detector 42 and to thereby prevent application of a reset signal to flip flop 40.

Upon receipt by flip flop 40 of a trigger pulse from signal processing circuitry 22, flip flop 40 is set to a first state typically a high state and thereby provides an output signal of a first level, typically a higher signal level, to multivibrator 30, this output signal also being operative to open switch S1 to permit charging of capacitor C1. When the voltage across capacitor C1 reaches a predetermined threshold level, detector 42 is triggered to provide a reset signal to flip flop 40 which, in turn, provides an output signal of second level, typically a lower signal level, and which is operative to close switch S1. The switch S1 is typically a solid state switch such as a transistor having its gate electrode coupled to the output of flip flop 40.

The flip flop 40 can only be triggered by alternate pulses applied to the set and reset input terminals thereof and thus cannot be retriggered until completion of the timing cycle provided by the RC integrator in relation to the threshold voltage of detector 42. Pulses received from signal processing circuitry 22 applied to the flip flop 40 during the charging cycle of the capacitor C1 are not operative to affect the state of flip flop 40 and are eliminated from subsequent processing.

The retriggerable monostable multivibrator 30 is shown more particularly in FIG. 4 and is generally similar to the multivibrator circuit of FIG. 3. A flip flop 50 receives a momentary set signal from multivibrator 28, specifically the leading edge of the received pulse, which also provides a momentary input signal via an OR gate 52 to a switch S2. The flip flop 50 receives a reset signal from a threshold detector 54 which is driven by an RC integrator network including a resistor R2 in series with a capacitor C2 and connected between a source of suitable potential +V and a source of reference potential, typically ground. The switch S2 is connected in shunt across capacitor C2 and when closed is operative to shunt the capacitor to the reference potential. The output signal from flip flop 50 is applied to integrator 32 and is also applied to an input of OR gate 52.

Upon receipt of a trigger pulse from multivibrator 28, capacitor C2 is discharged by momentary closure of switch S2 and flip flop 50 is set to its first state to provide an output signal of first, typically high, output level. The output signal of first signal level is applied via OR gate 52 to switch S2 to cause opening thereof for so long as the output signal remains at its high level and no trigger signals are received from MV 28. Thus, pulses being received from multivibrator 28 of predetermined periodicity, periodically cause S2 to close, discharging C2, and thus cause flip flop 50 to remain in its set condition to provide a continuous output signal of constant level. Received pulses from a valid tag circuit in the detection zone are predetermined to have the selected periodicity to achieve this result.

In the event that a pulse from multivibrator 28 is not received within the interval provided by the charging time constant of the integrator network, switch S2 remains open to permit the capacitor C2 to charge to its triggering level causing threshold detector 54 to provide a reset signal to flip flop 50. The flip flop provides in its reset state an output signal of second level, typically a low voltage, which signals the detection of a missed pulse. Thus, the multivibrator 30 functions as a missing pulse detector to cause resetting of the detection circuitry to prevent a spurious alarm indication of tag presence and to commence another detection cycle.

The integrator 32 and threshold detector 34 are illustrated in typical schematic form in FIG. 5. The integrator includes a resistor R3 in series with a capacitor C3, the resistor being operative to receive signals from multivibrator 30 while the capacitor is coupled to a ground or other reference potential. A diode D1 is connected with the polarity shown across resistor R3. A switching device, typically a transistor Q1, is connected with the collector connected to the junction between resistor R3 and capacitor C3 and the emitter connected to ground or reference potential. A bias resistor R4 is connected between the base and emitter electrodes of transistor Q1, and the base electrode is also operative to receive a reset signal from the staircase generator (FIG. 2).

The threshold detector includes a voltage divider network including a resistor R5 connected from a source of potential +V to the source electrode of a unijunction transistor Q2, the drain electrode of which is connected via a resistor R6 to ground or other reference potential. The gate electrode of transistor Q2 is connected to the junction between capacitor C3 and resistor R3. An output signal is coupled from the source electrode of transistor Q2. It will be appreciated that if an output signal of opposite polarity is desired, such output can be derived from the drain electrode of transistor Q2.

In response to the output from multivibrator 30 of high signal level, capacitor C3 charges via resistor R3 to a reference potential at which transistor Q2 is triggered to its conductive state to provide an output signal at the output terminal thereof for alarm actuation. The diode D1 is reverse biased by the voltage across resistor R3. If multivibrator 30 (FIG. 2) is reset to provide an output voltage of lower level, capacitor C3 will discharge through diode D1 and thus the voltage across capacitor C3 will be at the lower voltage level then being provided by multivibrator 30, and which is chosen to be below the threshold level at which transistor Q2 becomes conductive. As a result, no output signal appears from the threshold detector and no alarm is produced. The integrator 32 can also be reset from pulses provided from staircase generator and comparator 36 to prevent triggering of transistor Q2 which could provide spurious output signals. Upon receipt of a reset signal, transistor Q1 is caused to conduct and thus shunt capacitor C3 to ground or other reference potential. The capacitor C3 is thereby discharged during the interval of the reset signal to delay actuation of transistor Q2 and the resulting output signal for alarm actuation.

Staircase generator and comparator 36, which may be employed in the invention, is operative to apply a reset signal to integrator 32. In response to trigger pulses from signal processing circuitry 22, the staircase generator produces a staircase voltage which rises during the duration of each pulse from circuitry 22. The comparator contains a threshold circuit and upon exceedance of a predetermined threshold level by the staircase signal, an output pulse is produced to reset integrator 32, and also to reset the staircase generator itself. In addition, the staircase generator may be reset by

a signal from the integrator 32 or from threshold detector 34 to permit proper processing of subsequently received pulses. The voltage characteristics of the staircase generator are determined such that the staircase generator threshold requires a greater number of pulses to produce a reset signal than does the integrator to produce an alarm signal.

The operation of the circuit in FIG. 2 will be described in conjunction with the signal diagrams of FIG. 6. The pulses from the tag sensing circuitry, such as from circuitry 22 of FIG. 1, are depicted in FIG. 6A. These pulses are applied to the nonretriggerable monostable multivibrator 28, which has a period T1 slightly less than the period of the modulation rate. The leading edge of T1 triggers multivibrator 30 while multivibrator 28 is operative to inhibit spurious input signals from triggering multivibrator 30 at a rate faster than that of the expected signal, as illustrated in FIG. 6B.

Multivibrator 30 is a retriggerable monostable multivibrator with a normal timing period T2 slightly greater than the period of the expected signals. Each time multivibrator 30 receives a trigger pulse from multivibrator 28, multivibrator 30 is reset to its initial timing state and remains in its high voltage output state for a period T2 seconds after the last trigger pulse. FIG. 6C illustrates the output of multivibrator 30 provided that the trigger pulses occur with a period less than T2. The timing capacitor C2 voltage is depicted in FIG. 6D. As long as the capacitor voltage is discharged prior to exceeding the threshold voltage, multivibrator 30 will remain in its high voltage state.

As long as multivibrator 30 is in its high voltage state, the output voltage will be applied to the integrator and will generate a ramp signal from the integrator, as shown in FIG. 6E. If the integrator output voltage exceeds the threshold level, the alarm will be actuated. However, if multivibrator 30 should return to its low voltage state prior to time T3, the integration time of integrator 32, the integrator will be reset thereby preventing the threshold voltage from being exceeded and preventing alarm actuation.

Thus, the alarm can be actuated only if multivibrator 30 receives a continuous stream of trigger pulses with a period t, where $T1 < t < T2$, and where these pulses arrive continuously for a time period greater than T3. In the system shown in FIG. 2, the first pulse that is "missed" by multivibrator 30 will reset the entire system. Alternatively, multivibrator 30 may be modified so that more than one pulse must be "missed" before the integrator will be reset.

A major advantage of the circuitry of the invention is the provision of immediate reset of the pulse integrator upon detection of a missing pulse. For example, if the detection system receives noise signals just prior to the detection of an actual resonant tag, the system will reset itself immediately upon cessation of the spurious signal and will immediately begin integration of real pulses for alarm actuation. Additionally, by detecting missing pulses in a train of expected pulses of predetermined periodicity, the integration period of the circuitry is not related to the reset speed of the detector. Thus, a longer integration period may be used to increase noise rejection without thereby decreasing the reset speed of the detector upon receipt of spurious signals. Furthermore, variation in the integration period due to possible imperfections or changes in the circuit elements over time cannot render the detector inoperative such as if the reset period were shorter. In the circuitry of the invention, the primary reset function is independent of the integration period and will permit detection notwithstanding variation in the integration period.

It should be apparent that the invention can be implemented by various circuits other than those disclosed to accomplish the intended purpose. Accordingly, it is not intended to limit the invention by what has been particularly shown and described except as indicated in the appended claims.

What is claimed is:

1. For use in an electronic security system which includes means for providing in a surveillance zone an electromagnetic field of a frequency which is swept within a predetermined range, and means for detecting the presence of a resonant tag circuit having a frequency within said range, circuitry for discriminating between the presence of a valid tag circuit in said surveillance zone and spurious signals, said circuitry comprising:
   - means for receiving a train of pulses derived from detection of a tag circuit within said surveillance zone;
   - means operative upon receipt of a predetermined number of pulses of predetermined periodicity to provide an alarm indication; and
   - means for resetting said circuitry immediately upon detection of at least one missed pulse in the expected train of pulses.

2. A circuit according to claim 1 including
   - staircase generating means operative in response to the output pulses from said detecting means to generate a staircase signal which increases in amplitude; and
   - means for providing a reset signal to said circuitry upon the exceedance by said staircase signal of a predetermined threshold level.

3. For use in an electronic security system which includes means for providing in a surveillance zone an electromagnetic field of a frequency which is swept within a predetermined range, and means for detecting the presence of a resonant tag circuit having a resonant frequency within said range and for providing pulses in response thereto, noise rejection circuitry for distinguishing between pulses provided by said tag circuit and pulses caused by spurious conditions, said noise rejection circuitry comprising:
   - a nonretriggerable gating circuit receiving pulses from said detecting means and operative to provide output pulses in response to received pulses of predetermined periodicity;
   - a retriggerable circuit operative in response to the output pulses from said nonretriggerable gating circuit;
   - integrator means operative in response to the output pulses from said retriggerable circuit to provide an integrated signal; and
   - threshold detector means having a predetermined threshold level and operative to provide an output signal for alarm actuation upon exceedance of said threshold level by said integrated signal.

4. Noise rejection circuitry according to claim 3 and including:
   - staircase generating means operative in response to the output pulses from said detecting means to generate a staircase signal which increases in ampli-

tude in the presence of each of said output pulses and operative to provide a reset signal upon the exceedance by said staircase signal of a predetermined threshold level.

5. Noise rejection circuitry according to claim **3** wherein said retriggerable circuit provides output signal of first or second signal state to said integrator means.

6. Noise rejection circuitry according to claim **3** wherein said retriggerable circuit provides an output signal of first voltage level in response to a continuous train of pulses of predetermined periodicity from said nonretriggerable gating circuit, and provides an output signal of second voltage level in response to the absence of at least one pulse in said train of pulses.

7. Noise rejection circuitry according to claim **6** wherein said integrator means includes

means operative in response to said output signal of first voltage level to provide an integrated output signal for alarm actuation; and

means response to said output signal of second voltage level to reset said integrator.

8. Noise rejection circuitry according to claim **7** wherein said first voltage level is greater than said second voltage level.

9. Noise rejection circuitry according to claim **3** wherein said nonretriggerable gating circuit and said retriggerable circuit are each multivibrators.

10. Noise rejection circuitry according to claim **3** wherein said nonretriggerable gating circuit includes

an RC circuit;

a threshold detector operative in response to a predetermined voltage on the capacitor of said RC circuit; and

a flip flop operative to receive trigger pulses from said tag circuit and a reset signal from said threshold detector and to provide an output signal to said retriggerable circuit upon receipt of said trigger pulses.

11. Noise rejection circuitry according to claim **3** wherein said retriggerable circuit includes

a flip flop;

an RC circuit;

a switch operative to control the charging of the capacitor in said RC circuit; and

a threshold detector operative to provide a reset signal to said flip flop in response to a predetermined voltage level across said capacitor;

means for simultaneously providing from said nonretriggerable gating circuit a set signal to said flip flop and an input signal to said switch;

said switch being operative in response to said input signal to ground said capacitor and thereby prevent said threshold detector from providing a reset signal to said flip flop for a period of time greater than the minimum interval between pulses received from said nonretriggerable gating circuit.

12. Noise rejection circuitry according to claim **7** wherein said integrator means includes:

an RC circuit driven by the output voltage of said retriggerable circuit;

solid state gating means operative to provide an output signal for alarm actuation in response to a predetermined voltage; and

diode means conductive in response to signals from said retriggerable circuit of said lower voltage level and operative to prevent the voltage across the capacitor in said RC circuit from reaching a voltage required to activate said solid state gating means.

13. An electronic security system comprising

transmitter means for providing an electromagnetic field in a surveillance zone at a frequency repetitively swept through a predetermined range;

a multi-resonant tag circuit having a first resonant frequency within said predetermined range of frequencies and a second resonant frequency outside of said predetermined range of frequencies;

receiver means for detecting the presence of said first resonant frequency from a tag circuit present in said surveillance zone;

said receiver means including

detector means operative to provide output pulses in response to the presence of the first resonant frequency of said tag circuit in said electromagnetic field;

noise rejection circuitry operative in response to pulses from said detector means for distinguishing between pulses provided by said tag circuit and pulses caused by spurious conditions, said circuitry comprising:

means for receiving a train of pulses derived from detection of a tag circuit within said surveillance zone;

means operative upon receipt of a predetermined number of pulses of predetermined periodicity to provide an alarm indication; and

means for resetting said circuitry immediately upon detection of at least one missed pulse in the expected train of pulses.

14. An electronic security system according to claim **13** wherein

said means operative upon receipt of a predetermined number of pulses of predetermined periodicity includes

integrator means for providing an integrated output signal in response to said pulses of predetermined periodicity; and

threshold detector means operative to provide an output signal upon receipt of an integrated output signal of predetermined magnitude;

and wherein said resetting means includes

a retriggerable circuit operative to receive pulses having a predetermined minimum period and to provide an output voltage of a first voltage level to said integrator means in response to a continuous train of pulses having less than a predetermined period and to provide an output voltage of a second voltage level to said integrator means in response to a missed pulse.

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