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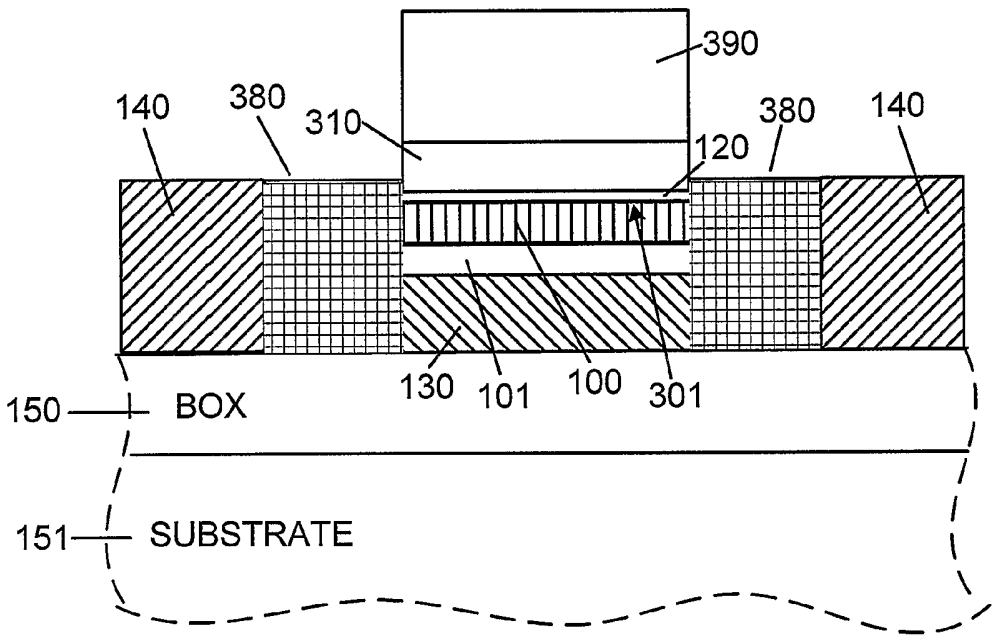
(54) Title: INTEGRATION OF STRAINED GE INTO ADVANCED CMOS TECHNOLOGY



(57) Abstract: A structure and method of fabrication for PMOS devices in a compressively strained Ge layer is disclosed. The fabrication method of such devices is compatible with standard CMOS technology and it is fully scalable. The processing includes selective epitaxial depositions of an over 50% Ge content buffer layer, a pure Ge layer, and a SiGe top layer. Fabricated buried channel PMOS devices hosted in the compressively strained Ge layer show superior device characteristics relative to similar Si devices.

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INTEGRATION OF STRAINED Ge INTO ADVANCED CMOS TECHNOLOGY

FIELD OF THE INVENTION

The present invention relates to semiconductor technology and, more specifically, to a PMOS device hosted in strained Ge. This device is fabricated in a manner that it can be effectively scaled and integrated into high performance silicon based CMOS technologies.

BACKGROUND OF THE INVENTION

Today's integrated circuits include a vast number of devices. Smaller devices are key to enhance performance and to improve reliability. As MOSFET (Metal Oxide Semiconductor Field- Effect- Transistor, a name with historic connotations meaning in general an insulated gate Field- Effect- Transistor) devices are being scaled down, the technology becomes more complex and new methods are needed to maintain the expected performance enhancement from one generation of devices to the next.

One of the most important indicators of potential device performance is the carrier mobility. There is great difficulty in keeping carrier mobility high in devices of deeply submicron generations. A promising avenue toward better carrier mobility is to modify the semiconductor that serves as raw material for device fabrication. It has been known, and recently further studied, that tensilely or compressively straining semiconductors have intriguing carrier properties. In particular, a 90-95% improvement in the electron mobility has been achieved in a strained silicon (Si) channel NMOS as described in U.S. Patent No.

6,649,492 B2 to J.O. Chu entitled "Strained Si Based Layer Made By UHV-CVD, and Devices Therein" incorporated herein by reference. Similarly for hole enhancement, compressively-strained buried germanium (Ge) MODFETs have yielded high hole mobilities as described by S.J. Koester, et. al. in "Extremely high transconductance $Ge/Si_{0.4}Ge_{0.6}$ p-MODFET's grown by UHV-CVD, " IEEE Elect. Dev. Lett. 21, 110 (2000). Combination of tensilely and compressively strained SiGe regions in the same wafer is described in PCT patent application "Dual Strain-State SiGe Layers for Microelectronics" by J.O. Chu, Ser. No. PCT/US2004/005481, published WO2004084264 on 09/30/2004.

Because of its enhanced hole mobility there is renewed technological interest in Ge-based MOSFET devices for high performance CMOS logic. In particular, surface channel Ge MOSFET devices, using oxynitride (GeON) as the gate insulator, have been demonstrated by H. Shang et al, IEDM, p. 441, 2002 . Or, using high-K as the gate insulator, Ge PMOS is described in the following references: C. Chui et al, IEDM, p. 437, 2002, C.H. Huang et al, VLSI symp. p. 119, 2003 and A. Ritenour et al, IEDM, p. 433, 2003 all three of which are incorporated herein by reference.

Buried channel strained Ge PMOS have also been reported having hole mobility enhancement as described in the following references of M. Lee et al, IEDM, p. 429 2003 and H. Shang et al, VLSI symp. 2004 both of which are incorporated herein by reference. Nonetheless, the Ge devices reported have employed simple device structures, such as ring type gate structure lay-out for simplified integration, and usually have relative large dimensions. Such features are not or suitable for integration into advanced high performance CMOS technologies.

A process compatible with standard CMOS technology, in order to incorporate strained Ge structures for enhanced hole mobility in PMOS devices, is not available.

SUMMARY OF THE INVENTION

This invention describes an integration scheme for advanced CMOS technology which incorporates a high mobility strained Ge buried channel structure, leading to PMOS device improvement. The scheme is readily scalable with decreasing dimensions.

A layered structure, including a SiGe seed layer, wherein the SiGe seed layer is monocrystalline and has about between 50% and 90% of Ge concentration, and a compressively strained Ge layer covering the SiGe seed layer, wherein the compressively strained Ge layer is monocrystalline and in epitaxial relation with the SiGe seed layer is disclosed.

A CMOS circuit, including a PMOS device hosted in a compressively strained Ge layer, wherein the compressively strained Ge layer is covering in epitaxial relation a SiGe seed layer, wherein the SiGe seed layer is monocrystalline and has about between 50% and 90% of Ge concentration is further disclosed.

A method for fabricating a PMOS device, including the steps of depositing epitaxially a monocrystalline SiGe seed layer having about between 50% and 90% of Ge concentration over a relaxed SiGe layer having about up to 50% of Ge concentration; depositing epitaxially a compressively strained Ge layer over the SiGe seed layer; and hosting the PMOS device in the compressively strained Ge layer is further disclosed.

A method for fabricating a CMOS circuit, including the steps of providing an SGOI wafer having a relaxed SiGe layer with about up to 50% of Ge concentration; using a shallow trench, or other, isolation technique to define NMOS and PMOS regions on the SGOI wafer; capping with a dielectric material the NMOS regions; depositing epitaxially and in a selective manner a monocrystalline SiGe seed layer having about between 50%

and 90% of Ge concentration over the relaxed SiGe layer; depositing epitaxially and in a selective manner a compressively strained Ge layer over the SiGe seed layer; and hosting a PMOS device in the compressively strained Ge layer is further disclosed. The method for fabricating a CMOS circuit further including the step of depositing epitaxially and selectively a SiGe top layer over the compressively strained Ge layer, wherein the SiGe top layer is chosen to have about up to 10% of Ge concentration is further disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the present invention will become apparent from the accompanying detailed description and drawings, wherein:

Fig. 1 shows a schematic cross sectional view of a layered structure used for fabricating devices;

Fig. 2 shows a schematic top view of isolation and NMOS and PMOS regions;

Fig. 3 shows a schematic cross sectional view of a buried channel PMOS device hosted in a compressively strained Ge layer;

Fig. 4 shows a plot of measured mobility values for a buried channel PMOS device hosted in a compressively strained Ge layer;

Fig. 5 shows a plot of measured transconductance values for a buried channel PMOS device hosted in a compressively strained Ge layer; and

Fig. 6 shows a measured conduction plot for a buried channel PMOS device hosted in a compressively strained Ge layer.

DETAILED DESCRIPTION OF THE INVENTION

In the integration of strained Ge into advanced CMOS technology it is preferable to maintain the overall standard fabrication process of mainline Si CMOS as much as feasible. This invention integrates compressively strained Ge into such a process with changing/adding only a few steps out of the well over a hundred steps of typical advanced Si CMOS processing. In an exemplary embodiment the overall process flow of CMOS fabrication, including the strained Ge hosted PMOS, would follow these steps: Start with a silicon-on-insulator (SOI) or silicon-germanium-on-insulator (SGOI) wafer; go through the standard shallow trench isolation (STI) process, as known to one skilled in the art; cap NMOS region with a mask; open up Si or SiGe islands only in PMOS region; grow selectively Ge on top of exposed Si or SiGe surface; strip masking cap on NFET region; continue with the standard CMOS fabrication as known to one skilled in the art. This invention also teaches steps and structures which are novel outside the framework of CMOS fabrication process.

Fig. 1 shows a schematic cross sectional view of a layered structure used for fabricating devices. Fig. 2 shows a schematic top view of isolation and NMOS and PMOS regions. In a representative embodiment the starting point is a SOI or SGOI wafer. A substrate 151, which is usually Si, has a so called buried oxide (BOX) 150 on over it, as known to one skilled in the art. On top of the BOX there is a relaxed monocrystalline SiGe layer 130 typically with about up to 50% of Ge concentration, with the possibility of being essentially pure Si. At the start this relaxed SiGe is a blanket layer on top of the BOX 150, but Fig. 1 shows a state of processing where an isolation dielectric 140 has already been applied and the relaxed SiGe layer 130 is fragmented. The isolation in an exemplary

embodiment is so called shallow trench isolation (STI), but it could be of other various kinds as known to one skilled in the art. The isolation 140 separates, or defines, regions designated for PMOS devices 210 from regions designated for NMOS devices 220. Preferably the strained Ge layer introduced in this invention is used for the PMOS devices in the PMOS regions 210. The NMOS regions are handled in ways known to one skilled in the art, possibly with material layers 190 over the relaxed SiGe 130. Layer, or layers, 190 in the NMOS region are shown only symbolically, since layer 190 may not even exist at this stage of the process, or may never be implemented. The present invention uses methods known in the art in the processing of the NFET regions and devices. At this stage, as represented in the figures, the NMOS regions are covered with a mask 160. Mask 160 preferably is a dielectric, such as SiO_2, or nitride, or others, as known to one skilled in the art.

Introduction of the layers for the Ge hole-conduction type device, such as a PMOS, or P-MODFET, commences with depositing epitaxially a monocrystalline SiGe seed layer 101 having about between 50% and 90% of Ge concentration over the relaxed SiGe layer 130. Preferably the epitaxial growth of the SiGe seed layer 101 is done in a selective manner, and with a Ge concentration of around 70%. Selectivity in deposition is with regard to dielectric materials, such as the STI dielectric 140, or the NMOS mask 160. The Ge concentration in this SiGe seed layer 101 is not necessarily uniform, it can have various Ge concentration gradients depending on requirements of a specific embodiment. Non-uniform concentration typically serves the purpose of improving material quality. The preferred thickness range for this SiGe seed layer 101 is about between 0.3nm and 3nm. Some of the preference for this SiGe seed layer 101 is to improve the surface quality of the relaxed SiGe 130 of the SGOI wafer. The relatively high Ge concentration of the SiGe

seed layer is an enabling aspect for the introduction of the compressively strained device quality Ge layer 100.

The compressively strained monocrystalline Ge layer 100 is deposited epitaxially over the SiGe seed layer 101. Preferably the epitaxial growth of the compressively strained Ge layer 100 is done in a selective manner. Selectivity in deposition is with regard to dielectric materials, such as the STI dielectric 140, or the NMOS mask 160. The preferred thickness range for this compressively strained Ge layer 100 is about between 5nm and 20nm. The Ge layer 100 is compressively strained because the relaxed lattice constant of Ge is larger than that of SiGe, and the epitaxial relationship through the layers forces the lattice of Ge layer 100 to comply with the layers underneath, all of which have smaller relaxed lattice constants than Ge. The compressively strained Ge layer is the one hosting a hole-type conduction device, such as a PMOS. The term of hosting a device in a certain material, or layer, means that the critical part of the device, that which is mainly sensitive to carrier properties, such as for instance, the channel of a MOS device, is residing in, composed of, housed in, in that certain material, or layer.

If one would prefer a surface channel PMOS device the material depositions could stop with the compressively strained Ge layer 100. For having a buried channel PMOS, as well as to preferably improve the interface qualities of the p-channel, a monocrystalline SiGe top layer 120 is epitaxially deposited covering the compressively strained Ge layer 100. The SiGe top layer 120 has about up to 10% of Ge concentration. In an exemplary embodiment this SiGe top layer is essentially pure Si, in which case a thickness of about between 0.3nm and 10nm is preferred. Preferably the epitaxial growth of the SiGe top layer 120 is done in a selective manner. Selectivity in deposition is with regard to dielectric materials, such as the STI dielectric 140, or the NMOS mask 160. Either the SiGe top layer

120, or the compressively strained Ge layer 100 is the last layer to be deposited, this layered structure has a well defined top surface 121. It is preferable for easy of processing that this surface 121 be coplanar with the top surface 141 of the isolating dielectric. However, lack of such coplanarity would not be a limiting factor.

The localized formation or growth of the buried Ge channel heterostucture within the selected confines of the PMOS regions entails using a selective CVD growth process whereby the growth of the device layers are selective to the known dielectric materials of SiO_2, Si_3N_4, SiON etc. Typical, or available selective growth processes for Si, SiGe and Ge films can be found in various growth techniques such as RT-CVD, UHV-CVD, LP-CVD, AP-CVD, etc. as known to one skilled in the art. In the preferred selective growth process of ultra-high-vacuum-chemical-vapor-deposition (UHV-CVD), the growth temperature for the SiGe seed layer 101 and the compressively strained Ge layer is the range of 250 – 350 °C.

For a detailed description of the UHV-CVD technique for growing epitaxial layers, reference is made to U.S. Patent No. 5, 259,918 "Heteroepitaxial Growth of Germanium on Silicon by UHV/CVD" to S. Akbar et al, issued 11/09/1993 assigned to the assignee herein and incorporated herein by reference. More UHV-CVD growth techniques are discussed in U.S. Patent No. US 6,350,993 B1 "High Speed Composite p-Channel Si/SiGe Heterostructure for Field Effect Devices" to J. O. Chu et al, issued on 02/26/2003 assigned to the assignee herein and incorporated herein by reference. Epitaxial depositions for the layered structure of the SiGe seed layer 101, the compressively strained Ge layer 100, and the SiGe top layer 120 are done with ultrahigh vacuum integrity: in the range of about 10^{-9} Torr prior to the epitaxial deposition. In particular, a hot wall isothermal CVD apparatus is utilized whereby essentially no homogeneous gas phase pyrolysis of the

silicon and/or germanium precursor such as silene (SiH_4) or germane (GeH_4) source gas occurs during the residence time, which is less than 1 second, within the selected temperature and pressure regime where the preferred growth process is operated. Typically, a batch of pre-patterned SGOI wafers are loaded in the UHV-CVD reactor and then heated in the range from 300 °C to 480 °C. The growth pressure typically is in the in range from 1 – 5 millitorr. The SiGe seed layer 101 in a representative embodiment is grown over the SGOI region using a flow combination of SiH_4 at 25 sccm and of GeH_4 at 95 sccm. To grow the compressively strained Ge layer 100, the growth temperature is lowered close to 300 °C and then the GeH_4 is turned on at a flow of 50sccm. After the completion of layer 100, the growth temperature is raised higher, and the SiH_4 is turned on at a flow of 30sccm, and the GeH_4 is turned on at a flow of 0 to 15sccm to form the thin SiGe top layer 120 over the compressively strained Ge layer 100. The thin top layer 120 in an exemplary embodiment is essentially pure Si.

Typically, but not necessarily, as known to one skilled in the art, selective CVD growth techniques prefer additional use of a chlorine based precursor or gas source, such as HCl, Cl_2, $SiCl_4$, $SiHCl_3$, SiH_2Cl_2 to induce the selective growth by removing any film growth over the standard masking materials.

Fig. 3 shows a schematic cross sectional view of a buried channel PMOS device hosted in a compressively strained Ge layer 100. Following the building up of the layered structure in Fig. 1, the device fabrication follows steps known to one skilled in the art. At one point source/drain junctions 380 are being created. The source/drain 380 as shown in the figure extend downward touching the BOX layer 150. This is only an illustration, in an exemplary embodiment the source/drain 380 may, or may not, reach down to the BOX layer interface 150, or may even happen that it penetrates into the BOX layer 150. At

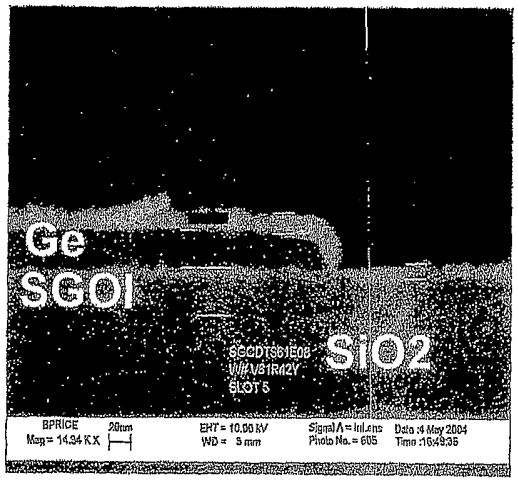
another point in the process a gate insulator 310 is employed. Preferred gate insulators are, but not limited to, a deposited oxide, typically by a plasma low temperature process, and so called high-K (high dielectric) materials, such as HfO_2, HfSiO, and others known to one skilled in the art. Similarly, a large variety of materials can be employed for the gate 390, as known to one skilled in the art. In further fabrication of the devices, such as during processing of the gate insulator 310, one may, or may not, consume from the Si/SiGe top layer 120. For illustration, the figure shows schematically a slight consumption of layer 120. Holes are conducted in a channel on the top surface 301 of the compressively strained Ge layer 100, which is the interface with the Si or SiGe top layer 120. The channel forms here due to the well known bandgap alignment between Ge and Si.

Fig. 4 shows a plot of measured mobility values for a buried channel PMOS device hosted in a compressively strained Ge layer as function of inversion charge. The maximum hole mobility in the disclosed device is over six times the Si universal hole mobility, which is also shown for comparison.

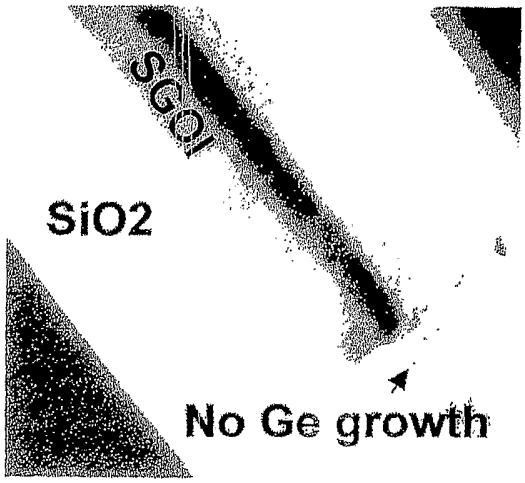
Fig. 5 shows a plot of measured transconductance values for a buried channel PMOS device hosted in a compressively strained Ge layer. The displayed characteristics is from a device with a deposited oxide gate insulator. As shown, the transconductance of the disclosed device is enhanced over that of a Si device by over a factor of two.

Fig. 6 shows a measured conduction plot for a buried channel PMOS device hosted in a compressively strained Ge layer. Subthreshold and conduction characteristics of buried channel PMOS with high-K, specifically HfO_2 gate insulator are shown for low and high drain voltage. A Si control device with the same HfO_2 as gate insulator is shown for comparison. The s-Ge (strained-Ge) device shows over two times enhancement in drive current.

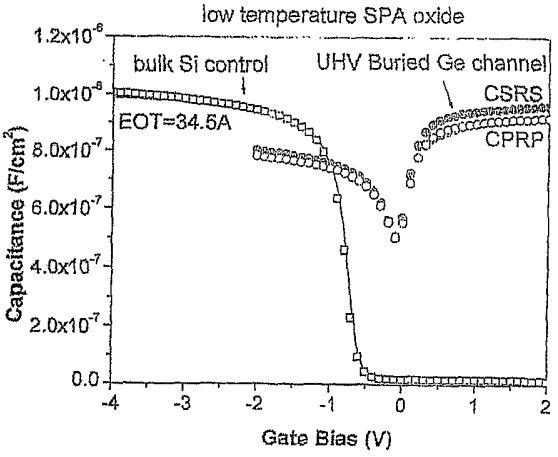
Many modifications and variations of the present invention are possible in light of the above teachings, and could be apparent for those skilled in the art. The scope of the invention is defined by the appended claims.



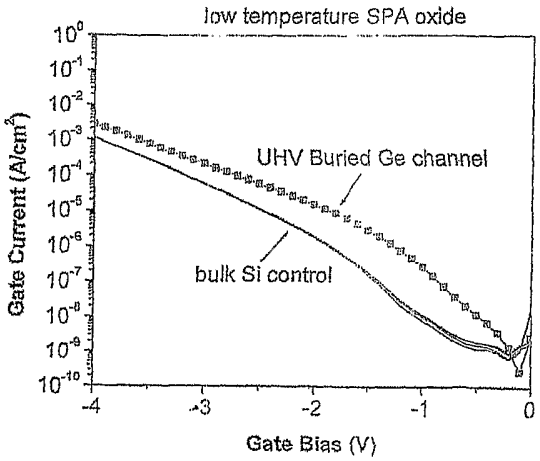
x-SEM image shows Ge layer is selectively grown on top of SGOI only, while no Ge growth is found on top of STI regions.



TEM image shows Ge layer is selectively grown on top of SGOI only, while no Ge growth is found on top of STI regions.



C-V characterixtics of low temperature SPA oxide formed at 500C with low Dit on both Si substrate and buried strained Ge substrate. This technique is the key to the demonstration of strained Ge buried channel high performance MOSFETs.



I-V characterixtics of low temperature SPA oxide formed at 500C with low Dit on both Si substrate and buried strained Ge substrate. Comparable leakage charateristics is achieved on both substrate.

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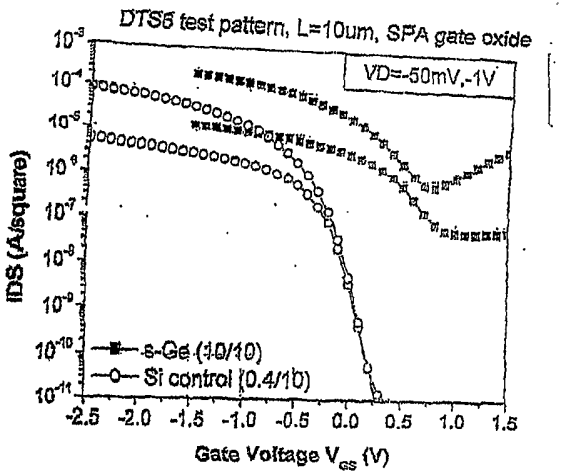
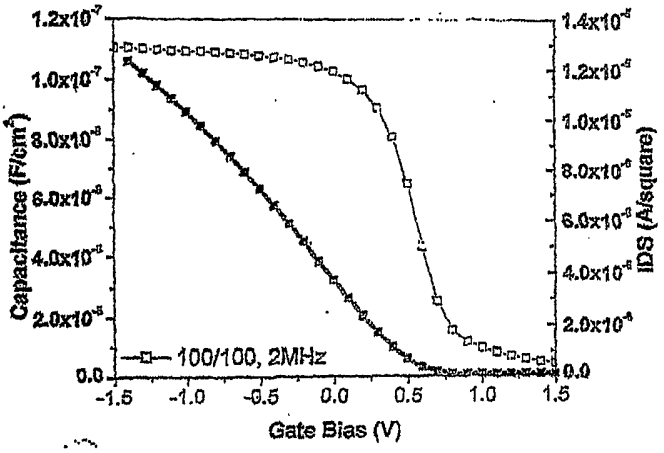
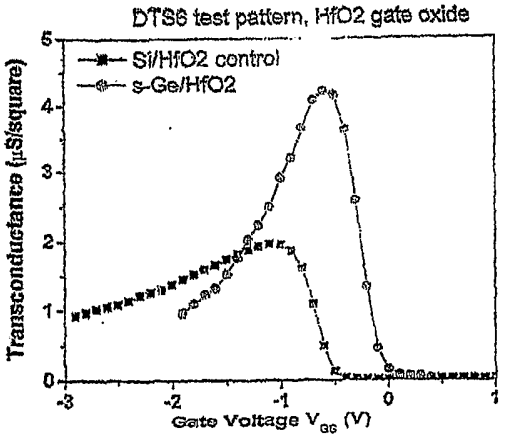


Substhreshold characteristics of PMOSFETs on both selectively formed strained-Ge buried channel substrate and Si control with STI isolation. >2X drive current enhancement is achieved. The higher off current is probably defect related.



Linear drive current and inversion capacitance measured on strained Ge buried channel PMOSFETs, which are used for effective mobility extraction.



Linear transconductance characteristics of strained Ge buried channel PMOSFETs with HfO2 gate dielectric. Si control devices with the same HfO2 is shown for comparison. S-Ge show ~2X enhancement in transconductance..

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WE CLAIM:

1. A layered structure, comprising:

a SiGe seed layer [101], wherein said SiGe seed layer is monocrystalline and has about between 50% and 90% of Ge concentration; and

a compressively strained Ge layer [100] covering said SiGe seed layer [101], wherein said compressively strained Ge layer is monocrystalline and in epitaxial relation with said SiGe seed layer.

2. The layered structure of claim 1, wherein said compressively strained Ge layer [100] is about between 5nm and 20nm thick.

3. The layered structure of claim 1, wherein said SiGe seed layer [101] is about between 0.3nm and 3nm thick.

4. The layered structure of claim 3, wherein the Ge in said SiGe seed layer [101] has a concentration gradient.

5. The layered structure of claim 1, further comprising a relaxed SiGe layer [130] underneath said SiGe seed layer [101], wherein said relaxed SiGe layer is monocrystalline and in epitaxial relation with said SiGe seed layer, and wherein said relaxed SiGe layer has about up to 50% of Ge concentration.

6. The layered structure of claim 1, further comprising a SiGe top layer [120] covering said compressively strained Ge layer [100], wherein said SiGe top layer is monocrystalline and in epitaxial relation with said compressively strained Ge layer, and wherein said SiGe top layer has about up to 10% of Ge concentration.

7. The layered structure of claim 6, wherein said SiGe top layer [120] is essentially pure Si having a thickness of about between 0.3nm and 10nm.

8. The layered structure of claim 1, wherein said layered structure is surrounded by a dielectric [140], wherein said dielectric provides isolation for said layered structure.

9. The layered structure of claim 1, wherein said layered structure and said isolating dielectric [140] have coplanar top surfaces [121, 141].

10. The layered structure of claim 1, further comprising a hole conduction type device hosted in said compressively strained Ge layer [100] .

11. The layered structure of claim 10, wherein said hole conduction type device is a PMOS [210] device.

12. The layered structure of claim 11, wherein said PMOS [210] device is a buried channel PMOS device.

13. The layered structure of claim 10, wherein a gate insulator [310] for said PMOS device comprises a high-K material.

14. The layered structure of claim 10, wherein a gate insulator [310] for said PMOS device comprises a deposited oxide.

15. A CMOS circuit, comprising:

a PMOS [210] device hosted in a compressively strained Ge layer [100], wherein said compressively strained Ge layer is covering in epitaxial relation a SiGe seed layer [101], wherein said SiGe seed layer is monocrystalline and has about between 50% and 90% of Ge concentration.

16. The CMOS circuit of claim 15, wherein said compressively strained Ge layer [100] is covered by a SiGe top layer [120], wherein said SiGe top layer is monocrystalline and in epitaxial relation with said compressively strained Ge layer, wherein said SiGe top layer has about up to 10% of Ge concentration, and wherein said SiGe seed layer [101] has underneath thereof a relaxed SiGe layer [130], wherein said relaxed SiGe layer is monocrystalline and in epitaxial relation with said SiGe seed layer, and wherein said relaxed SiGe layer has about up to 50% of Ge concentration.

17. The CMOS circuit of claim 16, wherein said SiGe top layer [120] is essentially pure Si having a thickness of about between 0.3nm and 10nm.

18. The CMOS circuit of claim 16, wherein said PMOS device is a buried channel PMOS device.

19. The CMOS circuit of claim 18, wherein said PMOS device has a gate insulator [310] and said gate insulator comprises a high-K material.

20. The CMOS circuit of claim 18, wherein said PMOS device has a gate insulator [310] and said gate insulator comprises a deposited oxide.

21. A method for fabricating a PMOS device, comprising the steps of:

depositing epitaxially a monocrystalline SiGe seed layer [101] having about between 50% and 90% of Ge concentration over a relaxed SiGe layer [130] having about up to 50% of Ge concentration;

depositing epitaxially a compressively strained Ge layer [100] over said SiGe seed layer; and

hosting said PMOS device in said compressively strained Ge layer [100] .

22. The method of claim 21, wherein said SiGe seed layer [101] is chosen to be about between 0.3nm and 3nm thick, and said compressively strained Ge layer [100] is chosen to be about between 5nm and 20nm thick.

23. The method of claim 21, further comprising the step of depositing epitaxially a SiGe top layer [120] over said compressively strained Ge layer [100], wherein said SiGe top layer is chosen to have about up to 10% of Ge concentration.

24. The method of claim 23, wherein said SiGe top layer [120] is chosen to be essentially pure Si with a thickness of about between 0.3nm and 10nm.

25. The method of claim 21, wherein the steps of depositing epitaxially said SiGe seed layer [101] and said compressively strained Ge layer [100] are executed in manner to be selective with regard to dielectric materials.

26. The method of claim 23, wherein the steps of depositing epitaxially said SiGe top layer [120] is executed in manner to be selective with regard to dielectric materials.

27. The method of claim 21, further comprising the step of using a high-K material in a gate insulator [310] for said PMOS device.

28. The method of claim 21, further comprising the step of using a deposited oxide in a gate insulator [310] for said PMOS device.

29. A method for fabricating a CMOS circuit, comprising the steps of:

providing an SGOI wafer [151,150,130] having a relaxed SiGe layer [130] with about up to 50% of Ge concentration;

defining NMOS [220] and PMOS [210] regions on said SGOI wafer;

capping said NMOS regions with a dielectric material [160] ;

depositing epitaxially and in a selective manner a monocrystalline SiGe seed layer [101] having about between 50% and 90% of Ge concentration over said relaxed SiGe layer;

depositing epitaxially and in a selective manner a compressively strained Ge layer [100] over said SiGe seed layer [101] ; and

hosting a PMOS device in said compressively strained Ge layer [100] .

30. The method of claim 29, further comprising the step of depositing epitaxially and in a selective manner a SiGe top layer [120] over said compressively strained Ge layer [100], wherein said SiGe top layer is chosen to have about up to 10% of Ge concentration.

31. The method of claim 30, wherein said SiGe top layer [120] is chosen to be essentially pure Si with a thickness of about between 0.3nm and 10nm.

32. The method of claim 29, further comprising the steps of stripping said dielectric material [160] capping said NMOS regions, and fabricating NMOS devices in said NMOS regions.

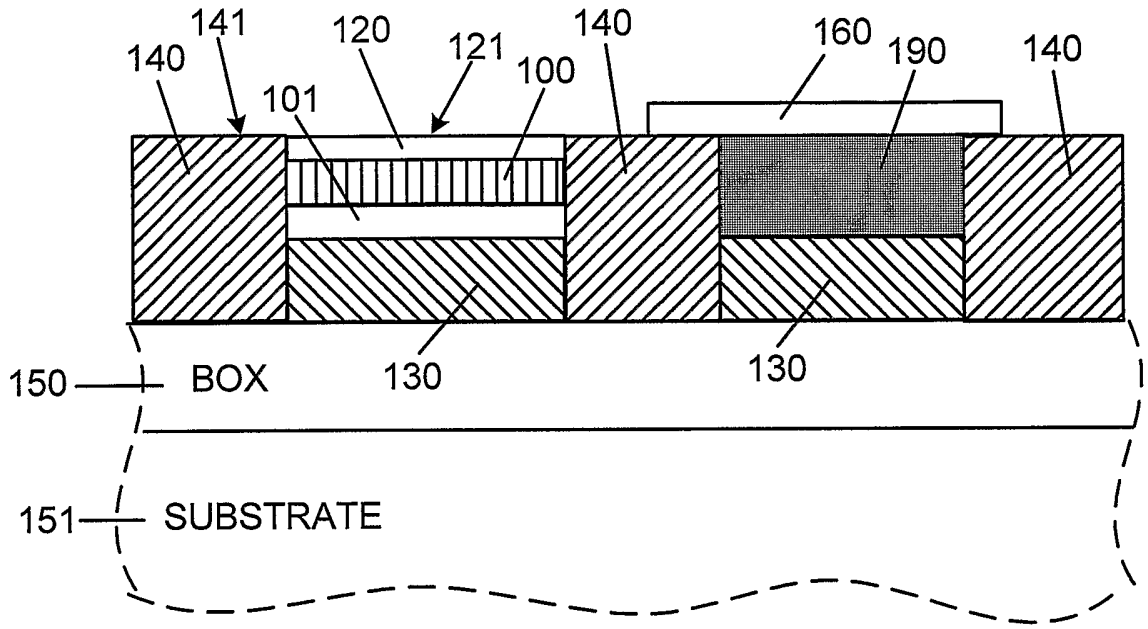
141
140
120
121
140
160
190
140
101
100
150
BOX
130
130
151
SUBSTRATE

Fig. 1

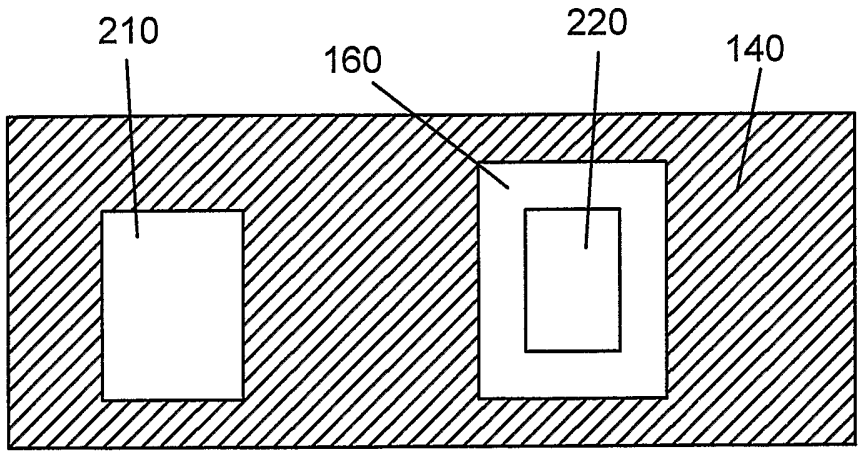
210
160
220
140

Fig. 2

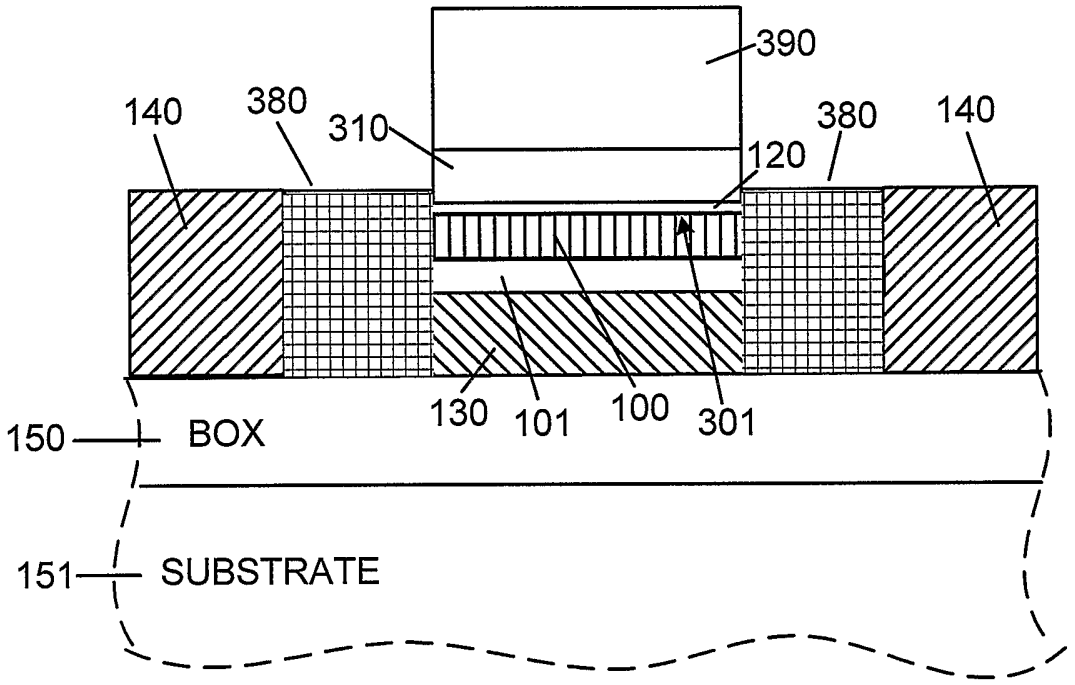
390
140
380
310
120
380
140
130
101
100
301
150
BOX
151
SUBSTRATE

Fig. 3

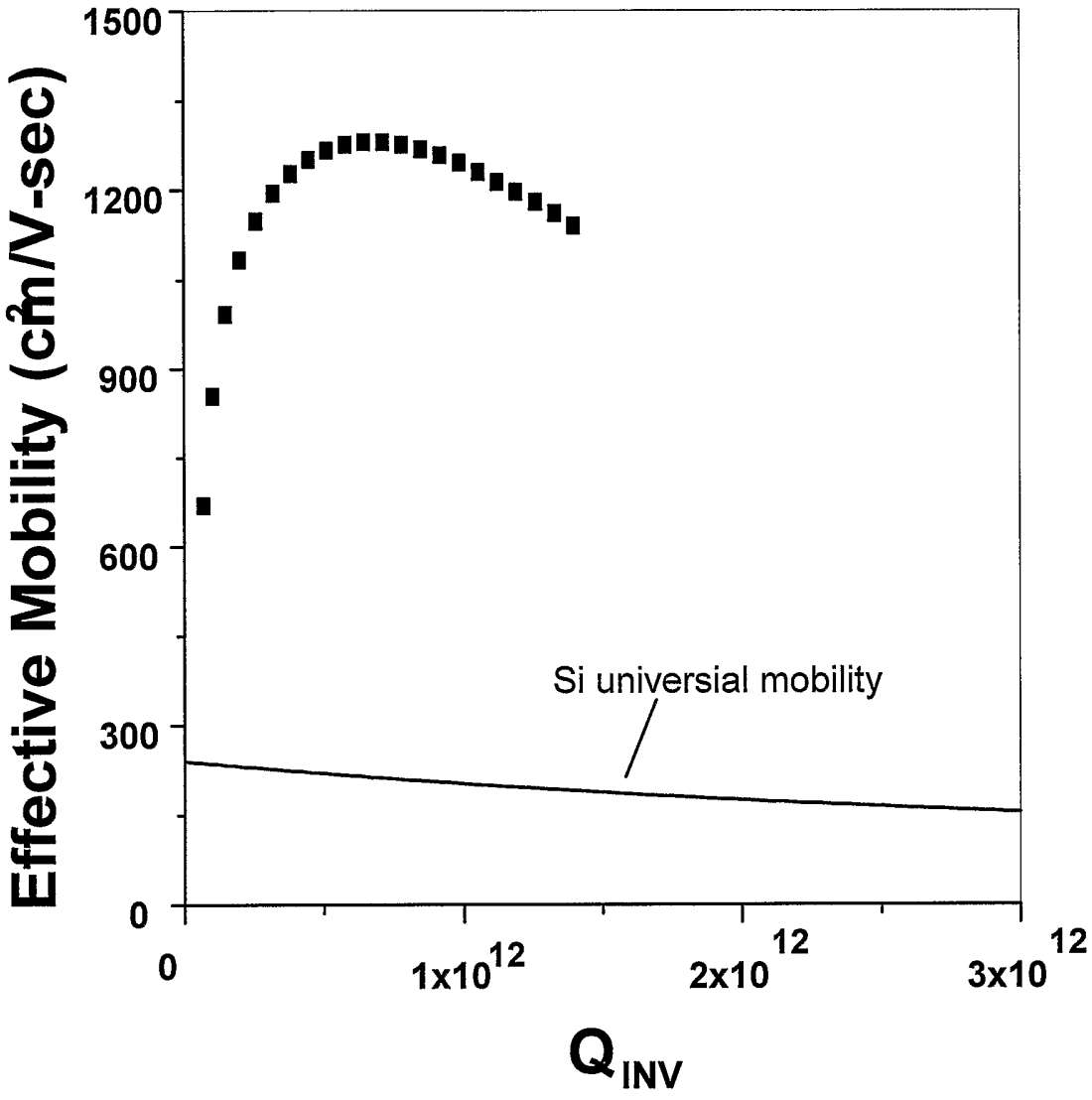
Effective Mobility (cm²/V-sec)
1500
1200
900
600
300
0
Si universial mobility
0
1x10^12
2x10^12
3x10^12
Q_INV

Fig. 4

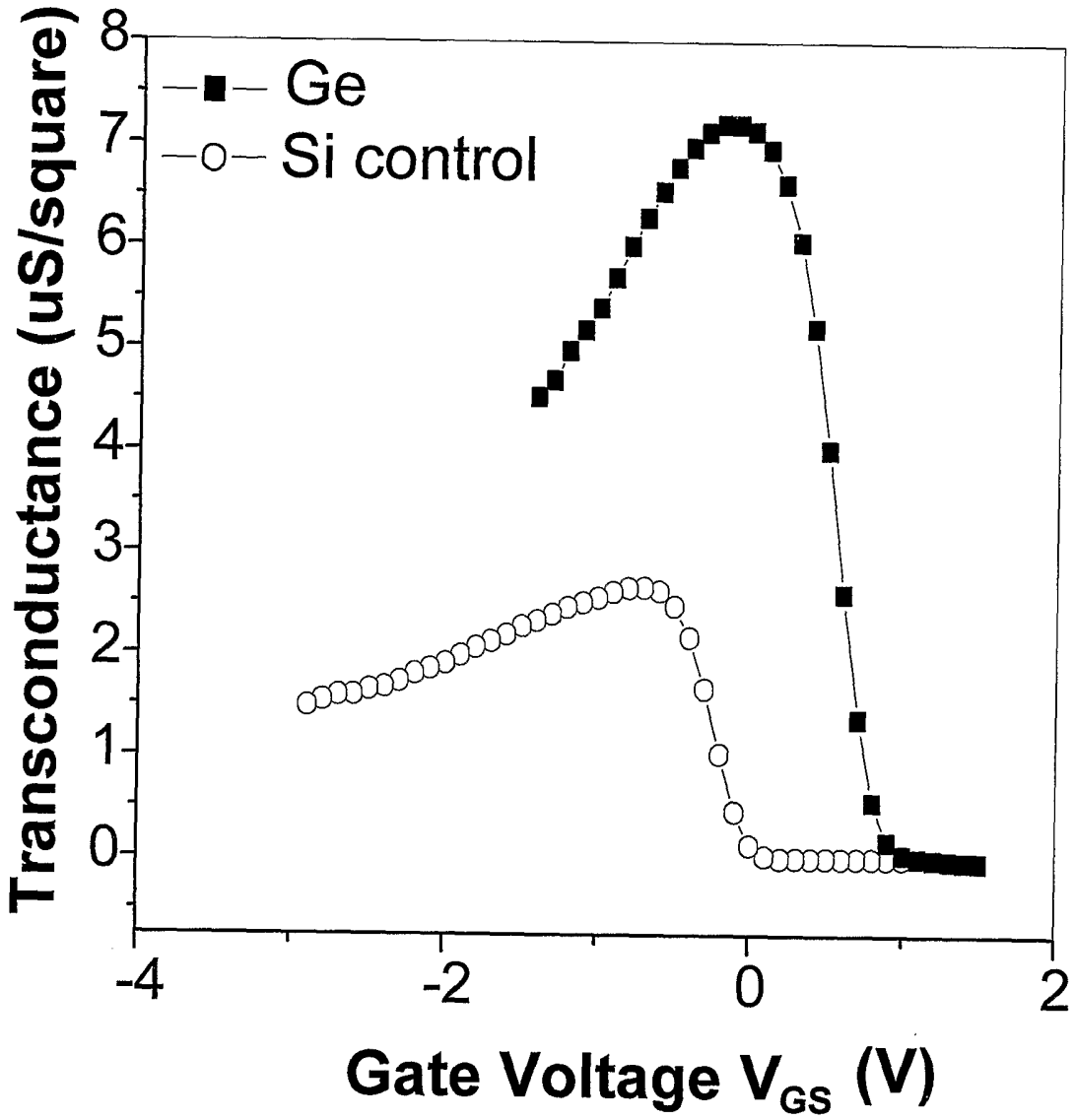
Transconductance (uS/square)
Gate Voltage V_{GS} (V)
Ge
Si control
8
7
6
5
4
3
2
1
0
-4
-2
0
2

Fig. 5

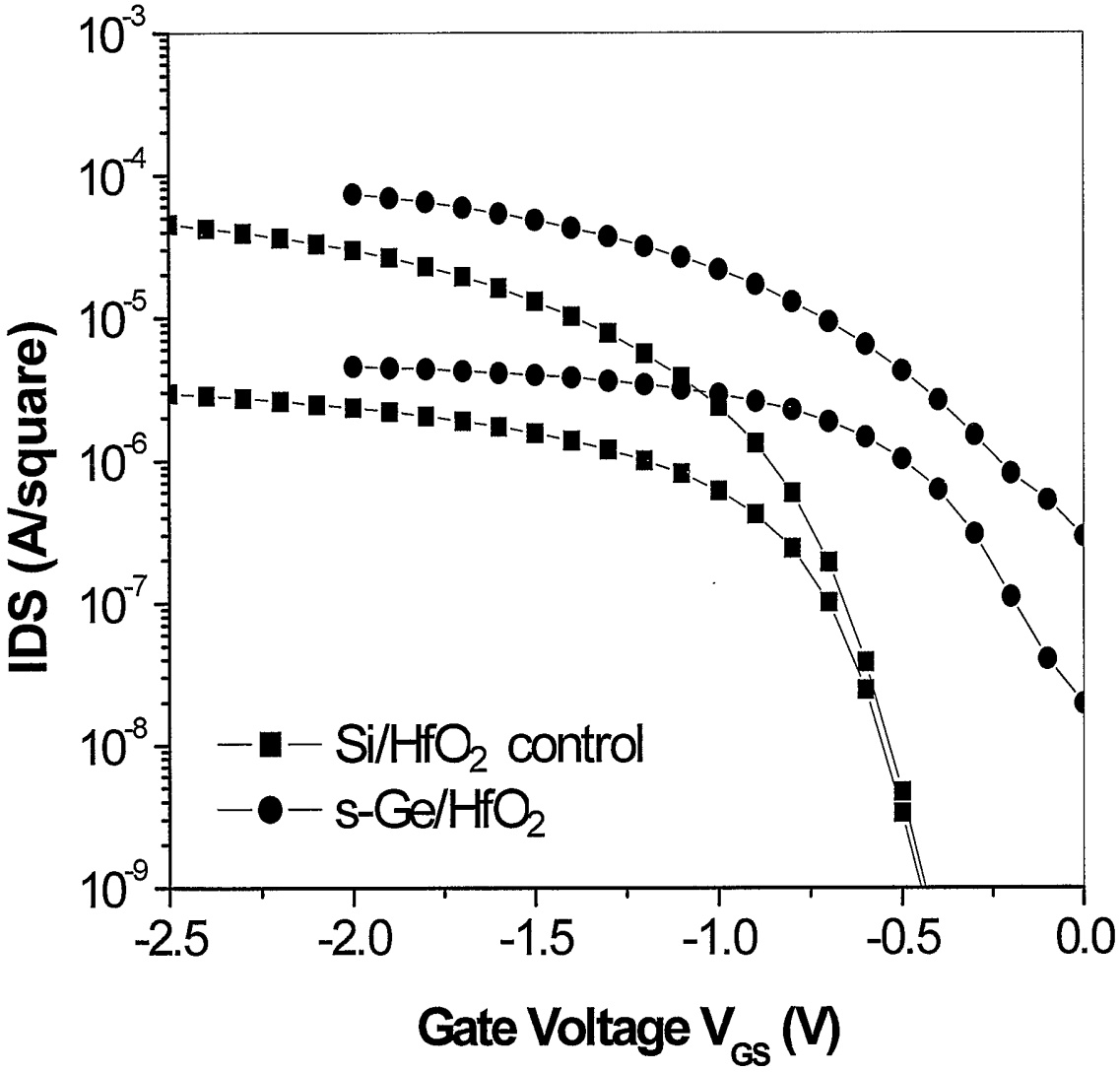
IDS (A/square)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
-2.5
-2.0
-1.5
-1.0
-0.5
0.0
Gate Voltage VGS (V)
Si/HfO2 control
s-Ge/HfO2

Fig. 6