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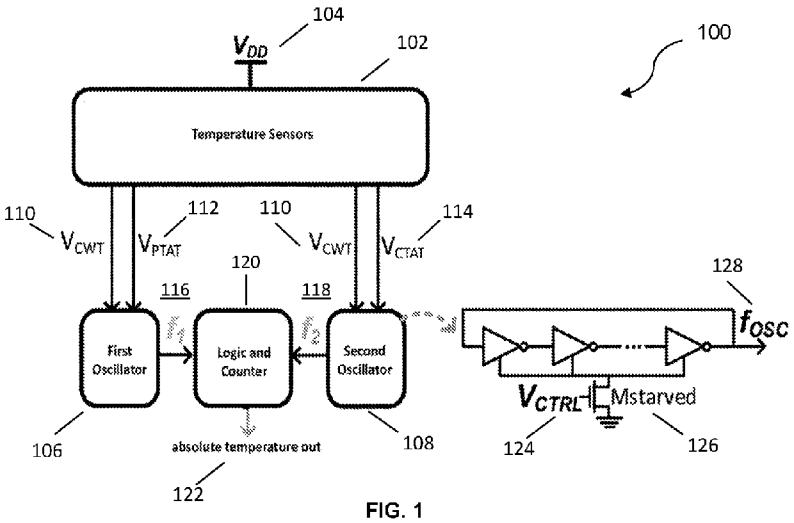



FIG. 1

(57) Abstract: In a described embodiment, a temperature-to-digital conversion system is provided including a plurality of sensors configured to convert a temperature into a plurality of voltage signals, wherein each voltage signal is independent, proportional, or inversely proportional to changes in the temperature. The system further includes a first oscillator configured to receive a first voltage signal that is proportional to changes in temperature and output a first frequency based on the first voltage signal. A second oscillator is configured to receive a second voltage signal that is inversely proportional to changes in temperature and output a second frequency based on the second voltage signal. A first level shifter configured to adjust a first voltage level corresponding to the first frequency and a second level shifter is configured to adjust a second voltage level corresponding to the second frequency. A digital conversion module is configured to receive the adjusted first and second voltage levels and convert the adjusted voltage levels into a digital output representative of the temperature.

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# System and Method for Converting Temperature Measurements into Digital Data

## Technical Field

The present application relates generally to temperature measurement technologies, and in particular to systems and methods that use oscillators for converting temperature measurements into digital data.

## Background

Temperature sensing is a critical component in diverse industries, where it supports crucial applications such as pharmaceuticals, food logistics, and environmental monitoring. These sectors depend on sensors that deliver high accuracy while operating autonomously for extended periods to ensure continuous monitoring without frequent maintenance.

Traditional temperature sensing systems often rely on energy storage elements like batteries or supercapacitors, which increase both the size and cost of these systems. More energy-efficient solutions have recently begun to replace these systems, designed to function with the limited power available from miniature energy harvesters. Although these advances have led to reductions in power consumption, the improvements in conversion times and accuracies have been moderate. These developments have primarily focused on reducing reliance on regulated power supplies and simplifying voltage conversion circuitry. Despite these improvements, significant challenges remain, particularly in balancing power efficiency with operational complexity and ensuring robust performance across varying environmental conditions. Existing solutions often still encounter trade-offs among these factors, which can complicate design and lead to increased costs.

Therefore, it is desirable to provide a system and method that optimizes temperature-to-digital conversion to address the disadvantages or limitations of the existing technologies or, at the very least, provide the public with a useful alternative.

## Summary

The present disclosure aims to provide new and useful systems and methods for temperature measurement, and in particular those that use oscillators to convert temperature measurements into digital data.

In broad terms, the present disclosure proposes a temperature-to-digital conversion system, including: a plurality of sensors configured to convert a temperature into a plurality of voltage signals, wherein each voltage signal is independent, proportional, or inversely proportional to changes in the temperature; a first oscillator configured to receive a first voltage signal that is proportional to changes in temperature and output a first frequency based on the first voltage

signal; a second oscillator configured to receive a second voltage signal that is inversely proportional to changes in temperature and output a second frequency based on the second voltage signal; a first level shifter configured to adjust a first voltage level corresponding to the first frequency; a second level shifter configured to adjust a second voltage level corresponding to the second frequency; and a digital conversion module configured to receive the adjusted first and second voltage levels and convert the adjusted voltage levels into a digital output representative of the temperature.

In embodiments, each sensor is configured to convert the temperature into the plurality of the voltage signals in a manner that is nearly-independent of variations in supply voltage.

In implementations, each of the first and second oscillator is a ring oscillator configured to utilize dynamic leakage suppression logic to reduce power leakage.

In particular embodiments, the digital conversion module includes a counter and calibration logic configured for dual-edge triggered counting in order to determine a plurality of temperature measurements.

In implementations, each sensor includes a basic cell or a variant thereof, wherein the basic cell includes a pair of transistors configured to carry equal current.

In implementations, the pair of transistors include a zero-VGS transistor and a diode-connected transistor.

In some embodiments, the variant of the basic cell corresponds to a current mirror arrangement for outputting the first voltage signal.

In particular embodiments, the variant of the basic cell corresponds to a bipolar-junction transistor arrangement for outputting the second voltage signal.

In implementations, the bipolar-junction transistor arrangement is a substitute for a diode-connected transistor of the basic cell.

In embodiments, at least one of the first and second level shifters includes a configuration having a current mirror arrangement and an output transistor with a modified body connection, wherein the configuration achieves a full voltage swing at an output of each level shifter.

In embodiments, the at least one of the first and second level shifters employ a voltage droop technique using one or more transistors configured within a current mirror arrangement for enhancing a voltage swing at an output of each level shifter.

In implementations, the at least one of the first and second level shifters incorporates transistors configured as Low Voltage Threshold (LVT) devices.

In embodiments, each of the first and second oscillators is configured as a five-stage ring oscillator that employs Dynamic Leakage Suppression (DLS) logic.

In particular embodiments, the first frequency varies exponentially with temperature and the first voltage signal, and the second frequency varies in relation to the second voltage signal, wherein each of the first and second frequencies are modulated by a body effect coefficient to linearize their responses to temperature variations.

In some embodiments, each of the first and second oscillators employ a voltage control mechanism through body terminals of their transistors to modulate their respect frequency outputs.

The present disclosure further proposes a method for converting temperature into digital data, including: converting a temperature into a plurality of temperature-dependent voltage signals via a plurality of sensors, wherein each voltage signal is independent, proportional, or inversely proportional to changes in the temperature; receiving a first voltage signal that is proportional to changes in temperature at a first oscillator and outputting a first frequency based on this first voltage signal using the first oscillator; receiving a second voltage signal that is inversely proportional to changes in temperature at a second oscillator and outputting a second frequency based on this second voltage signal using the second oscillator; adjusting a voltage level corresponding to the first frequency using a first level shifter; adjusting a voltage level corresponding to the second frequency using a second level shifter; receiving the adjusted first and second voltage levels at a digital conversion module; and converting the adjusted voltage levels into a digital output representative of the temperature using the digital conversion module.

The present disclosure further proposes a system for a system for temperature-to-digital conversion, including: a first circuit for providing a first output voltage that is constant with temperature; a second circuit for providing a second output voltage that is proportional to temperature and providing a third output voltage that is inversely proportional to temperature; a level shifter for adapting voltage levels within the system; two ring oscillators composed by body terminal-controlled logic gates to perform a voltage-to-frequency conversion for generating frequency information; and a digital block for converting the frequency information to a digital code.

In some embodiments, the system further comprises a plurality of regulation components, wherein the plurality of regulation components includes a NMOS-only transistor voltage reference configured to perform implicit voltage regulation.

The present disclosure further proposes a system including an oscillator system configured to perform voltage-to-frequency conversion including a first oscillator and a second oscillator, wherein each oscillator is powered by a first output voltage constant with temperature from a first circuit and controlled by a second output voltage that is proportional to temperature from a second circuit or a third output voltage that is inversely proportional to temperature from a third circuit; and a level shifter configured to adapt voltage levels corresponding to the outputs of the first oscillator and the second oscillator to voltage levels suitable for digital processing;

In embodiments, the system includes a readout logic for converting the adapted voltage levels from the level shifter to a digital format.

The above description is provided as an overview of some implementations of the present disclosure. Further description of those implementations, and other implementations, are described in more detail below.

Brief Description of the Drawings:

Embodiments of the invention will now be explained for the sake of example only, with reference to the following figures in which:

FIG. 1 is a schematic representation of a temperature-to-digital conversion system that converts temperature into digital signals, according to an embodiment of the present disclosure.

FIG. 2 is a circuit diagram within the conversion system, based on a basic cell, for converting temperature into voltage levels, according to an embodiment of the present disclosure.

FIG. 3 is a voltage-to-temperature conversion circuit within the conversion system for converting voltage levels to digital data, according to an embodiment of the present disclosure.

FIG. 4 is a level shifter circuit within the conversion system that adapts oscillator outputs to align with digital logic levels, according to an embodiment of the present disclosure.

FIG. 5A is a timing diagram showing digital readouts of the temperature-to-digital conversion system, illustrating a single-edge triggered counting, according to an embodiment of the present disclosure.

FIG. 5B is a timing diagram showing digital readouts of the temperature-to-digital conversion system, illustrating a dual-edge triggered counting, according to an embodiment of the present disclosure.

FIG. 6A is a graphical representation showing measured output voltages of a temperature-to-voltage conversion system as the output voltages vary across different temperatures, according to an embodiment of the present disclosure.

FIG. 6B is a graphical representation displaying measured variations in the output voltages of the temperature-to-voltage conversion system across different supply voltage levels, according to an embodiment of the present disclosure.

FIG. 7A is a graphical representation showing a resolution and conversion time across a number of slow clock periods for a temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7B is a graphical representation displaying measured frequencies of slow and fast oscillators and their ratio across a temperature range from -10°C to 70°C in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7C is a graphical representation showing noise characteristics in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7D is a graphical representation illustrating a power consumption across different supply voltages and temperatures in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 8A is a graphical representation showing temperature measurement errors of the temperature-to-digital conversion system across various process corners at a fixed supply voltage, according to an embodiment of the present disclosure.

FIG. 8B is a graphical representation showing the temperature measurement errors across a range of supply voltage levels at a constant temperature, according to an embodiment of the present disclosure.

FIG. 8C is a graphical representation showing an energy consumption per conversion of the temperature-to-digital conversion system across different temperatures at a fixed supply voltage $V_{DD}$, according to an embodiment of the present disclosure.

FIG. 8D is a graphical representation showing a variation of a reference voltage $V_{REF}$ in the temperature-to-digital conversion system across temperatures from -10°C to 70°C at a fixed supply voltage $V_{DD}$, according to an embodiment of the present disclosure.

FIG. 9 is a micrograph of a test chip used in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 10 is a flowchart illustrating a method for converting temperature into digital data according to an embodiment of the present disclosure.

Detailed Description

Embodiments will now be discussed with reference to the accompanying FIGs, which depict one or more exemplary embodiments. These embodiments are described in sufficient detail to enable those skilled in the art to practice the embodiments and it is to be understood that mechanical, logical, and other changes may be made without departing from the scope of the embodiments. Therefore, embodiments may be implemented in many different forms and should not be construed as limited to the embodiments set forth herein, shown in the FIGs, and/or described below.

Herein, the term “zero-VGS transistor” refers to the configuration of a transistor where the gate-source voltage (VGS) is intentionally set to zero, causing the transistor to operate in the subthreshold region.

Herein, the term “diode-connected transistor” refers to the configuration of a transistor wherein its gate is directly connected to its drain, making it behave in a manner analogous to a diode. This configuration allows the transistor to pass current in one direction, creating a predictable voltage drop across it that is useful in applications requiring voltage stabilization or rectification within electronic circuits.

Herein, the term "basic cell" refers to a fundamental unit within a temperature-to-voltage conversion system that includes a pair of transistors configured to carry equal current. As used in this disclosure, the basic cell may include the zero-VGS transistor and the diode-connected transistor.

Unless otherwise defined, all terms (including technical and scientific terms) used herein are to be interpreted as is customary in the art. It will be further understood that terms in common usage should also be interpreted as is customary in the relevant art.

FIG. 1 is a schematic representation of a temperature-to-digital conversion system 100 that converts temperature into digital signals, according to an embodiment of the present disclosure.

The conversion system 100 may include a plurality of temperature sensors 102 which convert an ambient temperature into a plurality of voltage signals. In examples, the sensors 102 may be configured to be nearly voltage-independent, i.e. the output voltages of the sensors are largely unaffected by changes in the supply voltage $V_{DD}$ 104, maintaining consistent output voltages without significant distortion or variation caused by potential fluctuations in the supply voltage.

The temperature-to-voltage conversion in the temperature-to-digital conversion system 100 may be implemented by three types of temperature sensors 102 that produce output voltages which are nearly independent of the supply voltage (VDD) but also vary according to different temperature dependencies. These temperature sensors 102 may be categorized as follows: Constant with Temperature (CWT) sensor: Outputs a stable voltage $V_{CWT}$ 110 that remains constant regardless of temperature changes, making it useful for providing a stable reference voltage across varying conditions. Proportional to Absolute Temperature (PTAT) sensor: Outputs a voltage $V_{PTAT}$ 112 that increases linearly with the temperature. Complementary to Absolute Temperature (CTAT) sensor: Outputs a voltage $V_{CTAT}$ 114 that decreases as the temperature rises, providing an inversely proportional temperature reading.

The temperature-to-digital conversion system 100 may further include a pair of oscillators, designated as First Oscillator 106 and Second Oscillator 108. In example embodiments, each of the first and second oscillators 106 and 108 may be configured as body-driven ring oscillators. Such body-driven ring oscillators may use body biasing techniques to control the threshold voltage of the transistors, affecting the oscillation frequency based on temperature changes. Each of the first and second oscillators 106 and 108 may function as a Voltage-Controlled Oscillator (VCO), varying its frequency based on the output voltages it receives from the temperature-dependent sensors.

In examples, the oscillators 106 and 108 may receive temperature-dependent voltages $V_{CWT}$ 110, $V_{PTAT}$ 112, and $V_{CTAT}$ 114 as inputs from the sensors 102. $V_{CWT}$ 110, provides a stable, constant voltage regardless of temperature fluctuations and may serve as a baseline reference voltage for both of the oscillators 106 and 108.

The First Oscillator 106 processes voltage input $V_{PTAT}$ 112 to produce a first frequency $f_1$ 116. The Second Oscillator 108 processes voltage input $V_{CTAT}$ 114 to produce a second frequency $f_2$ 118. This configuration allows each oscillator to adapt its output frequency according to varying temperature conditions, facilitating the system's ability to capture and accurately represent a wide range of temperature data.

The frequencies $f_1$ 116 and $f_2$ 118 outputted from the First Oscillator 106 and the Second Oscillator 108, respectively, are further inputted into a logic and counter 120. The logic and counter 120 may process the frequencies $f_1$ 116 and $f_2$ 118 to convert these signals into a digital readout, which is output as an 'absolute temperature out' 122. This process may include counting the frequency pulses over a specified period and utilizing digital logic operations to convert these counts into corresponding temperature measurements.

The temperature-to-digital converter 100 of the present disclosure may operate below a 100-pW (pico-watt) power threshold, which is a low level of power consumption. This feature makes it suitable for "always-on" applications, meaning it can continuously operate without the need to switch off to conserve energy. Such low power usage is important for systems that rely on energy harvesting (such as solar power or thermal energy), where available power is minimal and often variable. The converter 100 may be configured to operate with an unregulated power supply, which simplifies the design and reduces the cost of additional components like voltage regulators. This ability to operate with a non-steady or fluctuating input voltage is particularly valuable in environments where energy harvesting is used, as the energy sources (like light or temperature differences) can be inconsistent.

The temperature-to-digital converter 100 may be configured for applications that do not require instant temperature readings but can accept a slower response time (around 10 seconds). The sensors 102 of the converter 100 can be configured to not rely on a stable voltage supply for accurate operation, which is advantageous in unregulated systems. For example, the sensors 102 are capable of converting temperature directly to a voltage output independently of input voltage stability, therefore enhancing their performance and consistency under fluctuating power conditions.

In contemporary configurations, an option includes using ring oscillators that contain current-starved transistors, labeled as Mstarved 126. These transistors 126 are deliberately limited in current flow, which leads to challenges due to leakage currents disproportionately affecting ultra-low power consumption. Additionally, such current-starved oscillators exhibit a non-linear frequency response, where the oscillation frequency $f_{OSC}$ 128 is exponentially proportional to its control voltage $V_{CTRL}$ 124, expressed as $f_{OSC} \propto \exp(V_{CTRL})$. This exponential relationship complicates stable and precise operation, making it challenging to achieve accuracy in applications requiring high precision.

To address these challenges, the conversion system 100 is configured to provide a 'body-driven dynamic leakage suppression logic.' This technique involves using a plurality of transistor bodies of each oscillator 106 and 108 as a control element to actively regulate and

minimize leakage currents, thereby stabilizing power consumption and linearizing the frequency response. By enhancing the control over leakage currents, this logic improves the performance and reliability of the oscillators.

FIG. 2 is a circuit diagram 200 within the conversion system 100, based on a basic cell 202, for converting temperature into voltage levels, according to an embodiment of the present disclosure.

Basic Cell Design

As shown in FIG. 2, the circuit diagram uses a basic cell 202 design formed by a zero-VGS and diode-connected NMOS transistor pair for temperature-to-voltage conversion. The basic cell 202 includes two NMOS transistors, $M_{zvgs}$ 204 and $M_{diode}$ 206. $M_{zvgs}$ 204 is configured to operate at zero gate-source voltage (zero-VGS), meaning its gate and source are at the same potential, placing it in the subthreshold region where it operates with minimal current flow. $M_{diode}$ 206 is configured to be diode-connected, meaning its gate and drain are shorted together, which ensures that it behaves similarly to a diode, allowing current in only one direction and creating a specific voltage drop that is sensitive to changes in temperature. Both transistors $M_{zvgs}$ 204 and $M_{diode}$ 206 are designed to carry equal current, which helps maintain the stability of the output voltage against variations in supply voltage or environmental conditions.

Integration into Larger Circuitry

Temperature-to-voltage conversion in this system is achieved through three distinct circuits 208, 210 and 212, each designed to produce an output voltage that is nearly-independent of supply voltage fluctuations and exhibits different responses to temperature changes. These output responses are categorized as Constant with Temperature (CWT) 208, Proportional to Absolute Temperature (PTAT) 210, and Complementary to Absolute Temperature (CTAT) 212. Each circuit utilizes the same fundamental basic cell structure 202 to maintain consistency in design and minimize variations caused by layout and manufacturing processes.

By using the same basic cell configuration 202 (zero-VGS and diode-connected transistors) for each circuit, the design ensures that the physical and electrical properties are consistent. This uniformity helps in reducing the variability in performance that might otherwise arise from different circuit layouts on the chip. Moreover, semiconductor fabrication can have variations at different process "corners," which represent extremes in material properties or operating conditions. Utilizing a uniform basic cell configuration 202 across the various output circuits aims to make each circuit behave similarly under these extremes, improving the device's overall reliability and predictiveness across its manufacturing process.

Voltage Self-Regulation

Native NMOS transistors $M_{native}$ 214 may be designed to have minimal threshold voltage (Vth). In this circuit configuration, $M_{native}$ transistors 214 may be utilized at the source terminals of the circuitry involved in generating $V_{CWT}$ 208, $V_{PTAT}$ 210, and $V_{CTAT}$ 212 voltages. $M_{native}$ transistors 214 are used for implicit supply voltage self-regulation, ensuring the system's independence from external power variations. This self-regulation helps maintain consistent performance without additional power or circuitry for voltage regulation.

In embodiments, Voltage $V_Y$ 216 represents the voltage at the drain of a $M_{native}$ transistor 214. $V_Y$ 216 is independent of supply voltage $V_{dd}$ 218, and therefore fluctuations in the power supply $V_{dd}$ 218 do not affect the voltage level at $V_Y$ 216. In examples, $V_Y$ 216 may be derived as follows:

$$V_Y \approx V_{TH_{diode}} - V_{TH_{native}} + n\frac{kT}{q}\ln\left(\frac{W_{native}L_{diode}}{W_{native}L_{native}}\right) + n\frac{kT}{q}\ln\left(\frac{I_{leakage,native}}{I_{leakage,zvgs}}\right)$$

where $V_{TH_{diode}} - V_{TH_{native}}$ represents a difference in threshold voltages between the diode-connected transistor 206 and the native NMOS transistor 214. The term $n\frac{kT}{q}\ln\left(\frac{W_{native}L_{diode}}{W_{native}L_{native}}\right)$ accounts for a temperature-dependent voltage change influenced by the relative dimensions of the diode-connected and the native NMOS transistors 206 and 214. Here, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the charge of an electron, and $n$ is a factor dependent on the transistor characteristics. The term $n\frac{kT}{q}\ln\left(\frac{I_{leakage,native}}{I_{leakage,zvgs}}\right)$ accounts for the ratio of leakage currents between the native NMOS transistor 214 and the zero-VGS transistor 204. Leakage currents, which can increase with temperature and affect transistor performance, are factored into the overall voltage calculation of $V_Y$ 216.

Role of $V_{REF}$ in CWT Circuit

Reference voltage $V_{REF}$ 220 is generated from the CWT branch 222 of the circuit 200. The CWT branch 222 is configured to produce a stable output voltage $V_{CWT}$ 208 that remains constant or changes minimally with temperature variations. A characteristic of $V_{REF}$ 220 is that it has a near-zero temperature coefficient, and therefore its value does not fluctuate significantly with changes in ambient temperature. This property allows the reference voltage $V_{REF}$ 220 to remain consistent under various conditions, serving as a dependable standard for the other circuit components.

By using $V_{REF}$ 220 from the existing $V_{CWT}$ 208 circuit as the reference voltage, there is no need to allocate additional power and space to generate a separate reference voltage. This

integration reduces the overall power consumption and conserves space on the chip area, which is particularly beneficial for compact or power-sensitive applications. Moreover, as $V_{REF}$ 220 does not supply current to other parts of the circuit 200 (i.e. it should not be used in parts of the circuit that require current drive), it serves effectively for setting voltage levels or acting as a voltage standard within the circuit 200.

Output Voltage Generation:

As noted above, the basic cell 202 includes a zero-VGS transistor $M_{zvgs}$ 204 and a diode-connected transistor $M_{diode}$ 206, both set to carry equal current. This configuration forms the foundation of the circuitry for the CWT 202, PTAT 226, and CTAT 230 branches for generating three voltage types: $V_{CWT}$ 208, $V_{PTAT}$ 210, and $V_{CTAT}$ 212

In embodiments, an output voltage $V_X$ 224 corresponding to a basic cell configuration 202 may be derived as follows:

$$V_X \approx V_{TH_{diode}} - V_{TH_{zvgs}} + n\frac{kT}{q}\ln\left(\frac{W_{zvgs}L_{diode}}{W_{diode}L_{zvgs}}\right)$$

where $V_{TH_{diode}}$ and $V_{TH_{zvgs}}$ are threshold voltages of the diode-connected and zero-VGS transistors 204 and 206, respectively. Component $n\frac{kT}{q}$ represents a thermal voltage, where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the charge of an electron, and $n$ is a factor dependent on the transistor characteristics. The logarithmic term accounts involving the ratios of the widths (W) and lengths ($L$) of the gates of the diode-connected and zero-VGS transistors 204 and 206, respectively.

As indicated, the equation $V_X \approx V_{TH_{diode}} - V_{TH_{zvgs}} + n\frac{kT}{q}\ln\left(\frac{W_{zvgs}L_{diode}}{W_{diode}L_{zvgs}}\right)$ may serve as a basis for generating $V_X$ 224 in the basic cell. The PTAT 226, CTAT 230, and bias 228 branches each use this foundational equation to derive their respective versions of $V_X$ 224, i.e. $V_X$', $V_X$'', $V_X$''' 232. Each respective variation $V_X$', $V_X$'', $V_X$''' 232 is calculated to exhibit different temperature dependence which is determined by specific adjustments to the load types and aspect ratios of the transistors of each branch.

Output Voltage $V_{CWT}$– Constant with Temperature:

$V_{CWT}$ 208 is derived directly from the basic cell 202 and may be configured to maintain a stable output voltage that exhibits a near-zero temperature coefficient (TC). $V_{CWT}$ 208 serves as a voltage reference within the circuit, providing a consistent voltage level that is important for the accurate operation of other components in the system. In embodiments, $V_{CWT}$ 208 may

provide picoampere (pA) current delivery, indicative of very minimal power consumption and output.

Output Voltage $V_{PTAT}$– Proportional to Absolute Temperature:

$V_{PTAT}$ 210 may be generated by "folding" the basic cell 202 through a current mirror arrangement 234 to achieve a positive TC. The current mirror 234 in the PTAT branch is used to replicate the current from the basic cell 202 across multiple transistor stages. The design ensures that the voltage response to changes in temperature is amplified. By "folding" the basic cell 202 through the current mirror 234, the circuit 226 multiplies the effect of the thermal voltage component across several stages. Each stage contributes to an overall increase in output voltage $V_{PTAT}$ 210 as the temperature rises, ensuring that $V_{PTAT}$ 210 exhibits a positive TC and increases linearly with an increase of temperature.

Output Voltage $V_{CTAT}$– Complementary to Absolute Temperature:

$V_{CTAT}$ 212 may be generated by replacing a Metal-Oxide-Semiconductor (MOS) diode in the basic cell with a parasitic Bipolar Junction Transistor (BJT) replacement 234, which may be realized using a deep-N-well NMOS. The parasitic BJT replacement 234 may be either an NPN transistor or a PNP transistor. Notably, the PNP transistor solution may demonstrate better process sensitivity by using the NMOS deep-N-well configuration. This substitution leverages the NPN or PNP's increased capability to conduct current at higher temperatures, causing the output voltage to decrease as the temperature increases, hence a negative temperature coefficient.

FIG. 3 is a voltage-to-temperature conversion circuit 300 within the conversion system 100 for converting voltage levels to digital data, according to an embodiment of the present disclosure.

As shown in FIG. 3, the voltage-to-temperature conversion circuit 300 includes a fast oscillator 302 and a slow oscillator 304, where the fast oscillator 302 is driven by output voltage $V_{PTAT}$ and the slow oscillator 304 is driven by output voltage $V_{CTAT}$, and powered by self-regulated voltage $V_{CWT}$, leveraging the outputs of the temperature-to-voltage conversion in FIG. 2. Both output voltages $V_{PTAT}$ and $V_{CTAT}$ control the oscillators through the body of footer transistors. Both oscillators are powered by a self-regulated voltage $V_{CWT}$, which provides consistent performance regardless of external power fluctuations.

Both oscillators 302 and 304 may implement a Dynamic Leakage Suppression (DLS) logic framework to substantially reduce leakage currents. Leakage current, especially in low-power circuits, can affect the efficiency and operational life of a device.

In implementations, the PTAT-controlled fast oscillator 302 may be configured as a 5-stage ring oscillator utilizing DLS logic. A frequency output $f_{FAST}$ 308 of the fast oscillator 302 decreases with rising $V_{PTAT}$ following the relationship expressed as $f_{FAST} \propto^{-1} \exp(\lambda_{BB} * V_{PTAT})$, where $\lambda_{BB}$ represents a body effect coefficient. In implementations, the CTAT-controlled slow oscillator 304 may similarly be configured as a 5-stage ring oscillator using DLS logic. A frequency output $f_{SLOW}$ of the slow oscillator also decreases with rising $V_{CTAT}$ following the relationship expressed as $f_{SLOW} \propto^{-1} \exp(\lambda_{BB} * V_{CTAT})$, where $\lambda_{BB}$ represents the body effect coefficient. In example embodiments, the body effect coefficient $\lambda_{BB}$ measures the sensitivity of a threshold voltage to changes in the body voltage.

Voltage-controlled oscillators in low-power circuits may often use a current-starving transistor to control the frequency. This current-starving transistor restricts the flow of current through the oscillator circuit, which in turn modulates the oscillation frequency. As shown in FIG. 3, in the body-driven control approach 306, instead of using a current-starving transistor, the control 306 is achieved through modulating the body voltage of the transistors in the oscillator. This technique is called "body-driven" because it utilizes the body terminal of MOSFETs (a type of transistor) to influence the transistor's threshold voltage and thus its conducting state. One of the issues with current-starved oscillators is that they can exhibit non-linear behaviour between the control voltage and the frequency. This non-linearity is often exponential, making it difficult to predict or control precisely, especially in sensors where accuracy is important. By implementing voltage control through the body terminal, mitigation of voltage frequency non-linearity can be achieved. In embodiments, effective mitigation of voltage-frequency non-linearity is achieved when the body effect coefficient $\lambda_{BB}$ is significantly less than one.

Additionally, by using body voltage for control instead of gate or source voltages, the sensitivity of the frequency response to changes in control voltage is reduced. Moreover, it is typically easier and more efficient to modulate voltage parameters at very low power levels (e.g. the pW range) compared to controlling current. The body-driven oscillators 302 and 304 may achieve a very low power consumption—less than 100 pW, which is below typical leakage levels. As the temperature changes, $V_{PTAT}$ and $V_{CTAT}$ (which control the fast oscillator 302 and the slow oscillator 304, respectively) also change. $V_{PTAT}$ increases with temperature, while $V_{CTAT}$ decreases. This differential behaviour causes the output frequencies $f_{FAST}$ 308 and $f_{SLOW}$ 310 of the two oscillators 302 and 304 to diverge in a nearly linear fashion relative to temperature changes.

The voltage-to-digital conversion circuit 300 may further include two level shifters 312 and 314 that adapt output voltages corresponding to the output frequencies $f_{FAST}$ 308 and $f_{SLOW}$ 310 from the oscillators to suitable levels for digital processing. Each level shifter 312 or 314

provides compatibility between the oscillator signals and the digital logic levels required for the subsequent processing stages of the circuit. The level shifters 312 and 314 may have a static power consumption of less than 2.5 pW, enhancing the conversion circuit's 300 overall energy efficiency. Furthermore, each level shifter 312 or 314 may consume 60 fJ of energy per transition, contributing to the circuit's 300 overall low power consumption. Each level shifter 312 or 314 may also operate at 25 degrees Celsius with a Vdd 316 of 0.6 V and $V_{CWT}$ 318 of 0.5 V. Further specifics about the design and features of the level shifter circuitries 312 and 314 are described with respect to FIG. 4.

A counter and calibration logic module 320 provide digital processing for the voltage-to-digital conversion 300. The module 320 receives frequencies $f_{FAST}$ 308 and $f_{SLOW}$ 310 output from the oscillators 302 and 304 as input, counts and converts them into a digital output that represents the temperature, which is indicated as 'temperature out' 322. In embodiments, the module 320 may be enhanced with settings 324 from a scan chain, allowing dynamic configuration or calibration. The module 320 may incorporate Dynamic Leakage Suppression (DLS) logic, to optimize the reduction of power leakage and improve the energy efficiency during digital processing. The temperature output 322 of the module 320 is a digital signal representing the measured temperature, which can be used for further monitoring, control, or further processing in a variety of applications.

The counter and calibration logic module 320 may implement a dual-edge triggered design. This dual-edge configuration is implemented to enhance efficiency by capturing both the rising and falling edges of the signal during each oscillation cycle. By doing so, it effectively doubles the data rate compared to single-edge triggered systems, allowing for faster data processing within the same conversion time. This increase in processing efficiency significantly reduces the power required per unit of time, optimizing the overall energy consumption of the voltage-to-digital conversion circuit 300.

In embodiments, the temperature-to-digital conversion system 300 is designed so that both the fast oscillator 302 and the slow oscillator 304 share a common dependence on process corners and residual voltage fluctuations. This means that any such fluctuations impact both oscillators 302 and 304 equally. Consequently, the system 300 is configured to inherently reject the effects of these fluctuations, minimizing their impact on the accuracy of the temperature output 322.

In certain embodiments, the circuit 300 incorporates a digital correction mechanism within the readout logic of module 320. This feature enhances accuracy and minimizes the impact of any frequency mismatch between $f_{FAST}$ 308 and $f_{SLOW}$ 310 on the output count. This calibration, involving an offset digital correction strategy using a digital adder, is integrated into the circuit's

total power consumption. Notably, this integration allows the system to maintain low power usage, achieving figures as minimal as 38.4 pW.

FIG. 4 is a level shifter circuit 400 within the conversion system 100 that adapts oscillator outputs to align with digital logic levels, according to an embodiment of the present disclosure.

The level shifter 400 in FIG. 4 is designed to adjust the output voltage levels from both the fast oscillator 302, corresponding to output frequency $f_{FAST}$ 308, and the slow oscillator 304, corresponding to output frequency $f_{SLOW}$ 310, so that the output voltages align with the digital logic supply voltage $V_{DD}$ 326.

The level shifter 400 receives an input voltage (IN) 402 corresponding to one of output frequencies $f_{FAST}$ 308 or $f_{SLOW}$ 310 and effectively shifts this voltage 402 to drive the output (OUT) 404. This process not only reduces power consumption but also ensures that the output signals from the oscillators align with the voltage levels required by digital logic circuits.

DLS Headers and Footers and LVT devices

Dynamic Leakage Suppression (DLS) Headers 406 and Footers 408 are part of the DLS logic which reduces static power consumption. The DLS headers 406 and footers 408 control the flow of current, minimizing leakage in low-power states.

Low voltage threshold (LVT) devices may be used to reduce the necessary voltage to turn on the transistors, further contributing to the low-power levels achieved by the circuit.

Current Mirror Active Load (M2, M4 and M5)

The current mirror configuration 410 involving transistors M2, M4 and M5 helps maintain consistent current levels, which is important for stable voltage output in a low-power setting. The arrangement of the current mirrors 410 corresponds to Dynamic Leakage Suppression (DLS) logic. Unlike configurations that may use PMOS transistors alone for certain functions, the design of the current mirror uses both NMOS and PMOS transistors connected at their sources. The current mirror configuration 410 is useful in ultra-low power circuits as leakage can be a major source of power drain.

In the level shifter 400, *Ix* 412a and *Iy* 412b represent currents within a current mirror configuration, where *Ix* 412a is a reference current and *Iy* 412b is a mirrored output current. These currents are integral to ensuring consistent performance across the circuit by replicating the current from one part of the current mirror (where *Ix* 412a flows) to another (where *Iy* 412b is controlled).

Handling Voltage Limitations

DLS logic may face challenges in achieving full voltage swing at higher voltages, such as 1.2 V in 180 nm. To counteract the incomplete swing, an additional PMOS transistor (M5) is used to introduce a "voltage droop" 414. This effectively means that M5 helps pull up the voltage at a crucial node Va 418, enabling M4 to turn on more robustly, thereby enhancing the output swing at node Vb 416. Moreover, by connecting the body of M6 to its source rather than connecting the body to the ground, the threshold voltage of M6 is adjusted. This adjustment makes M6 stronger (i.e., it can turn on more effectively), which helps in achieving a full-swing output 404. Similarly, M4 has a modified body connection for helping achieve a full output swing at Vb 416 and voltage OUT 404.

In the example readouts shown in FIG. 5, the oscillations from the fast oscillator $f_{FAST}$ 308 and the slow oscillator $f_{SLOW}$ 310 are digitally converted through the conversion and calibration logic module. This is achieved by counting the cycles of $f_{FAST}$ 308 within a time window determined by M cycles of $f_{SLOW}$ 310.

FIG. 5A is a timing diagram 500 showing digital readouts of the temperature-to-digital conversion system, illustrating a single-edge triggered counting, according to an embodiment of the present disclosure.

The timing diagram 500 of FIG. 5A illustrates the temperature-to-digital conversion system measuring a temperature of 9°C using a single-edge triggered counting method. The time window for the measurement is set to M=1, indicating that the counting occurs over one cycle of the slow oscillator. $f_{SLOW}$ indicates one cycle of the slow oscillator, providing the duration over which the measurement is taken. $f_{FAST}$ indicates the frequency of the fast oscillator, which responds to temperature changes. The number of peaks represents how $f_{FAST}$ varies during the $f_{SLOW}$ cycle. For single-edge triggered counting, only the rising edges of $f_{FAST}$ within the one cycle of $f_{SLOW}$ are counted, resulting in a total count of 9 for this period. The timing diagram 500 specifies a resolution of 1°C, derived from counting nine rising edges during the cycle. In example embodiments, increasing M (the number of cycles of $f_{SLOW}$ counted) would increase the number of rising edges counted, thus improving resolution but at the cost of longer conversion time.

FIG. 5B is a timing diagram 502 showing digital readouts of the temperature-to-digital conversion system, illustrating a dual-edge triggered counting, according to an embodiment of the present disclosure.

The timing diagram 502 of FIG. 5B illustrates the temperature-to-digital conversion system measuring the same temperature of 9°C, but utilizing a dual-edge triggered counting method

within the same time window of M=1. The components are similar to those in FIG. 5A but with a key difference in the counting method. For dual-edge triggered counting, both rising and falling edges of $f_{FAST}$ are counted within the single cycle of $f_{SLOW}$, effectively doubling the count to 18 for the period. This results in an enhanced resolution of 0.5°C derived from counting eighteen rising edges during the cycle. The timing diagram 502 of FIG. 5B shows that counting both rising and falling edges doubles the resolution at the same conversion time, therefore achieving more precise measurements without an increase in the duration of the measurement cycle.

Experimental Results

The following section describes various experiments conducted to evaluate embodiments of the disclosure. Some of these experiments illustrate embodiments of the disclosure other than those discussed above.

FIG. 6A is a graphical representation showing output voltages of a temperature-to-voltage conversion system as the output voltages vary across different temperatures, according to an embodiment of the present disclosure.

FIG. 6A illustrates the response of four types of output voltages ($V_{CWT}$, $V_{PTAT}$, $V_{CTAT}$, $V_{REF}$) as the temperature varies from -10 °C to 70 °C, each responding differently due to their design purposes. $V_{CWT}$ and $V_{REF}$ are designed to be stable across temperature changes. They exhibit low temperature coefficients (TC) of 97.5 µV/°C and 40 µV/°C respectively, translating to 196 ppm/ºC and 269 ppm/ºC. This low sensitivity makes them ideal for providing reliable reference voltages in the circuit, ensuring that variations in temperature do not significantly affect their output. $V_{PTAT}$ and $V_{CTAT}$ exhibit higher sensitivities to temperature changes, with slopes of approximately +1 mV/°C and -1.5 mV/°C respectively. These characteristics are intentional to allow these voltages to be used effectively for measuring temperature. The combination of the temperature-to-voltage conversion and the body-driven oscillators results in an integral non-linearity (INL) of 1.05 °C (1.3 °C) in the 0-70 °C (-10-70 °C) range, indicating that while the outputs are generally linear, there is a small expected deviation across the operational temperature range.

FIG. 6B is a graphical representation displaying variations in the output voltages of the temperature-to-voltage conversion system across different supply voltage levels, according to an embodiment of the present disclosure.

FIG. 6B plots the same output voltages as FIG. 6A against changes in the power supply voltage (VDD) from 0.5 V to 1.8 V at a constant temperature (25 °C), illustrating their line

sensitivity. The line sensitivity values provided in the figure—$V_{CWT}$ (0.7 %/V), $V_{PTAT}$ (2.1 %/V), $V_{CTAT}$ (0.35 %/V), and $V_{REF}$ (0.4 %/V)—show how these voltages respond to changes in supply voltage. Lower line sensitivity values indicate better stability of the voltage output against fluctuations in the power supply. Native NMOS headers perform implicit voltage regulation at their source terminals, reducing the need for additional system voltage regulation. The line sensitivity values being kept to less than or equal to 2.1 % (the highest being $V_{PTAT}$ at 2.1 %) show this capability, allowing these circuits to maintain performance without external voltage regulators.

Notably, the experiments depicted in FIG. 6B showed an increase in the output of $V_{CWT}$ as the supply voltage approaches 1.8 V. To maintain consistent performance across the range of $V_{DD}$, it is recommended to limit the supply voltage to a maximum of 1.6 V. This precaution helps avoid the destabilizing effects that occur at higher voltage levels, maintaining the reliability of the output voltages across their operational range. Additionally, FIG. 6B indicates that the minimum operational voltage $V_{DD}$ for the circuit was 0.6 V.

FIG. 7A is a graphical representation showing a resolution and conversion time across a number of slow clock periods for a temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7A illustrates a trade-off between resolution and conversion time across different settings of the slow clock periods (M). The resolution improves (decreases in value) as M increases, indicating finer temperature differentiation capability at the cost of increased conversion time. At M=8, the resolution is 0.46 °C, achieved by counting the edges of the fast oscillator $f_{FAST}$ for 8 periods of the slow oscillator $f_{SLOW}$. The conversion time at this setting is approximately 17.6 seconds corresponding to 38.4 pW at room temperature, which is reflective of the system's operational efficiency at this specific measurement configuration. By reducing M, conversion time can be less than 10 seconds, but this comes at the expense of resolution, which would then be about 1 °C. This flexibility allows the system to be adapted based on specific application needs—faster response or finer resolution.

FIG. 7B is a graphical representation displaying frequencies of slow and fast oscillators and their ratio across a temperature range from -10 °C to 70 °C in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7B illustrates how the frequencies ($f_{SLOW}$ and $f_{FAST}$) of the slow and fast oscillators, and their ratio $f_{RATIO}$, change as the temperature varies from -10 °C to 70 °C. A very high linearity ($R^2$ = 0.9983) between the $f_{RATIO}$ and an ideal linear model ($f_{RATIO}$ linear) in the frequency response is achieved, indicating a highly predictable and reliable performance.

A readout logic complements the count to ensure that the output is correct and increasing, reflecting stable digital output behaviour across the operational temperature range. By maintaining a consistent and linear relationship between the oscillator frequencies and temperature, the system ensures minimal deviation and error in temperature readings.

FIG. 7C is a graphical representation showing noise characteristics in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7C illustrates the noise characteristics of the temperature-to-digital conversion system at a stable operating condition with a supply voltage ($V_{DD}$) of 0.6 V and temperature of 25 °C. Over 100 measurement iterations, the output logic code demonstrates a low RMS peak noise of 0.36 °C, indicating minimal fluctuation and high stability in temperature readings. The average output value is consistently recorded at 25.0046 °C, with a standard deviation ($\sigma_{code}$) of 0.78, showing the system's ability to deliver precise and reliable measurements under controlled conditions.

FIG. 7D is a graphical representation illustrating a power consumption across different supply voltages and temperatures in the temperature-to-digital conversion system, according to an embodiment of the present disclosure.

FIG. 7D illustrates the power consumption patterns of the temperature-to-digital conversion system through two separate graphs, one depicting changes with supply voltage and the other with temperature. The first graph shows a linear increase in power usage as the supply voltage rises from 0.6 V to 1.6 V at a constant temperature of 25 °C, demonstrating how power consumption scales with voltage in a manner characteristic of transistor leakage. The second graph displays a linear increase in power as the temperature ranges from -10 °C to 70 °C at a fixed voltage of 0.6 V, indicating that power consumption also scales with temperature, following a pattern similar to transistor leakage, with a slope of 16 X/°C. This slope is equivalent to 1.1 times the leakage current of a single NMOS transistor. At typical room temperature conditions, power consumption stabilizes at 38.4 pW.

FIG. 8A is a graphical representation showing temperature measurement errors of the temperature-to-digital conversion system across various process corners at a fixed supply voltage, according to an embodiment of the present disclosure.

FIG. 8A presents the errors across the different process corners (TT, FF, SS, FS, SF) over a temperature range from -10 °C to 70 °C and at the fixed supply voltage of 0.6 V.

The graph indicates that error varies with temperature, showing a general trend where errors increase at extreme temperatures for most corners. TT1, TT2, and TT3 represent the performance of three different samples from the 'Typical-Typical' (TT) process corner across

the temperature range. Different process corners exhibit different levels of stability, with TT corners showing less variation in error compared to FS and SF, which demonstrate larger errors at higher temperatures. The graph shows error ranges from -2.2 °C to 3.4 °C across corners, and from -1.7 °C to 2.9 °C among three TT corner chips.

FIG. 8B is a graphical representation showing the temperature measurement errors across a range of supply voltage levels at a constant temperature, according to an embodiment of the present disclosure. More specifically, the graph shows a sensitivity of the temperature measurement error on the supply voltage $V_{DD}$, varying from 0.6 V to 1.6 V, at a fixed temperature of 25 °C, for different process corners. The error for each corner shows different sensitivities to changes in $V_{DD}$, with error remaining relatively moderate across most corners.

FIG. 8C is a graphical representation showing an energy consumption per conversion of the temperature-to-digital conversion system across different temperatures at a fixed supply voltage $V_{DD}$, according to an embodiment of the present disclosure.

More specifically, FIG. 8C illustrates the energy consumption across a temperature range from -10 °C to 70 °C, maintained at a supply voltage of $V_{DD}$ = 0.6 V. This graph displays the variation in energy consumption per conversion for different technology corners (e.g., TT1, TT2, FF, SS, FS, SF) as the temperature changes. The energy required increases with higher temperatures, particularly noted in corners such as SF, which is represented by numeral 802 and exhibits the slowest conversion times and therefore higher energy consumption (up to 1.17 nJ at 25°C). Different corners demonstrate varying energy efficiencies, with the fast corners (FF), denoted by numeral 804, showing the lowest energy use (as low as 0.47 nJ at 25 °C), which signifies faster conversions. Although this data is less relevant for systems powered only by harvesters, it is included for completeness to assess the overall energy efficiency of the system across a range of operating conditions. For TT, FF, and FS corners, energy per conversion is shown to be less than 0.82 nJ, and for SS and SF corners, it is less than 1.17 nJ at room temperature.

FIG. 8D is a graphical representation showing a variation of a reference voltage $V_{REF}$ in the temperature-to-digital conversion system across temperatures from -10 °C to 70 °C at a fixed supply voltage $V_{DD}$, according to an embodiment of the present disclosure. The graph of FIG. 8D provides a Temperature Coefficient (TC) of $V_{REF}$ across temperatures, with each corner showing different stability levels. For example, The SS (Stable-Slow) corner exhibits the lowest TC at 146 ppm/°C, indicating the most stable performance. TT samples—TT1, TT2, and TT3—show different levels of stability with TCs of 194 ppm/°C, 230 ppm/°C, and 267 ppm/°C respectively, pointing to variations even within the same manufacturing specification. The SF (Slow-Fast) corner shows a TC of 186 ppm/°C. The FS (Fast-Slow) and FF (Fast-Fast) corners

exhibit higher instabilities with TCs of 325 ppm/°C and 361 ppm/°C respectively, indicating that devices from these corners might experience greater shifts in reference voltage with temperature changes. The inherently available reference voltage in these systems has an average temperature coefficient $\mu_{TC}$ of 244 ppm/°C (33 µV/°C) across all corners. The standard deviation $\sigma_{TC}$ is 72 ppm/°C or 8.2 µV/°C, which measures the variability of this temperature sensitivity across different samples or process corners.

FIG. 9 is a micrograph 900 of a test chip used in the temperature-to-digital conversion system, according to an embodiment of the present disclosure. It illustrates a distribution and organization of key components on the chip: it highlights an area of 119 kµm² dedicated to logic blocks that manage calibration and counters, including both FSLOW and FFAST counters, which are important for accurate temperature measurements. Adjacent to this, a compact and specialized 21 kµm² section is allocated for temperature-to-voltage conversion alongside voltage-to-frequency oscillators, which is important for the conversion process from temperature changes to digital signals.

Based on benchmarking and testing, the temperature sensor of the present disclosure may operate with a supply voltage range from 0.6 to 1.6 V and in a temperature range of -10 to 70 °C, utilizing a 180 nm technology process and occupying a minimal area of 0.14 mm². Notably, it can achieve an extremely low power consumption of 38.4 pW, significantly lower by 3-20 times than comparable sensors currently available, and maintains a power efficiency of 64.7 pW under most demanding conditions (FF corner), which is more than 1.8 times better than the lowest previously reported figures. Additionally, this sensor can offer a resolution of 0.49 °C, competitive with sensors operating below the nano-Watt level, but without the complexity of voltage regulation, streamlining both the design and operation.

Furthermore, it maintains an accuracy range of -1.7 to 2.9 °C, demonstrating robustness across different manufacturing conditions as it includes measurements at corner wafers (FF, SS, TT, FS, SS). The sensor may be configured to require a voltage reference but does not need a current reference or voltage regulation, distinguishing it from many others that require more complex support circuitry. Its calibration employs a 2-point method, enhancing its accuracy and reliability. The sensor may be configured to receive power from a 3 mm by 3 mm solar cell down to 1 lux (near-dark). This combination of low-power consumption, minimal external dependencies, and robust performance makes the sensor particularly suitable for applications demanding high efficiency and compactness.

FIG. 10 is a flowchart 1000 illustrating a method for converting temperature into digital data according to an embodiment of the present disclosure. FIG. 10 sequentially outlines the steps

involved in processing temperature measurements into a digital format representative of the temperature:

In step 1002, temperature is converted into a plurality of temperature-dependent voltage signals via a plurality of sensors, wherein each voltage signal is independent, proportional, or inversely proportional to changes in the temperature. This step initiates the process 1000 by capturing ambient temperature through sensors and converting it into corresponding voltage signals.

In step 1004, a first voltage signal that is proportional to changes in temperature at a first oscillator is received and a first frequency based on the first voltage signal is outputted using the first oscillator. Here, the method 1000 continues by processing the first voltage signal through the first oscillator, which then generates a frequency directly related to the temperature.

In step 1006, a second voltage signal that is inversely proportional to changes in temperature at a second oscillator is received and a second frequency based on the second voltage signal is outputted using the second oscillator. This step processes the second voltage signal via the second oscillator to produce a frequency inversely related to the temperature changes.

In step 1008, a voltage level corresponding to the first frequency is adjusted using a first level shifter and a voltage level corresponding to the second frequency is adjusted using a second level shifter. Adjustment of voltage levels is performed here to match the frequencies derived from the first and second oscillators, preparing them for digital conversion.

In step 1010, the adjusted first and second voltage levels are received at a digital conversion module. This step involves the digital conversion module receiving the voltage levels that have been adjusted by the first and second level shifters.

In step 1012, the adjusted first and second voltage levels are converted into a digital output representative of the temperature using the digital conversion module. The final step in this method includes converting the received and adjusted voltage levels into a digital format that accurately represents the ambient temperature.

Whilst the foregoing description has described exemplary embodiments, it will be understood by those skilled in the art that many variations of the embodiments can be made within the scope of the invention as defined by the claims. Moreover, features of one or more embodiments may be mixed and matched with features of one or more other embodiments.

Claims:

1. A temperature-to-digital conversion system, comprising:

a plurality of sensors configured to convert a temperature into a plurality of voltage signals, wherein each voltage signal is independent, proportional, or inversely proportional to changes in the temperature.

a first oscillator configured to receive a first voltage signal that is proportional to changes in temperature and output a first frequency based on the first voltage signal;

a second oscillator configured to receive a second voltage signal that is inversely proportional to changes in temperature and output a second frequency based on the second voltage signal;

a first level shifter configured to adjust a first voltage level corresponding to the first frequency;

a second level shifter configured to adjust a second voltage level corresponding to the second frequency; and

a digital conversion module configured to receive the adjusted first and second voltage levels and convert the adjusted voltage levels into a digital output representative of the temperature.

2. The system of claim 1, wherein each sensor is configured to convert the temperature into the plurality of the voltage signals in a manner that is nearly-independent of variations in supply voltage.

3. The system of claim 1 or 2, wherein each of the first and second oscillator is a ring oscillator configured to utilize dynamic leakage suppression logic to reduce power leakage.

4. The system of any one of the preceding claims, wherein the digital conversion module includes a counter and calibration logic configured for dual-edge triggered counting in order to determine a plurality of temperature measurements.

5. The system of any one of the preceding claims, wherein each sensor comprises a basic cell or a variant thereof, wherein the basic cell includes a pair of transistors configured to carry equal current.

6. The system of claim 5, wherein the pair of transistors comprise of a zero-VGS transistor and a diode-connected transistor.

7. The system of claim 5, wherein the variant of the basic cell corresponds to a current mirror arrangement for outputting the first voltage signal.

8. The system of claim 5, wherein the variant of the basic cell corresponds to a bipolar-junction transistor arrangement for outputting the second voltage signal.

9. The system of claim 8, wherein the bipolar-junction transistor arrangement is a substitute for a diode-connected transistor of the basic cell.

10. The system of any one of the preceding claims, wherein at least one of the first and second level shifters comprises a configuration having a current mirror arrangement and an output transistor with a modified body connection, wherein the configuration achieves a full voltage swing at an output of each level shifter.

11. The system of any one of the preceding claims, wherein at least one of the first and second level shifters employ a voltage droop technique using one or more transistors configured within a current mirror arrangement for enhancing a voltage swing at an output of each level shifter.

12. The system of any one of the preceding claims, wherein at least one of the first and second level shifters incorporates transistors configured as Low Voltage Threshold (LVT) devices.

13. The system of any one of the preceding claims, wherein each of the first and second oscillators is configured as a five-stage ring oscillator that employs Dynamic Leakage Suppression (DLS) logic.

14. The system of any one of the preceding claims, wherein the first frequency varies exponentially with temperature and the first voltage signal, and the second frequency varies with temperature and in relation to the second voltage signal, wherein each of the first and second frequencies are modulated by a body effect coefficient to linearize their responses to temperature variations.

15. The system of any one of the preceding claims, wherein each of the first and second oscillators employ a voltage control mechanism through body terminals of their transistors to modulate their respect frequency outputs.

16. A method for converting temperature into digital data, comprising:

converting a temperature into a plurality of temperature-dependent voltage signals via a plurality of sensors, wherein each voltage signal is independent, proportional, or inversely proportional to changes in the temperature;

receiving a first voltage signal that is proportional to changes in temperature at a first oscillator and outputting a first frequency based on this first voltage signal using the first oscillator;

receiving a second voltage signal that is inversely proportional to changes in temperature at a second oscillator and outputting a second frequency based on this second voltage signal using the second oscillator;

adjusting a voltage level corresponding to the first frequency using a first level shifter;

adjusting a voltage level corresponding to the second frequency using a second level shifter;

receiving the adjusted first and second voltage levels at a digital conversion module; and

converting the adjusted voltage levels into a digital output representative of the temperature using the digital conversion module.

17. A system for temperature-to-digital conversion, comprising:

a first circuit for providing a first output voltage that is constant with temperature;

a second circuit for providing a second output voltage that is proportional to temperature and providing a third output voltage that is inversely proportional to temperature;

a level shifter for adapting voltage levels within the system;

two ring oscillators composed by body terminal-controlled logic gates to perform a voltage-to-frequency conversion for generating frequency information; and

a digital block for converting the frequency information to a digital code.

18. The system of claim 16, further comprising a plurality of regulation components, wherein the plurality of regulation components includes a NMOS-only transistor voltage reference configured to perform implicit voltage regulation.

19. A system comprising:

an oscillator system configured to perform voltage-to-frequency conversion including a first oscillator and a second oscillator, wherein each oscillator is powered by a first output voltage constant with temperature from a first circuit and controlled by a second output

voltage that is proportional to temperature from a second circuit or a third output voltage that is inversely proportional to temperature from a third circuit; and

a level shifter configured to adapt voltage levels corresponding to the outputs of the first oscillator and the second oscillator to voltage levels suitable for digital processing;

20. The system of claim 19, further comprising a readout logic for converting the adapted voltage levels from the level shifter to a digital format.

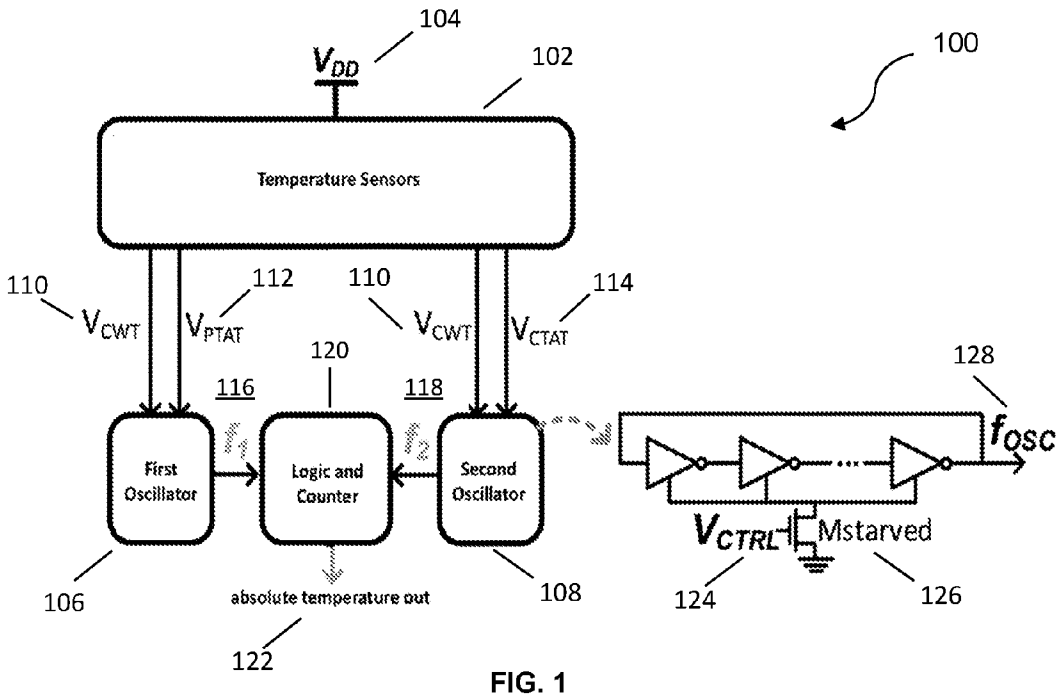

104
$V_{DD}$
102
100
Temperature Sensors
110
$V_{CWT}$
112
$V_{PTAT}$
110
$V_{CWT}$
114
$V_{CTAT}$
120
116
118
128
First Oscillator
Logic and Counter
Second Oscillator
$f_{OSC}$
$V_{CTRL}$
Mstarved
106
absolute temperature out
108
124
126
122

FIG. 1

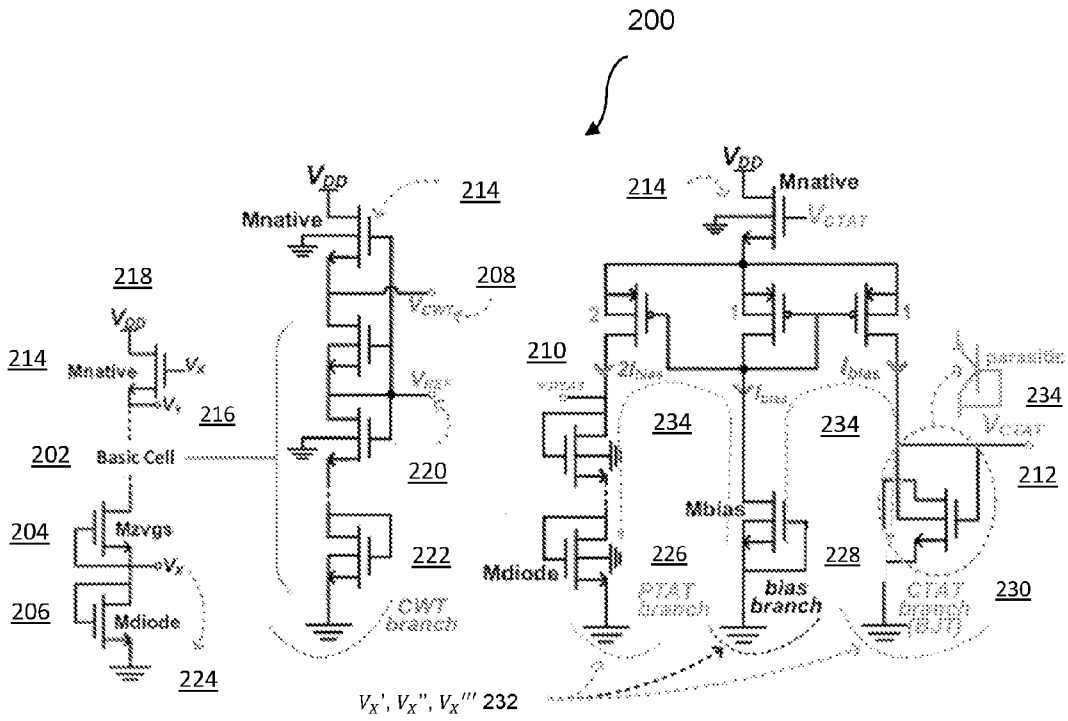

200
$V_{DD}$
214
Mnative
208
$V_{CWT}$
218
$V_{DD}$
214
Mnative
$V_X$
$V_Y$
216
202
Basic Cell
220
204
Mavgs
$V_X$
206
Mdiode
222
224
CWT branch
$V_X'$, $V_X''$, $V_X'''$ 232
$V_{DD}$
214
Mnative
$V_{CTAT}$
210
$2I_{bias}$
$I_{bias}$
$V_{PTAT}$
$V_{bias}$
234
234
Parasitic
234
$V_{CTAT}$
212
Mbias
Mdiode
226
228
230
PTAT branch
bias branch
CTAT branch

FIG. 2

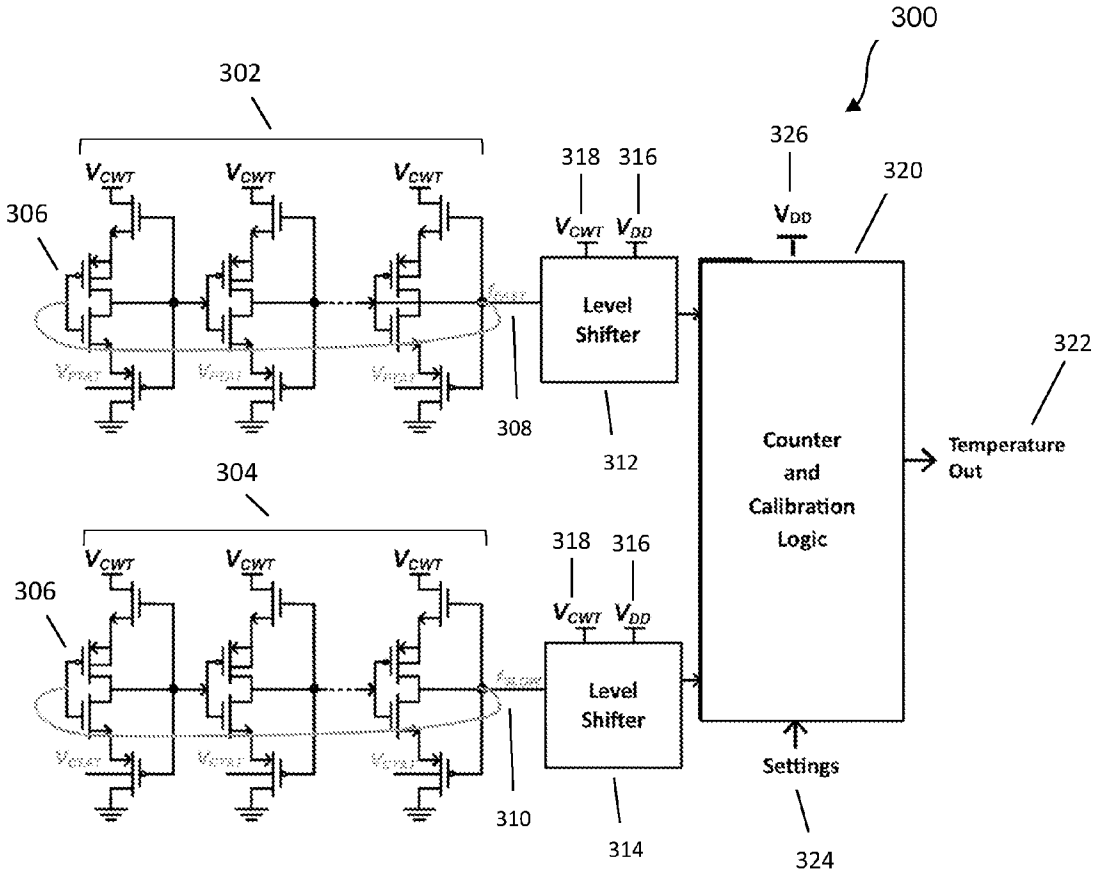

300
302
304
306
306
$V_{CWT}$
$V_{DD}$
318
316
326
320
322
308
310
312
314
324
Level Shifter
Level Shifter
Counter and Calibration Logic
Temperature Out
Settings

FIG. 3

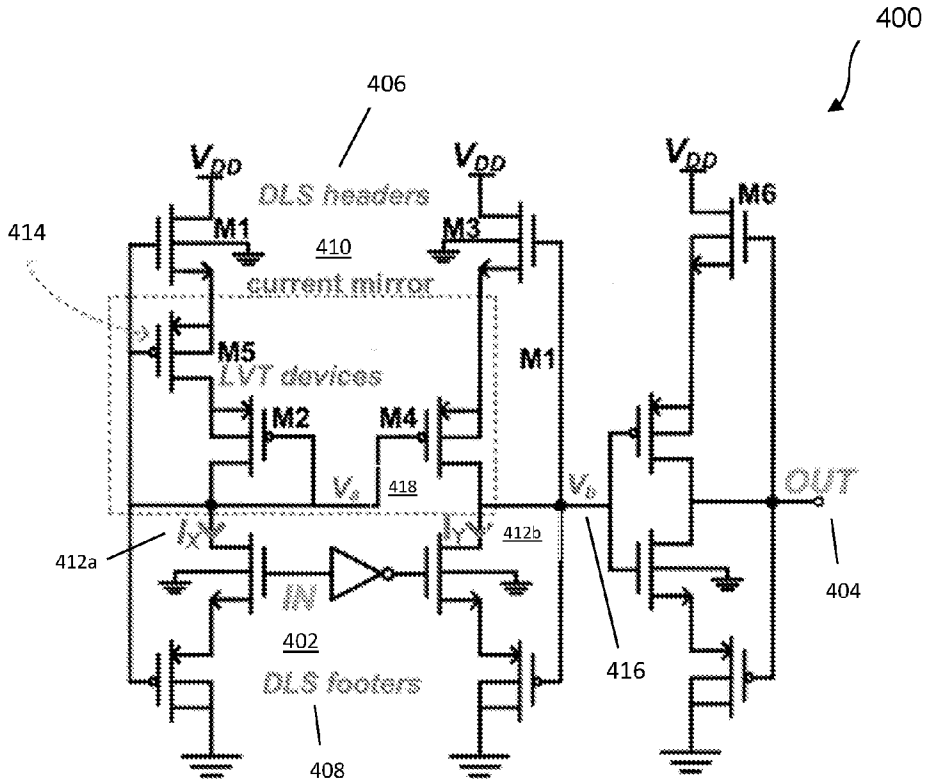

400
406
$V_{DD}$
$V_{DD}$
$V_{DD}$
DLS headers
M1
410
M3
M6
414
current mirror
M5
LVT devices
M1
M2
M4
$V_a$
418
$V_b$
OUT
$I_X$
$I_Y$
412b
412a
IN
402
404
416
DLS footers
408

FIG. 4

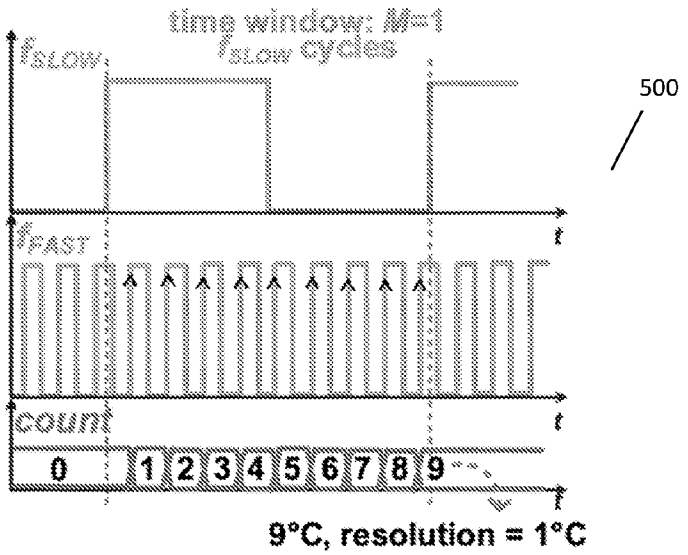

time window: M=1
$f_{SLOW}$ cycles
$f_{SLOW}$
500
$f_{FAST}$
t
count
t
0 1 2 3 4 5 6 7 8 9
t
9°C, resolution = 1°C

FIG. 5A

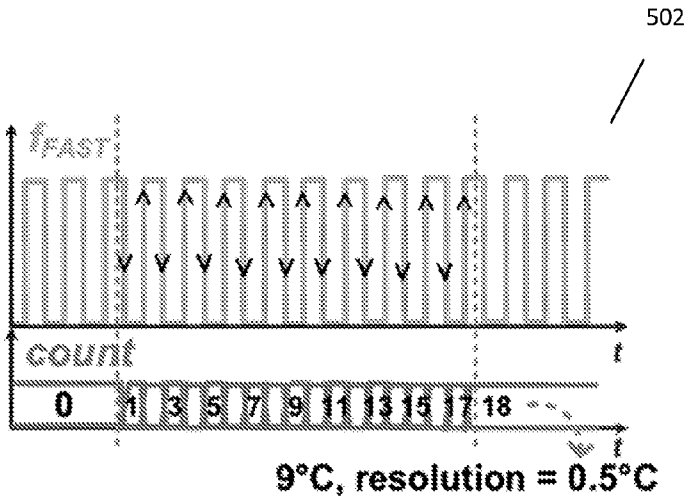

502
$f_{FAST}$
count
t
0 1 3 5 7 9 11 13 15 17 18
t
9°C, resolution = 0.5°C

FIG. 5B

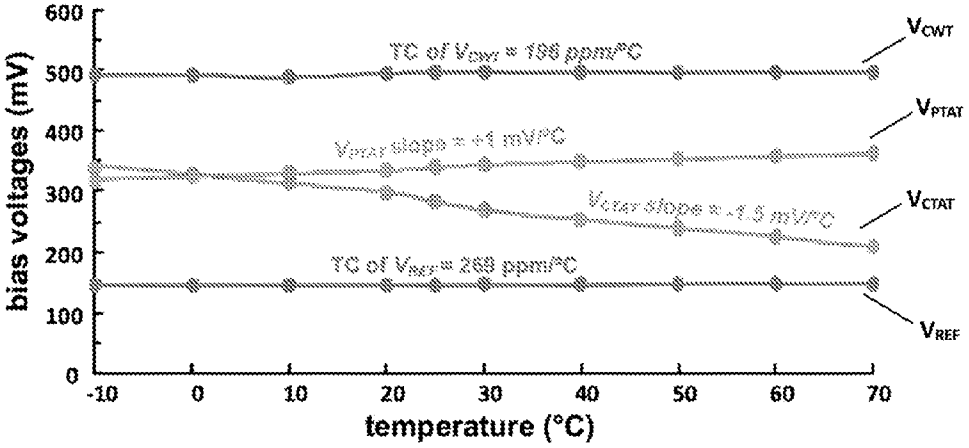

bias voltages (mV)
temperature (°C)
TC of $V_{CWT}$ = 196 ppm/°C
$V_{PTAT}$ slope = +1 mV/°C
$V_{CTAT}$ slope = -1.3 mV/°C
TC of $V_{REF}$ = 269 ppm/°C
$V_{CWT}$
$V_{PTAT}$
$V_{CTAT}$
$V_{REF}$

FIG. 6A

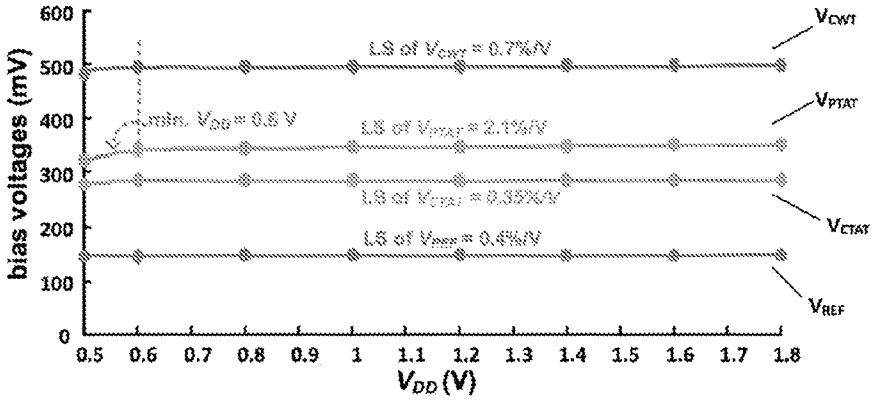

bias voltages (mV)
$V_{DD}$ (V)
LS of $V_{CWT}$ = 0.7%/V
$V_{DD}$ min. = 0.6 V
LS of $V_{PTAT}$ = 2.1%/V
LS of $V_{CTAT}$ = 0.39%/V
LS of $V_{REF}$ = 0.4%/V
$V_{CWT}$
$V_{PTAT}$
$V_{CTAT}$
$V_{REF}$

FIG. 6B

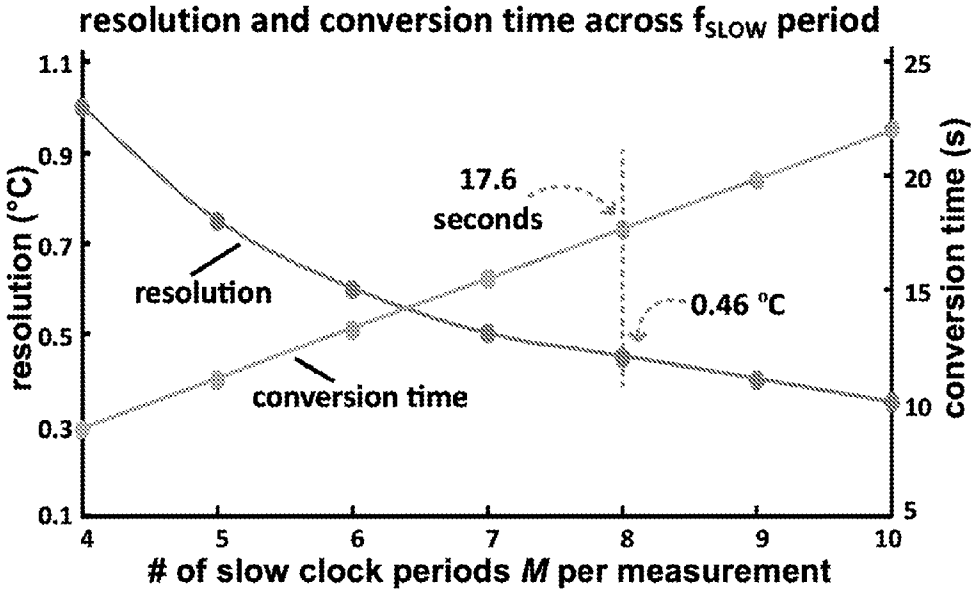

resolution and conversion time across $f_{SLOW}$ period
resolution (°C)
conversion time (s)
17.6
seconds
resolution
0.46 °C
conversion time
# of slow clock periods M per measurement

FIG. 7A

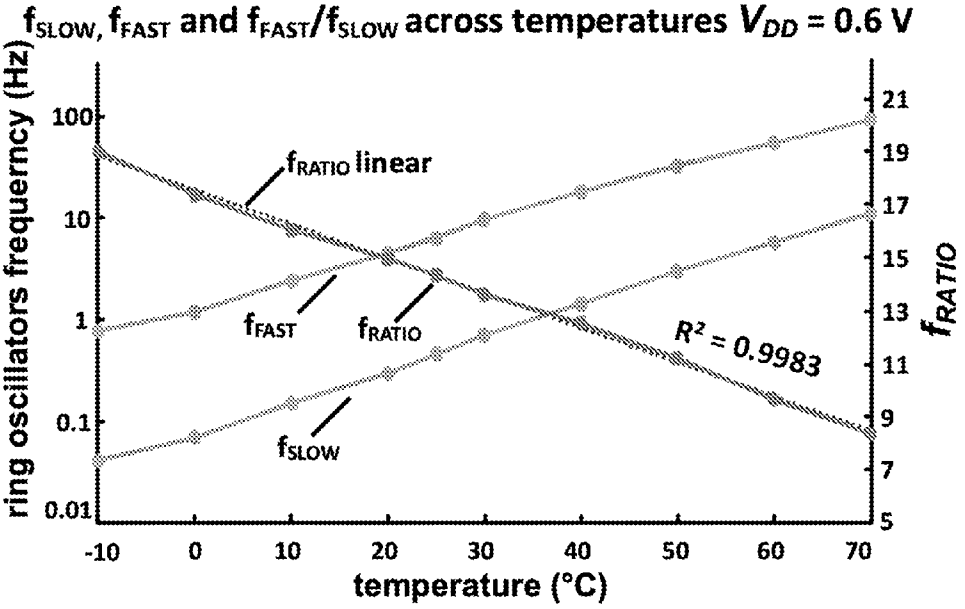

$f_{SLOW}$, $f_{FAST}$ and $f_{FAST}/f_{SLOW}$ across temperatures $V_{DD}$ = 0.6 V
ring oscillators frequency (Hz)
$f_{RATIO}$
$f_{RATIO}$ linear
$f_{FAST}$
$f_{RATIO}$
$R^2$ = 0.9983
$f_{SLOW}$
temperature (°C)

FIG. 7B

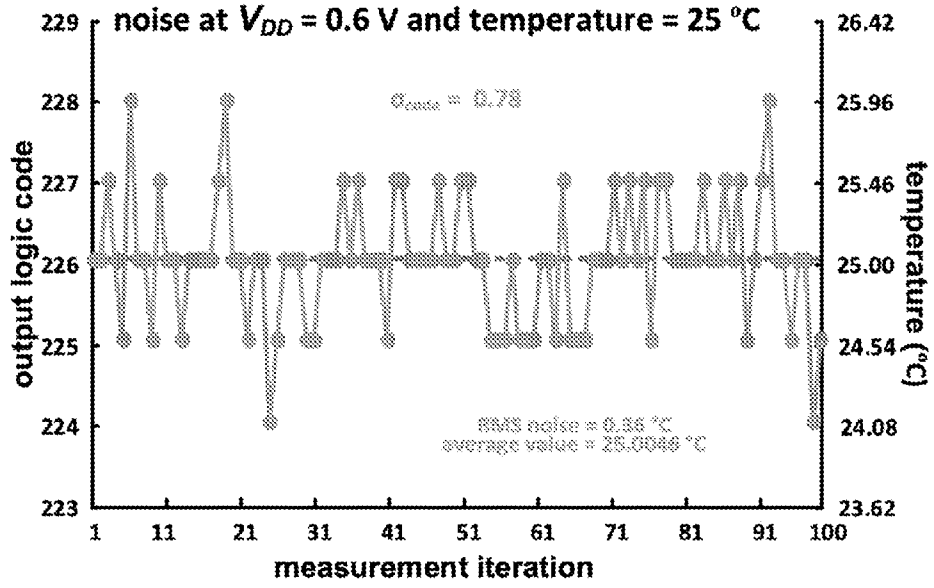

noise at $V_{DD}$ = 0.6 V and temperature = 25 °C
$\sigma_{code}$ = 0.78
RMS noise = 0.36 °C
average value = 25.0046 °C
output logic code
temperature (°C)
measurement iteration
229
228
227
226
225
224
223
26.42
25.96
25.46
25.00
24.54
24.08
23.62
1
11
21
31
41
51
61
71
81
91
100

FIG. 7C

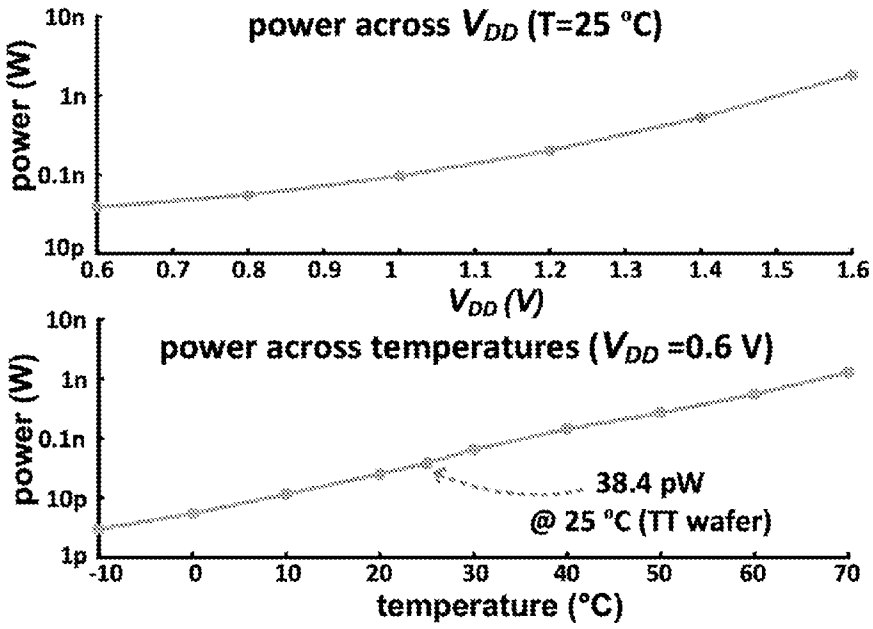

power across $V_{DD}$ (T=25 °C)
power (W)
$V_{DD}$ (V)
power across temperatures ($V_{DD}$ =0.6 V)
38.4 pW
@ 25 °C (TT wafer)
temperature (°C)
10n
1n
0.1n
10p
1p
0.6
0.7
0.8
0.9
1
1.1
1.2
1.3
1.4
1.5
1.6
-10
0
10
20
30
40
50
60
70

FIG. 7D

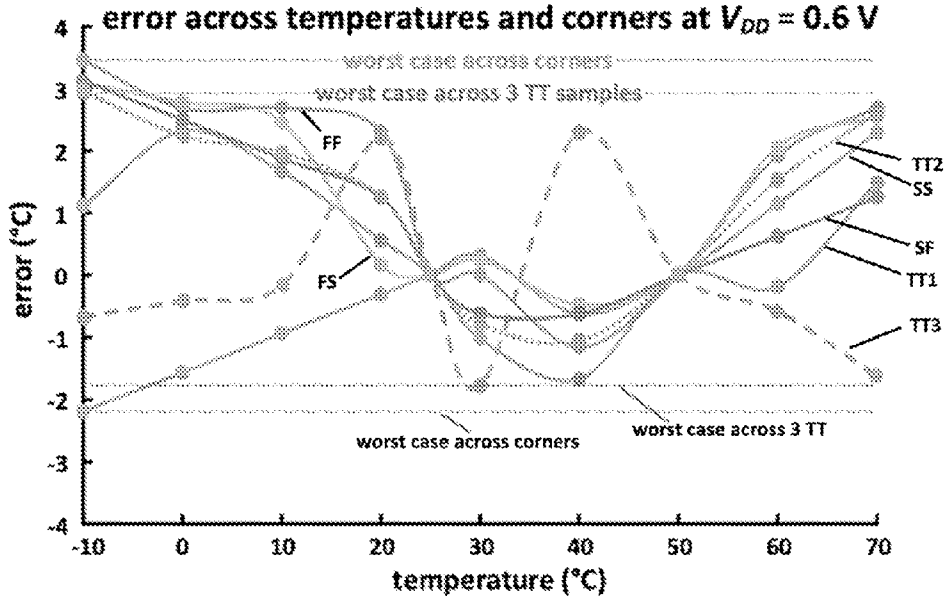

error across temperatures and corners at $V_{DD}$ = 0.6 V
worst case across corners
worst case across 3 TT samples
FF
FS
TT2
SS
SF
TT1
TT3
worst case across corners
worst case across 3 TT
error (°C)
temperature (°C)
4
3
2
1
0
-1
-2
-3
-4
-10
0
10
20
30
40
50
60
70

FIG. 8A

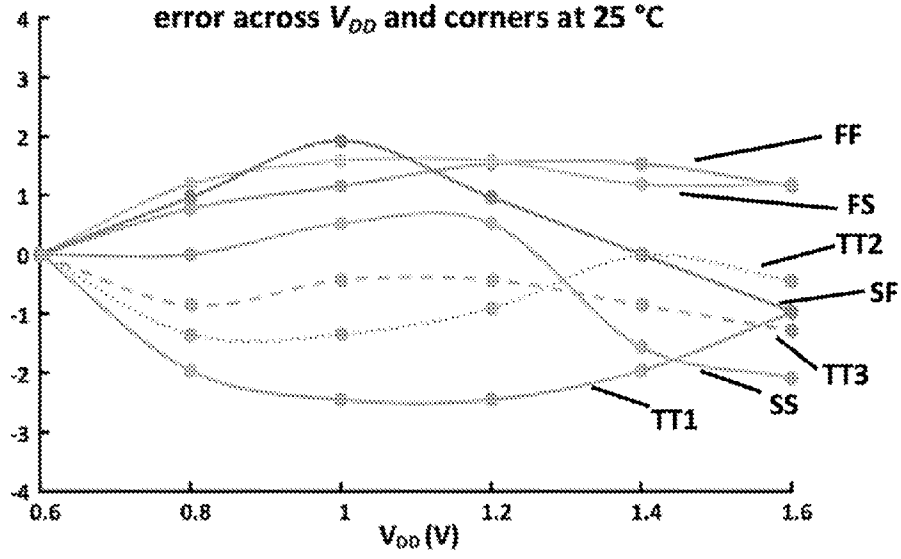

error across $V_{DD}$ and corners at 25 °C
FF
FS
TT2
SF
TT3
SS
TT1
$V_{DD}$ (V)
4
3
2
1
0
-1
-2
-3
-4
0.6
0.8
1
1.2
1.4
1.6

FIG. 8B

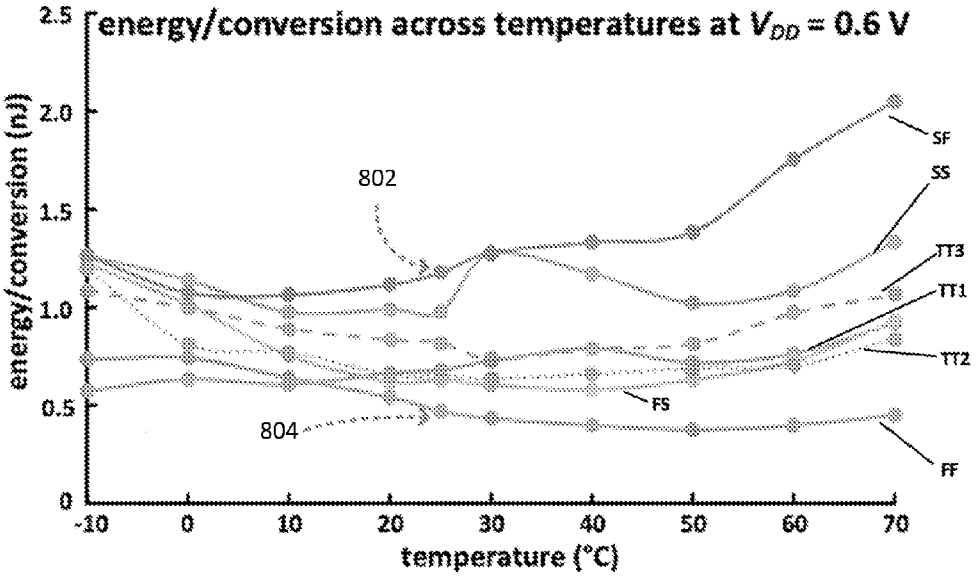

energy/conversion across temperatures at $V_{DD}$ = 0.6 V
energy/conversion (nJ)
temperature (°C)
802
804
SF
SS
TT3
TT1
TT2
FS
FF

FIG. 8C

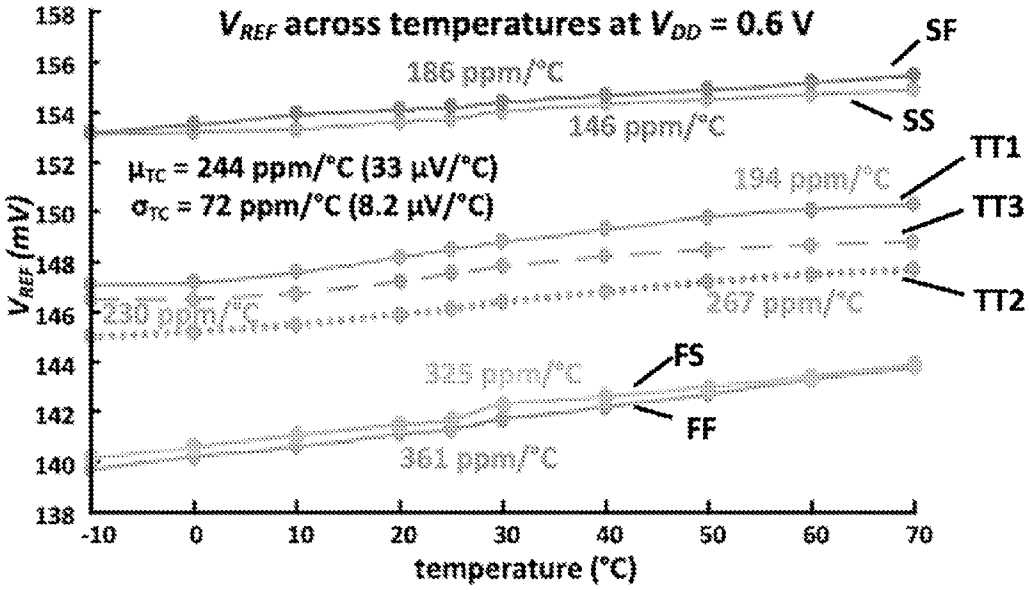

$V_{REF}$ across temperatures at $V_{DD}$ = 0.6 V
$V_{REF}$ (mV)
temperature (°C)
$\mu_{TC}$ = 244 ppm/°C (33 µV/°C)
$\sigma_{TC}$ = 72 ppm/°C (8.2 µV/°C)
186 ppm/°C
146 ppm/°C
194 ppm/°C
230 ppm/°C
267 ppm/°C
325 ppm/°C
361 ppm/°C
SF
SS
TT1
TT3
TT2
FS
FF

FIG. 8D

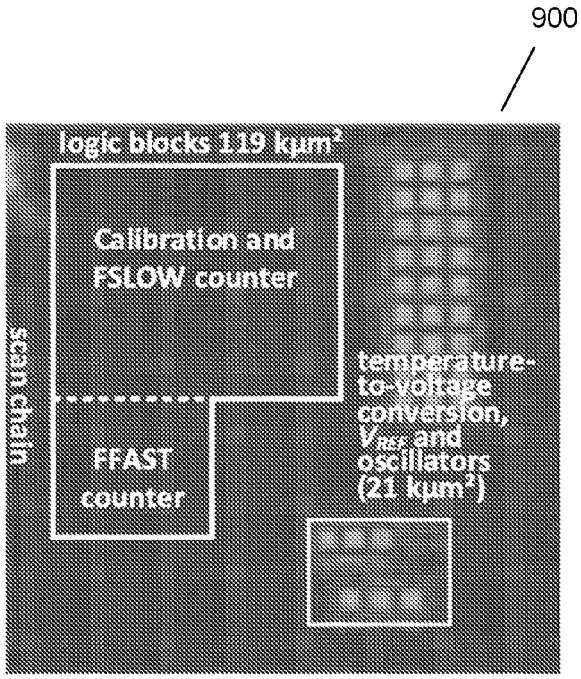

900
logic blocks 119 kum²
Calibration and FSLOW counter
FFAST counter
scan chain
temperature-to-voltage conversion, V_REF and oscillators (21 kum²)

FIG. 9

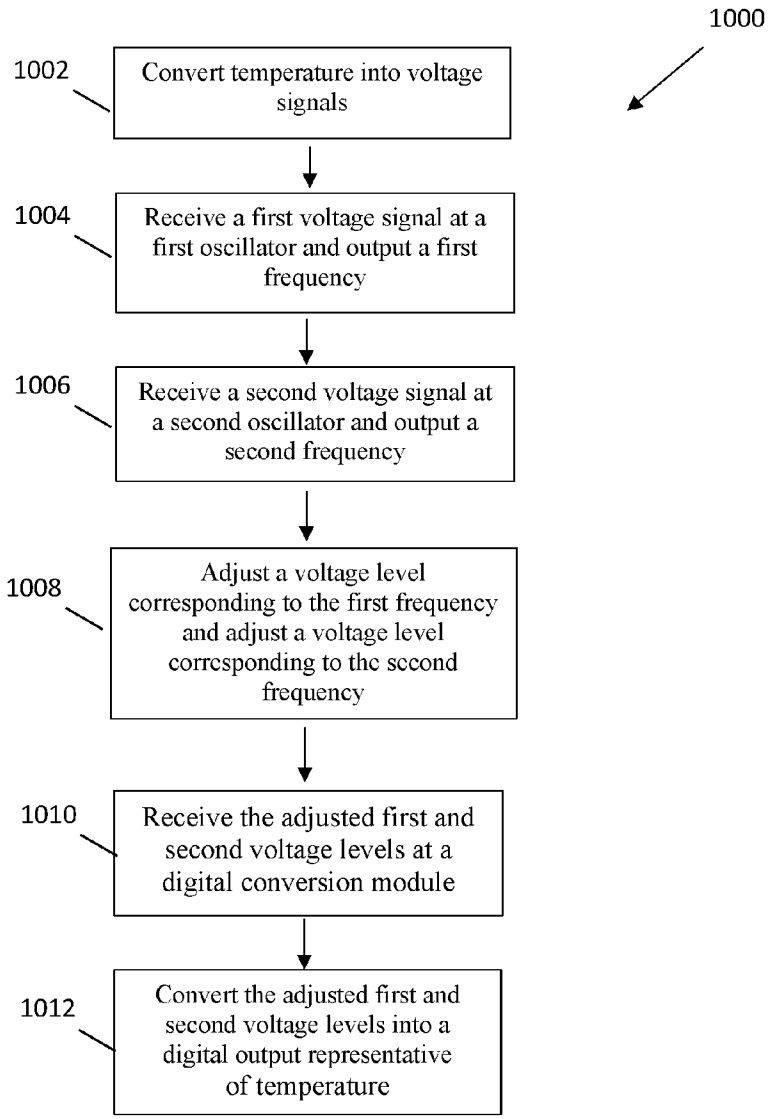

1000
1002
Convert temperature into voltage signals
1004
Receive a first voltage signal at a first oscillator and output a first frequency
1006
Receive a second voltage signal at a second oscillator and output a second frequency
1008
Adjust a voltage level corresponding to the first frequency and adjust a voltage level corresponding to the second frequency
1010
Receive the adjusted first and second voltage levels at a digital conversion module
1012
Convert the adjusted first and second voltage levels into a digital output representative of temperature

FIG. 10

# INTERNATIONAL SEARCH REPORT

International application No.
**PCT/SG2024/050375**

## A. CLASSIFICATION OF SUBJECT MATTER

***G01K 7/01 (2006.01)*** *H03M 1/12 (2006.01)*

According to International Patent Classification (IPC)

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01K, H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

FAMPAT, Google Scholar, IEEE Xplore: temperature, thermal, thermometer, sensor, detector, conversion, digital, voltage, signal, output, proportional, linear, PTAT, inverse, complementary, CTAT, absolute, oscillator, frequency, level shifter, adjust, and related terms.

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>A | US 2015/0300889 A1 (RAMARAJU, R. ET AL.) 22 October 2015<br>Para. [0017]-[0018], [0021]-[0042], Fig. 4-5 | 1-9, 13-20<br>10-12 |
| A | KUMAR, M. ET AL., Low Power Voltage Controlled Ring Oscillator Designwith Substrate Biasing. *International Journal of Information and Electronics Engineering*, 31 March 2012, Vol. 2, No. 2, pages 156-159<br>[Retrieved on 2024-07-29] <DOI: 10.7763/IJIEE.2012.V2.72><br>Whole document | |
| A | VINSHTOK-MELNIK, N. ET AL., Ultra Miniature 1850 μm$^2$ Ring Oscillator Based Temperature Sensor. *IEEE Access*, 14 May 2020, Vol. 8, pages 91415-91423<br>[Retrieved on 2024-07-29] <DOI: 10.1109/ACCESS.2020.2994326><br>Whole document | |

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 29/07/2024 *(day/month/year)* | 30/07/2024 *(day/month/year)* |


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# INTERNATIONAL SEARCH REPORT

International application No.
**PCT/SG2024/050375**

**C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 2020/0149975 A1 (CHO, S. H. ET AL.) 14 May 2020<br>Whole document | |
| A | CN 115638888 A (UNIV FUZHOU) 24 January 2023<br>Whole document of the original non-English language document (a machine translation is enclosed **only** for your reference) | |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

**PCT/SG2024/050375**

*Note: This Annex lists known patent family members relating to the patent documents cited in this International Search Report. This Authority is in no way liable for these particulars which are merely given for the purpose of information.*

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2015/0300889 A1 | 22/10/2015 | NONE | |
| US 2020/0149975 A1 | 14/05/2020 | US 2015/0063420 A1<br>US 2018/0128690 A1<br>KR 20150027413 A | 05/03/2015<br>10/05/2018<br>12/03/2015 |
| CN 115638888 A | 24/01/2023 | NONE | |