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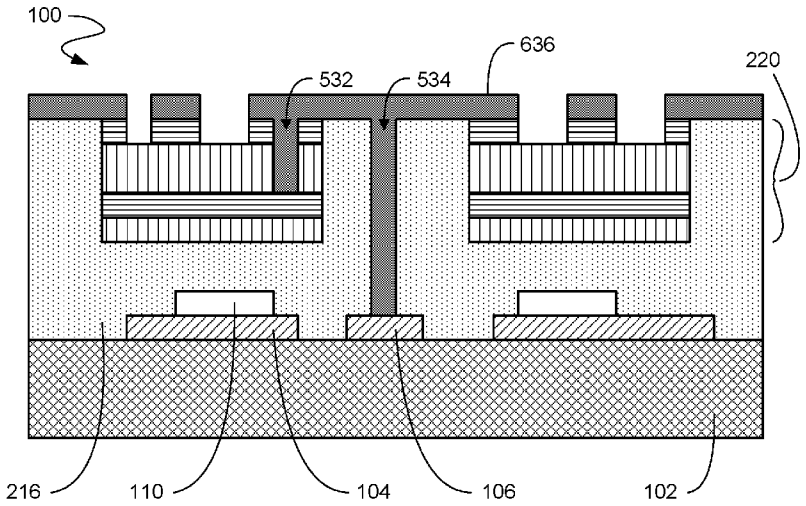


FIG. 6

(57) Abstract: Provided herein is a method including bonding a first oxide layer on a handle substrate to a second oxide layer on a complementary metal oxide semiconductor ("CMOS"), wherein the fusion bonding forms a unified oxide layer including a diaphragm overlying a cavity on the CMOS. The handle substrate is removed leaving the unified oxide layer. A piezoelectric film stack is deposited over the unified oxide layer. Vias are formed in the piezoelectric film stack and the unified oxide layer. An electrical contact layer is deposited, wherein the electrical contact layer electrically connects the piezoelectric film stack to an electrode on the CMOS.

INTEGRATION OF AIN ULTRASONIC TRANSDUCER ON A CMOS SUBSTRATE USING FUSION BONDING PROCESS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit and priority to the U.S. Provisional Patent Application Serial No. 62/312,439 filed March 23, 2016, entitled "AIN PMUT SENSOR MODULE INTEGRATION METHOD", which is incorporated by reference in its entirety.

BACKGROUND

[0002] Piezoelectric materials convert energy between mechanical energy and electrical energy. A piezoelectric material generates electrical energy when mechanically deformed (e.g. under mechanical stress). On the other hand, a piezoelectric material may mechanically deform in response to electrical energy. For example, a piezoelectric material may vibrate in response to electrical energy, thereby acting as an ultrasonic transducer to generate acoustic waves. Piezoelectric materials may be used in micro-electro-mechanical system ("MEMS") devices, for example, in fingerprint recognition.

SUMMARY

[0003] Provided herein is a method including bonding a first oxide layer on a handle substrate to a second oxide layer on a complementary metal oxide semiconductor ("CMOS"), wherein the fusion bonding forms a unified oxide layer including a diaphragm overlying a cavity on the CMOS. The handle substrate is removed leaving the unified oxide layer. A piezoelectric film stack is deposited over the unified oxide layer. Vias are formed in the piezoelectric film stack and the unified oxide layer. An electrical contact layer is deposited, wherein the electrical contact layer electrically connects the piezoelectric film stack to an

electrode on the CMOS. These and other features and advantages will be apparent from a reading of the following detailed description.

BRIEF DESCRIPTION OF DRAWINGS

[0004] Figure 1 shows an integrated pMUT on CMOS at an early stage of manufacture according to one aspect of the present embodiments.

[0005] Figure 2 shows the integrated pMUT on CMOS after fusion bonding and removal of the carrier substrate according to one aspect of the present embodiments.

[0006] Figure 3 shows the integrated pMUT on CMOS after piezoelectric film stack deposition and patterning according to one aspect of the present embodiments.

[0007] Figure 4 shows the integrated pMUT on CMOS after gap fill oxide has been deposited and planarized according to one aspect of the present embodiments.

[0008] Figure 5 shows the integrated pMUT on CMOS after formation of a first electrical contact via and a second electrical contact via according to one aspect of the present embodiments.

[0009] Figure 6 shows the integrated pMUT on CMOS after deposition and patterning of an electrical contact layer according to one aspect of the present embodiments.

[0010] Figure 7 shows another integrated pMUT on CMOS at an early stage of manufacture according to one aspect of the present embodiments.

[0011] Figure 8 shows the integrated pMUT on CMOS after fusion bonding and removal of the carrier substrate according to one aspect of the present embodiments.

[0012] Figure 9 shows the integrated pMUT on CMOS after piezoelectric film stack patterning and deposition of gap fill oxide according to one aspect of the present embodiments.

[0013] Figure 10 shows the integrated pMUT on CMOS after formation of a first electrical contact via and a second electrical contact via according to one aspect of the present embodiments.

[0014] Figure 11 shows the integrated pMUT on CMOS after deposition and patterning of an electrical contact layer according to one aspect of the present embodiments.

[0015] Figure 12 shows an exemplary flow diagram for an integration of pMUT on CMOS according to one aspect of the present embodiments.

[0016] Figure 13 shows an exemplary flow diagram for another integration of pMUT on CMOS according to one aspect of the present embodiments.

DESCRIPTION

[0017] Before various embodiments are described in greater detail, it should be understood that the embodiments are not limiting, as elements in such embodiments may vary. It should likewise be understood that a particular embodiment described and/or illustrated herein has elements which may be readily separated from the particular

embodiment and optionally combined with any of several other embodiments or substituted for elements in any of several other embodiments described herein.

[0018] It should also be understood that the terminology used herein is for the purpose of describing the certain concepts, and the terminology is not intended to be limiting. Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood in the art to which the embodiments pertain.

[0019] Unless indicated otherwise, ordinal numbers (e.g., first, second, third, etc.) are used to distinguish or identify different elements or steps in a group of elements or steps, and do not supply a serial or numerical limitation on the elements or steps of the embodiments thereof. For example, "first," "second," and "third" elements or steps need not necessarily appear in that order, and the embodiments thereof need not necessarily be limited to three elements or steps. It should also be understood that, unless indicated otherwise, any labels such as "left," "right," "front," "back," "top," "middle," "bottom," "beside," "forward," "reverse," "overlying," "underlying," "up," "down," or other similar terms such as "upper," "lower," "above," "below," "under," "between," "over," "vertical," "horizontal," "proximal," "distal," and the like are used for convenience and are not intended to imply, for example, any particular fixed location, orientation, or direction. Instead, such labels are used to reflect, for example, relative location, orientation, or directions. It should also be understood that the singular forms of "a," "an," and "the" include plural references unless the context clearly dictates otherwise.

[0020] Terms such as "over," "overlying," "above," "under," etc. are understood to refer to elements that may be in direct contact or may have other elements in-between. For example, two layers may be in overlying contact, wherein one layer is over another layer and

the two layers physically contact. In another example, two layers may be separated by one or more layers, wherein a first layer is over a second layer and one or more intermediate layers are between the first and second layers, such that the first and second layers do not physically contact.

[0021] Piezoelectric ultrasonic transducers have been miniaturized to form a MEMS device, referred to as a piezoelectric micromachined ultrasonic transducer ("pMUT"). MEMS pMUT wafers may be eutecticly bonded to CMOS wafers, however such processes can be costly. In addition, integration of CMOS and MEMS pMUT wafers is limited by alignment accuracy tolerances between structures. Accordingly, a need has arisen to reduce the cost of CMOS and MEMS pMUT wafer integration, as well as improving alignment tolerances. Embodiments described herein address such needs by integrating a pMUT directly on a CMOS substrate using fusion bonding processes.

[0022] Referring now to Figure 1, an integrated pMUT on CMOS 100 at an early stage of manufacture is shown according to one aspect of the present embodiments. A CMOS substrate 102 has been formed with a first metal electrode 104 and a second metal electrode 106 on the CMOS substrate 102. A first fusion bond oxide 108 is deposited over the CMOS substrate 102, the first metal electrode 104 and the second metal electrode 106. A cavity 110 is formed in the first fusion bond oxide 108, located over the first metal electrode 104. In various embodiments, one or more cavities 110 may be formed over one or more first metal electrodes 104. At this stage of manufacture, the second metal electrode 106 remains covered by the first fusion bond oxide 108. It is understood that the CMOS substrate 102 includes many CMOS structures including, but not limited to, integrated circuit(s), transistor(s), substrate(s), electrical connection(s), metal electrode(s), the fusion bond oxide, etc.

[0023] A carrier substrate 112 (e.g. handle substrate) includes a second fusion bond oxide 114. The second fusion bond oxide 114 may be the same material as the first fusion bond oxide 108 or a different material. In various embodiments, the carrier substrate 112 (e.g. handle substrate) and the second fusion bond oxide 114 do not contain any metal, and no features have been formed (e.g. no patterning) in either the carrier substrate 112 or the second fusion bond oxide 114.

[0024] Referring now to Figure 2, the integrated pMUT on CMOS 100 after fusion bonding and removal of the carrier substrate 112 is shown according to one aspect of the present embodiments. The first fusion bond oxide 108 and the second fusion bond oxide 114 have been fusion bonded together to form a unified oxide layer 216. The unified oxide layer 216 encloses the cavity 110, thereby forming a membrane 218 (e.g. diaphragm) over the cavity 110 and a portion of the first metal electrode 104. After the fusion bonding and formation of the unified oxide layer 216, the carrier substrate 112 is removed (e.g. by grinding, etching, etc.) leaving the unified oxide layer 216 over the CMOS substrate 102.

[0025] Referring now to Figure 3, the integrated pMUT on CMOS 100 after piezoelectric film stack 220 deposition and patterning is shown according to one aspect of the present embodiments. The piezoelectric film stack 220 includes a seed layer 222 (e.g. aluminum nitride) overlying the unified oxide layer 216, a first metal layer 224 (e.g. molybdenum) overlying the seed layer 222, a piezoelectric layer 226 (e.g. aluminum nitride) overlying the first metal layer 224, and a second metal layer 228 (e.g. molybdenum) overlying the piezoelectric layer 226. In various embodiments, the piezoelectric film stack 220 includes aluminum nitride, lead zirconate titanate, zinc oxide, polyvinylidene difluoride, and/or lithium niobate.

[0026] After layer deposition, the piezoelectric film stack 220 is patterned and formed, resulting in at least a portion of the piezoelectric film stack 220 remaining over the first metal electrode 104. In various embodiments, the piezoelectric film stack 220 does not overly the second metal electrode 106 after patterning. As such, the piezoelectric film stack 220 is over the cavity 110, the membrane 218 (e.g. diaphragm), and the unified oxide layer 216 (e.g. the first fusion bond oxide 108 and the second fusion bond oxide 114 fusion bonded together).

[0027] Referring now to Figure 4, the integrated pMUT on CMOS 100 after gap fill oxide has been deposited and planarized is shown according to one aspect of the present embodiments. Additional oxide (e.g. gap fill oxide) has been added to the unified oxide layer 216 and planarized. In various embodiments, the gap fill oxide is deposited subsequent to patterning the piezoelectric film stack 220. As a result the unified oxide layer 216 surrounds the piezoelectric film stack 220, leaving a top surface 430 of the piezoelectric film stack 220 exposed and free of the unified oxide layer 216.

[0028] Referring now to Figure 5, the integrated pMUT on CMOS 100 after formation of a first electrical contact via 532 and a second electrical contact via 534 is shown according to one aspect of the present embodiments. In various embodiments, the first electrical contact via 532 is formed (e.g. etched) into the piezoelectric film stack 220. In addition, the second electrical contact via 534 is formed (e.g. etched) into the unified oxide layer 216 down to the second metal electrode 106.

[0029] Referring now to Figure 6, the integrated pMUT on CMOS 100 after deposition and patterning of an electrical contact layer 636 is shown according to one aspect of the present embodiments. The electrical contact layer 636 is deposited over the unified oxide layer 216 and the piezoelectric film stack 220. The electrical contact layer 636 fills the first

electrical contact via 532 and the second electrical contact via 534, thereby electrically connecting the piezoelectric film stack 220 to the second metal electrode 106 on the CMOS substrate 102. In various embodiments, the electrical contact layer 636 and the piezoelectric film stack 220 are patterned. Such patterning defines electrical connections from the piezoelectric film stack 220 to one or more electrodes (e.g. first metal electrode 104, second metal electrode 106, and/or other metal electrodes). As a result of the fusion bonding and layer depositions described above, the piezoelectric film stack 220 is electrically connected to the CMOS substrate 102 without a eutectic bond.

[0030] As a result of the integrated pMUT on CMOS fabrication described above, expensive eutectic bonding processes (e.g. Al-Ge eutectic bonding) can be avoided. In addition, process throughput can be improved by removing the relatively lengthy eutectic bonding process. The fusion bonding process described above addresses these concerns by reducing expense and improving process throughput.

[0031] In addition, the fusion bonding process described above uses silicon oxide. As a result, cost is reduced by removing the use of silicon on insulator or polysilicon on insulator substrates used in eutectic bonding.

[0032] Furthermore, the fusion bonding process described above does not rely on the accuracy of wafer-to-wafer bonding processes. Instead the wafers are bonded together prior to patterning, resulting in improved alignment accuracy between defined features.

[0033] Referring now to Figure 7, an integrated pMUT on CMOS 700 at an early stage of manufacture is shown according to one aspect of the present embodiments. A CMOS substrate 702 has been formed with a first metal electrode 704, a second metal electrode 706,

and a first fusion bond oxide 708. A cavity 710 is formed in the first fusion bond oxide 708. The cavity 710 is formed over the first metal electrode 704. In various embodiments, one or more cavities 710 may be formed over one or more first metal electrodes 704. At this stage of manufacture, the second metal electrode 706 remains covered by the fusion bond oxide 708. It is understood that the CMOS substrate 702 includes many CMOS structures including, but not limited to, integrated circuit(s), transistor(s), substrate(s), electrical connection(s), metal electrode(s), the fusion bond oxide, etc.

[0034] A stop oxide layer 738 is formed on a carrier substrate 712 (e.g. handle substrate). A piezoelectric film stack 720 is formed on the stop oxide layer 738 and includes a seed layer 722 (e.g. aluminum nitride) on the stop oxide layer 738, a first metal layer 724 (e.g. molybdenum) on the seed layer 722, a piezoelectric layer 726 (e.g. aluminum nitride) on the first metal layer 724, and a second metal layer 728 (e.g. molybdenum) on the piezoelectric layer 226. In various embodiments, the piezoelectric film stack 720 includes aluminum nitride, lead zirconate titanate, zinc oxide, polyvinylidene difluoride, and/or lithium niobate.

[0035] A second fusion bond oxide 714 is formed on the second metal layer 728 of the piezoelectric film stack 720. The second fusion bond oxide 714 may be the same material as the first fusion bond oxide 708 or a different material. In various embodiments, no features have been formed in either the carrier substrate 712 or the second fusion bond oxide 714.

[0036] Referring now to Figure 8, the integrated pMUT on CMOS 700 after fusion bonding and removal of the carrier substrate 712 is shown according to one aspect of the present embodiments. The first fusion bond oxide 708 and the second fusion bond oxide 714 have been fusion bonded together to form a unified oxide layer 816. The unified oxide layer 816 encloses the cavity 710 and forms a membrane 818 (e.g. diaphragm) over the cavity 710

and a portion of the first metal electrode 704. After the fusion bonding and formation of the unified oxide layer 816, the carrier substrate 712 and the stop oxide layer 738 are removed (e.g. by grinding, etching, etc.).

[0037] The removal leaves the piezoelectric film stack 720 including the first metal layer 724, the piezoelectric layer 726, and the second metal layer 728. The first metal layer 724 is over the piezoelectric layer 726. The piezoelectric layer 726 is over the second metal layer 728. The second metal layer 728 is over the unified oxide layer 816 (e.g. the first fusion bond oxide 708 and the second fusion bond oxide 714 fusion bonded together).

[0038] Referring now to Figure 9, the integrated pMUT on CMOS 700 after piezoelectric film stack 720 patterning and deposition of gap fill oxide is shown according to one aspect of the present embodiments. The piezoelectric film stack 720 is patterned and formed (e.g. by etching), resulting in at least a portion of the piezoelectric film stack 720 remaining over the first metal electrode 704, the cavity 710, the membrane 818 (e.g. diaphragm), and the unified oxide layer 816 (e.g. the first fusion bond oxide 708 and the second fusion bond oxide 714 fusion bonded together). In various embodiments, the piezoelectric film stack 720 does not overly the second metal electrode 706 after patterning.

[0039] After the patterning of the piezoelectric film stack 720, additional oxide (e.g. gap fill oxide) has been deposited and added to the unified oxide layer 816 and planarized. In various embodiments, the gap fill oxide is deposited subsequent to depositing and patterning the piezoelectric film stack 720. As a result the unified oxide layer 816 surrounds the piezoelectric film stack 720, leaving a top surface 930 of the piezoelectric film stack 720 exposed and free of the unified oxide layer 816.

[0040] Referring now to Figure 10, the integrated pMUT on CMOS 700 after formation of a first electrical contact via 1032 and a second electrical contact via 1034 is shown according to one aspect of the present embodiments. In various embodiments, the first electrical contact via 1032 is formed (e.g. etched) into the piezoelectric film stack 720. In addition, the second electrical contact via 1034 is formed (e.g. etched) into the unified oxide layer 816 down to the second metal electrode 706.

[0041] Referring now to Figure 11, the integrated pMUT on CMOS 700 after deposition and patterning of an electrical contact layer 1136 is shown according to one aspect of the present embodiments. The electrical contact layer 1136 is deposited over the unified oxide layer 816 and the piezoelectric film stack 720. The electrical contact layer 1136 fills the first electrical contact via 1032 and the second electrical contact via 1034, thereby electrically connecting the piezoelectric film stack 720 to the second metal electrode 706 on the CMOS substrate 702. In various embodiments, the electrical contact layer 1136 and the piezoelectric film stack 720 are patterned. Such patterning defines electrical connections from the piezoelectric film stack 720 to one or more electrodes (e.g. first metal electrode 704, second metal electrode 706, and/or other metal electrodes). As a result of the fusion bonding and layer depositions described above, the piezoelectric film stack 720 is electrically connected to the CMOS substrate 702 without a eutectic bond.

[0042] As a result of the integrated pMUT on CMOS fabrication described above, expensive eutectic bonding processes (e.g. Al-Ge eutectic bonding) can be avoided. In addition, process throughput can be improved by removing the relatively lengthy eutectic bonding process. The fusion bonding process described above addresses these concerns by reducing expense and improving process throughput.

[0043] In addition, the fusion bonding process described above uses silicon oxide. As a result, cost is reduced by removing the use of silicon on insulator or polysilicon on insulator substrates used in eutectic bonding.

[0044] Furthermore, the fusion bonding process described above does not rely on the accuracy of wafer-to-wafer bonding processes. Instead the wafers are bonded together prior to patterning, resulting in improved alignment accuracy between defined features.

[0045] Figure 12 shows an exemplary flow diagram 1200 for the integration of pMUT on CMOS according to one aspect of the present embodiments. At block 1202, a first oxide layer on a handle substrate is fusion bonded to a second oxide layer on a CMOS, wherein the fusion bonding forms a unified oxide layer including a diaphragm overlying a cavity on the CMOS. For example, in Figures 1 and 2 the second fusion bond oxide on the carrier substrate is fusion bonded to the first fusion bond oxide. The fusion bonding forms the unified oxide layer that encloses the cavity, thereby forming a membrane (e.g. diaphragm) over the cavity on the CMOS.

[0046] In some embodiments, the handle substrate and the first oxide layer do not include any metal. For example, in Figure 1 the carrier substrate (e.g. handle substrate) and the second fusion bond oxide do not contain any metal. In various embodiments, the fusion bonding occurs prior to any patterning of the second oxide layer. For example, in Figure 1 no features have been formed (e.g. no patterning) in either the carrier substrate or the second fusion bond oxide.

[0047] At block 1204, the handle substrate is removed leaving the unified oxide layer. For example, in Figure 2 the carrier substrate is removed (e.g. by grinding, etching, etc.) leaving the unified oxide layer over the CMOS substrate.

[0048] At a block 1206, a piezoelectric film stack is deposited over the unified oxide layer. For example, in Figure 3 the piezoelectric film stack is deposited over the unified oxide layer. In some embodiments, the piezoelectric film stack includes the seed layer deposited over the unified oxide layer, the first metal layer deposited over the seed layer, the piezoelectric layer deposited over the first metal layer, and the second metal layer deposited over the piezoelectric layer. In various embodiments, the seed layer and the piezoelectric layer include aluminum nitride. In further embodiments, the first metal layer and the second metal layer include molybdenum.

[0049] In some embodiments, a gap fill oxide is deposited subsequent to depositing the piezoelectric film stack over the unified oxide layer. For example, in Figure 4 additional oxide (e.g. gap fill oxide) has been added to the unified oxide layer and planarized subsequent to depositing and patterning the piezoelectric film stack.

[0050] At a block 1208, vias are formed in the piezoelectric film stack and the unified oxide layer. For example, in Figure 5 the first electrical contact via is formed (e.g. etched) into the piezoelectric film stack. In addition, the second electrical contact via is formed (e.g. etched) into the unified oxide layer down to the second metal electrode.

[0051] At a block 1210, an electrical contact layer is deposited, wherein the electrical contact layer electrically connects the piezoelectric film stack to an electrode on the CMOS. For example, in Figure 6 the electrical contact layer fills the first electrical contact via and the

second electrical contact via, thereby electrically connecting the piezoelectric film stack to the second metal electrode on the CMOS.

[0052] Figure 13 shows an exemplary flow diagram 1300 for the integration of pMUT on CMOS according to one aspect of the present embodiments. At block 1302, a stop oxide layer is formed over a handle substrate. For example, in Figure 7 a stop oxide layer is formed on a carrier substrate (e.g. handle substrate).

[0053] At block 1304, a piezoelectric film stack is formed over the stop oxide layer. For example, in Figure 7 a piezoelectric film stack is formed over the stop oxide layer and includes a seed layer deposited over the stop oxide layer, a first metal layer deposited over the seed layer, a piezoelectric layer deposited over the first metal layer, and a second metal layer deposited over the piezoelectric layer. In various embodiments, the piezoelectric film stack includes aluminum nitride, lead zirconate titanate, zinc oxide, polyvinylidene difluoride, and/or lithium niobate.

[0054] At a block 1306, a first oxide layer on a CMOS is fusion bonded to a second oxide layer on the piezoelectric film stack, wherein the fusion bonding forms a unified oxide layer including a diaphragm overlying a cavity on the CMOS. For example, in Figure 8 the first fusion bond oxide on the CMOS and the second fusion bond oxide on the piezoelectric film stack have been fusion bonded together to form a unified oxide layer. The unified oxide layer encloses the cavity and forms a membrane (e.g. diaphragm) over the cavity.

[0055] At a block 1308, the handle substrate and the stop oxide layer are removed from the piezoelectric film stack. For example, in Figure 8 the carrier substrate and the stop oxide layer are removed (e.g. by grinding, etching, etc.).

[0056] At a block 1310, the piezoelectric film stack is patterned. For example, in Figure 9 the piezoelectric film stack is patterned and formed (e.g. by etching). In some embodiments, a gap fill oxide is deposited and planarized subsequent to patterning the piezoelectric film stack. For example, in Figure 9 after the patterning of the piezoelectric film stack, additional oxide (e.g. gap fill oxide) has been deposited and added to the unified oxide layer and planarized. In various embodiments, the gap fill oxide is deposited subsequent to depositing and patterning the piezoelectric film stack.

[0057] In some embodiments, the fusion bonding occurs prior to the patterning of the piezoelectric film stack. For example, in Figures 8 and 9 the first fusion bond oxide and the second fusion bond oxide have been fusion bonded together to form a unified oxide layer. Thereafter, the piezoelectric film stack is patterned and formed (e.g. by etching), resulting in at least a portion of the piezoelectric film stack remaining over the unified oxide layer (e.g. the first fusion bond oxide and the second fusion bond oxide fusion bonded together).

[0058] At a block 1312, vias are formed in the piezoelectric film stack and the unified oxide layer. For example, in Figure 10 the first electrical contact via is formed (e.g. etched) into the piezoelectric film stack. In addition, the second electrical contact via is formed (e.g. etched) into the unified oxide layer down to the second metal electrode.

[0059] At a block 1314, an electrical contact layer is deposited, wherein the electrical contact layer electrically connects the piezoelectric film stack to an electrode on the CMOS. For example, in Figure 11 the electrical contact layer fills the first electrical contact via and the second electrical contact via, thereby electrically connecting the piezoelectric film stack to the second metal electrode on the CMOS substrate.

[0060] In some embodiments, the piezoelectric film stack is electrically connected to the CMOS without eutectic bonding. For example, in Figure 11 the electrical contact layer electrically connects the piezoelectric film stack to the second metal electrode on the CMOS substrate. As a result of the fusion bonding and layer depositions described above, the piezoelectric film stack is electrically connected to the CMOS substrate without a eutectic bond.

[0061] While the embodiments have been described and/or illustrated by means of particular examples, and while these embodiments and/or examples have been described in considerable detail, it is not the intention of the Applicants to restrict or in any way limit the scope of the embodiments to such detail. Additional adaptations and/or modifications of the embodiments may readily appear, and, in its broader aspects, the embodiments may encompass these adaptations and/or modifications. Accordingly, departures may be made from the foregoing embodiments and/or examples without departing from the scope of the concepts described herein. The implementations described above and other implementations are within the scope of the following claims.

CLAIMS

What is claimed is:

1. A method comprising:

fusion bonding a first oxide layer on a complementary metal oxide semiconductor (CMOS) to a second oxide layer on a handle substrate, wherein the fusion bonding forms a unified oxide layer including a diaphragm overlying a cavity on the CMOS;

removing the handle substrate leaving the unified oxide layer;

depositing a piezoelectric film stack over the unified oxide layer;

forming vias in the piezoelectric film stack and the unified oxide layer; and

depositing an electrical contact layer, wherein the electrical contact layer electrically connects the piezoelectric film stack to an electrode on the CMOS.

2. The method of Claim 1, wherein depositing the piezoelectric film stack includes:

depositing a seed layer over the unified oxide layer;

depositing a first metal layer over the seed layer;

depositing a piezoelectric layer over the first metal layer; and

depositing a second metal layer over the piezoelectric layer.

3. The method of Claim 2, wherein

the seed layer and the piezoelectric layer include aluminum nitride, and

the first metal layer and the second metal layer include molybdenum.

4. The method of Claim 1, further comprising depositing a gap fill oxide subsequent to the depositing the piezoelectric film stack over the unified oxide layer.

5. The method of Claim 4, further comprising planarizing the gap fill oxide.

6. The method of Claim 1, wherein the handle substrate and the second oxide layer do not include any metal.

7. The method of Claim 1, wherein the fusion bonding occurs prior to any patterning of the second oxide layer.

8. A method comprising:

forming a stop oxide layer over a handle substrate;

forming a piezoelectric film stack over the stop oxide layer;

fusion bonding a first oxide layer on a complementary metal oxide semiconductor (CMOS) to a second oxide layer on the piezoelectric film stack, wherein the fusion bonding forms a unified oxide layer including a diaphragm overlying a cavity on the CMOS;

removing the handle substrate and the stop oxide layer from the piezoelectric film stack;

patterning the piezoelectric film stack;

forming vias in the piezoelectric film stack and the unified oxide layer; and

depositing an electrical contact layer, wherein the electrical contact layer electrically connects the piezoelectric film stack to an electrode on the CMOS.

9. The method of Claim 8, wherein depositing the piezoelectric film stack includes:

depositing a seed layer over the stop oxide layer;

depositing a first metal layer over the seed layer;

depositing a piezoelectric layer over the first metal layer; and

depositing a second metal layer over the piezoelectric layer.

10. The method of Claim 8, wherein the piezoelectric film stack includes aluminum nitride, lead zirconate titanate, zinc oxide, polyvinylidene difluoride, or lithium niobate.

11. The method of Claim 8, further comprising depositing a gap fill oxide subsequent to the patterning the piezoelectric film stack.

12. The method of Claim 11, further comprising planarizing the gap fill oxide.

13. The method of Claim 8, wherein the fusion bonding occurs prior to the patterning of the piezoelectric film stack.

14. The method of Claim 8, wherein the piezoelectric film stack is electrically connected to the CMOS without eutectic bonding.

15. An apparatus comprising:

a complementary metal oxide semiconductor (CMOS) substrate;

an electrode on the CMOS substrate;

a first oxide layer over the CMOS substrate;

a second oxide layer fusion bonded to the first oxide layer, wherein the first oxide layer and the second oxide layer define a cavity and a diaphragm;

a piezoelectric film stack over the second oxide layer, the cavity, and the diaphragm; and

an electrical contact layer electrically connecting the electrode to the piezoelectric film stack.

16. The apparatus of Claim 15, wherein the piezoelectric film stack includes:

a first metal layer over the second oxide layer;

a piezoelectric layer over the first metal layer; and

a second metal layer over the piezoelectric layer.

17. The apparatus of Claim 16, further comprising a seed layer between the first metal layer and the second oxide layer.

18. The apparatus of Claim 16, wherein

the piezoelectric layer includes aluminum nitride, and

the first metal layer and the second metal layer include molybdenum.

19. The apparatus of Claim 15, wherein the piezoelectric film stack includes aluminum nitride, lead zirconate titanate, zinc oxide, polyvinylidene difluoride, or lithium niobate.

20. The apparatus of Claim 15, wherein the piezoelectric film stack is electrically connected to the CMOS without a eutectic bond.

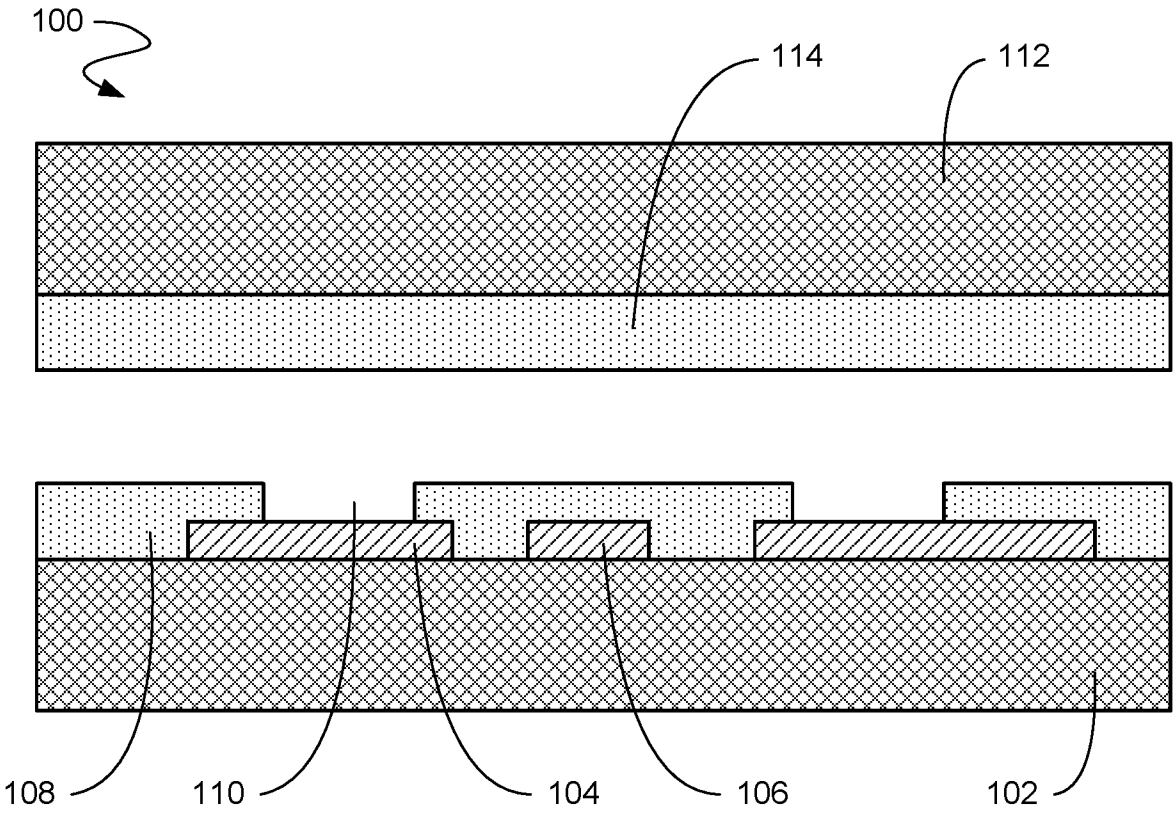


FIG. 1

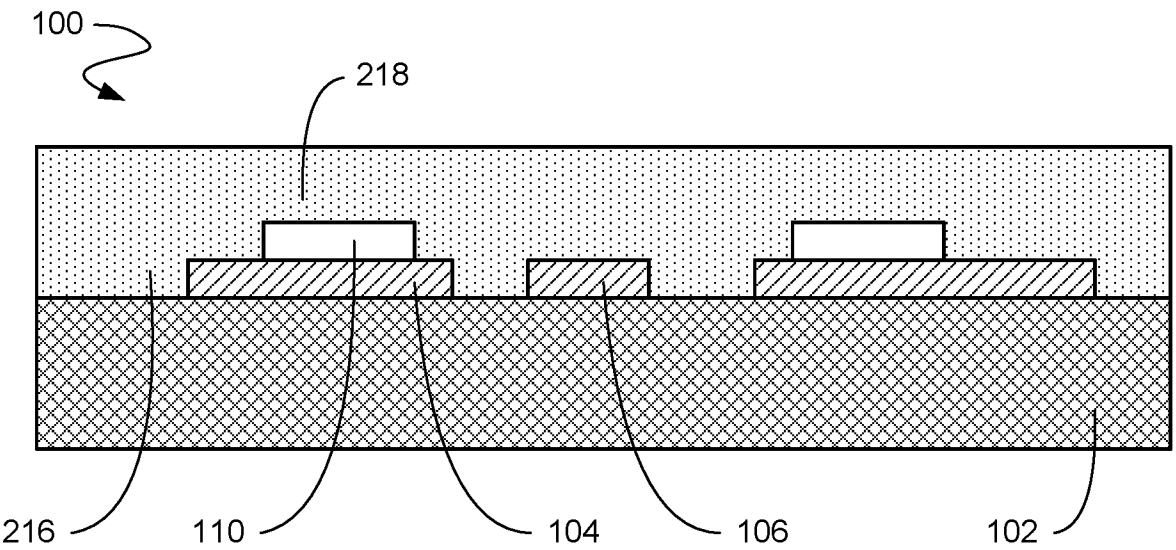


FIG. 2

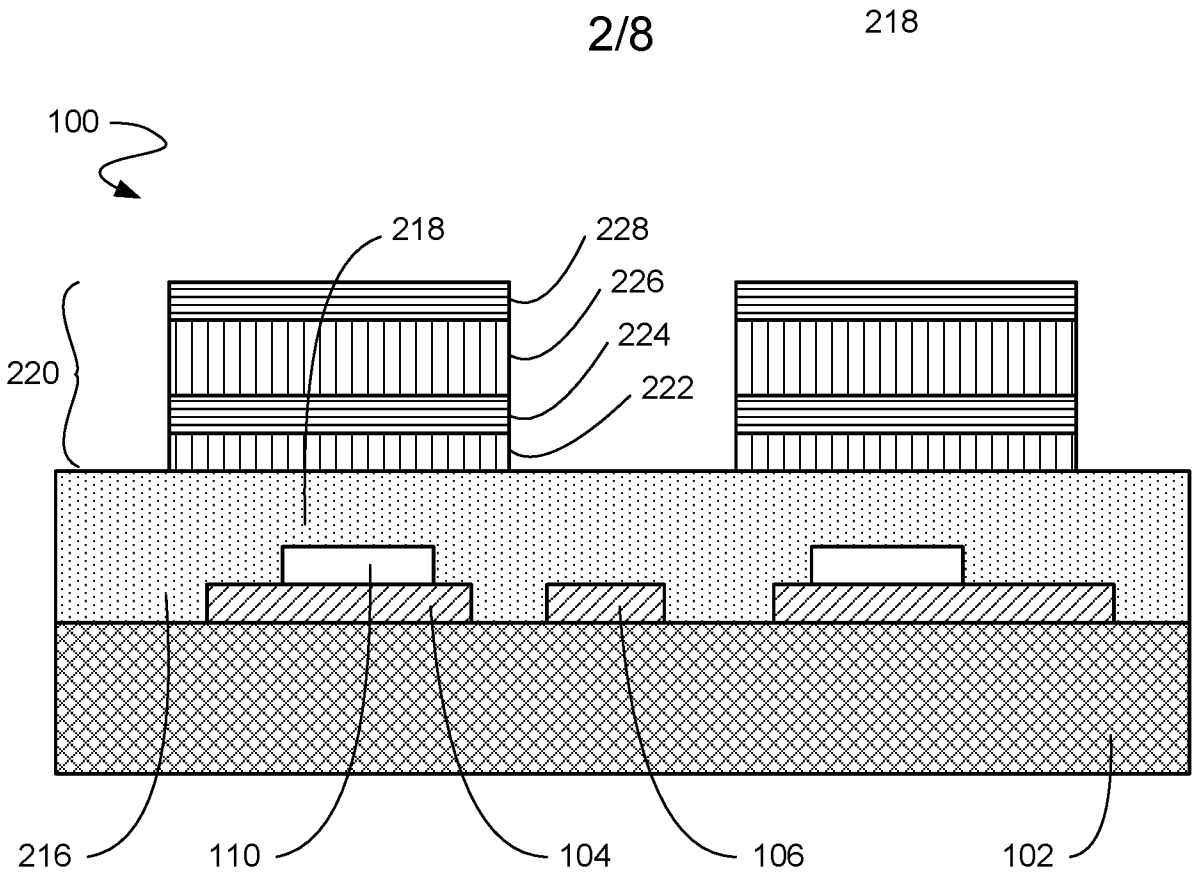

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100
218
228
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222
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106
102

FIG. 3

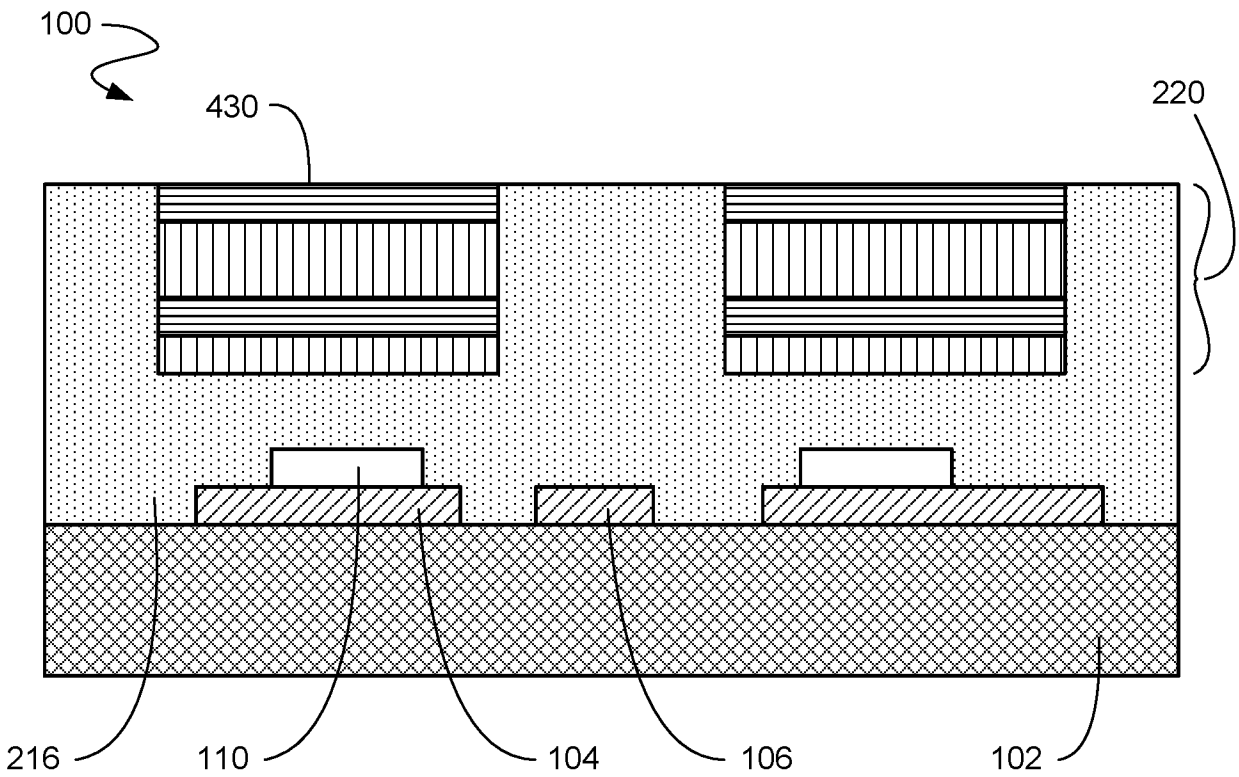

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216
110
104
106
102

FIG. 4

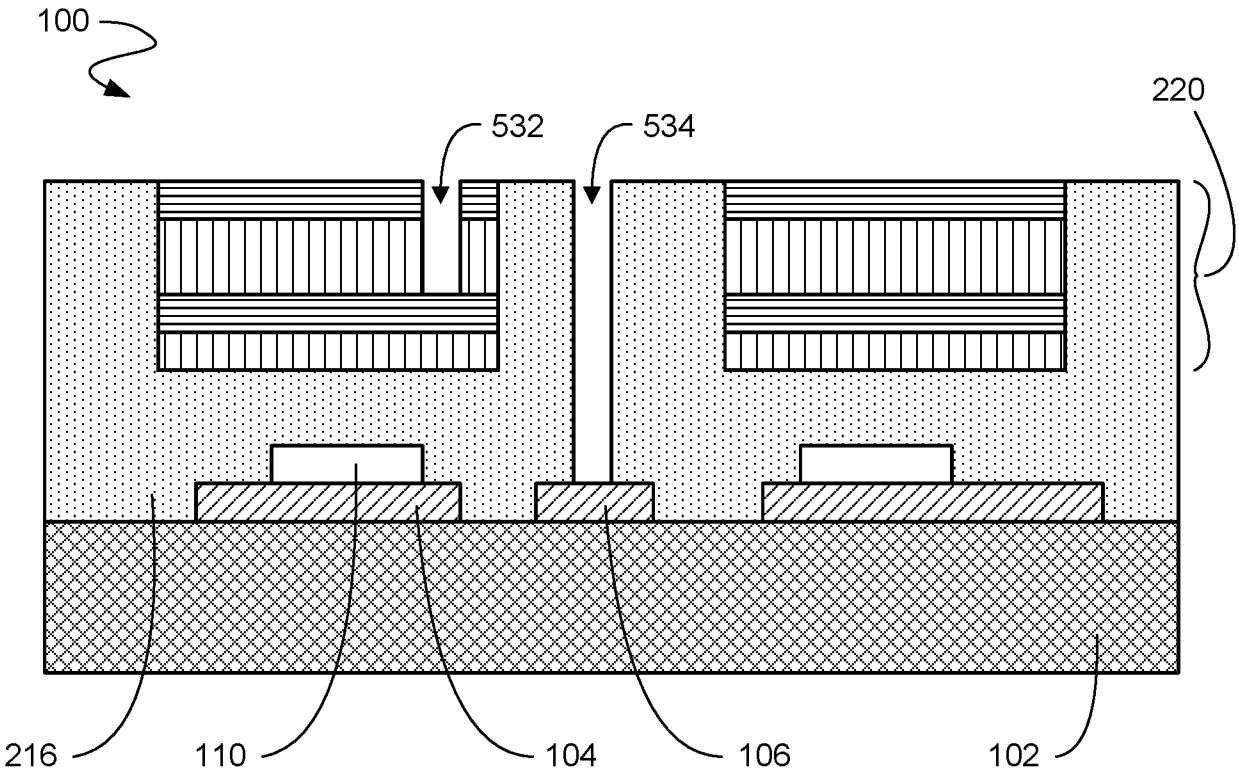

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532
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216
110
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106
102

FIG. 5

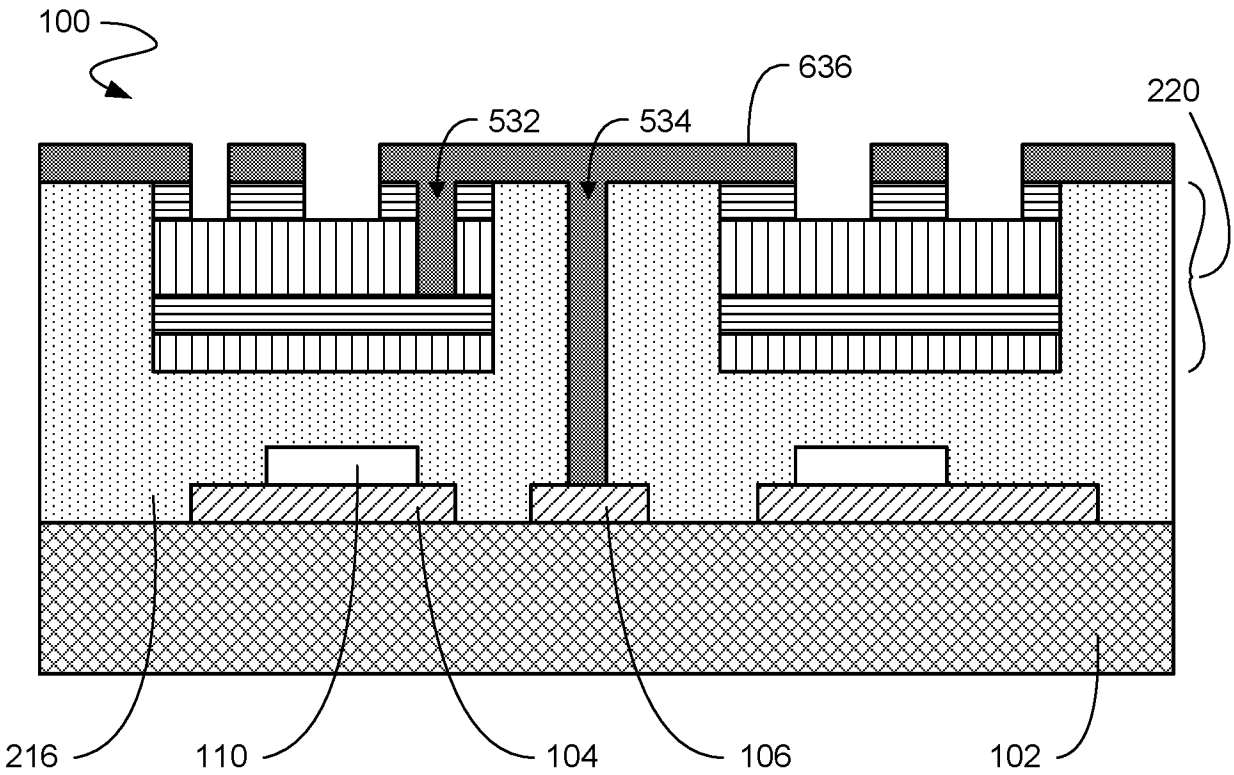

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636
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216
110
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106
102

FIG. 6

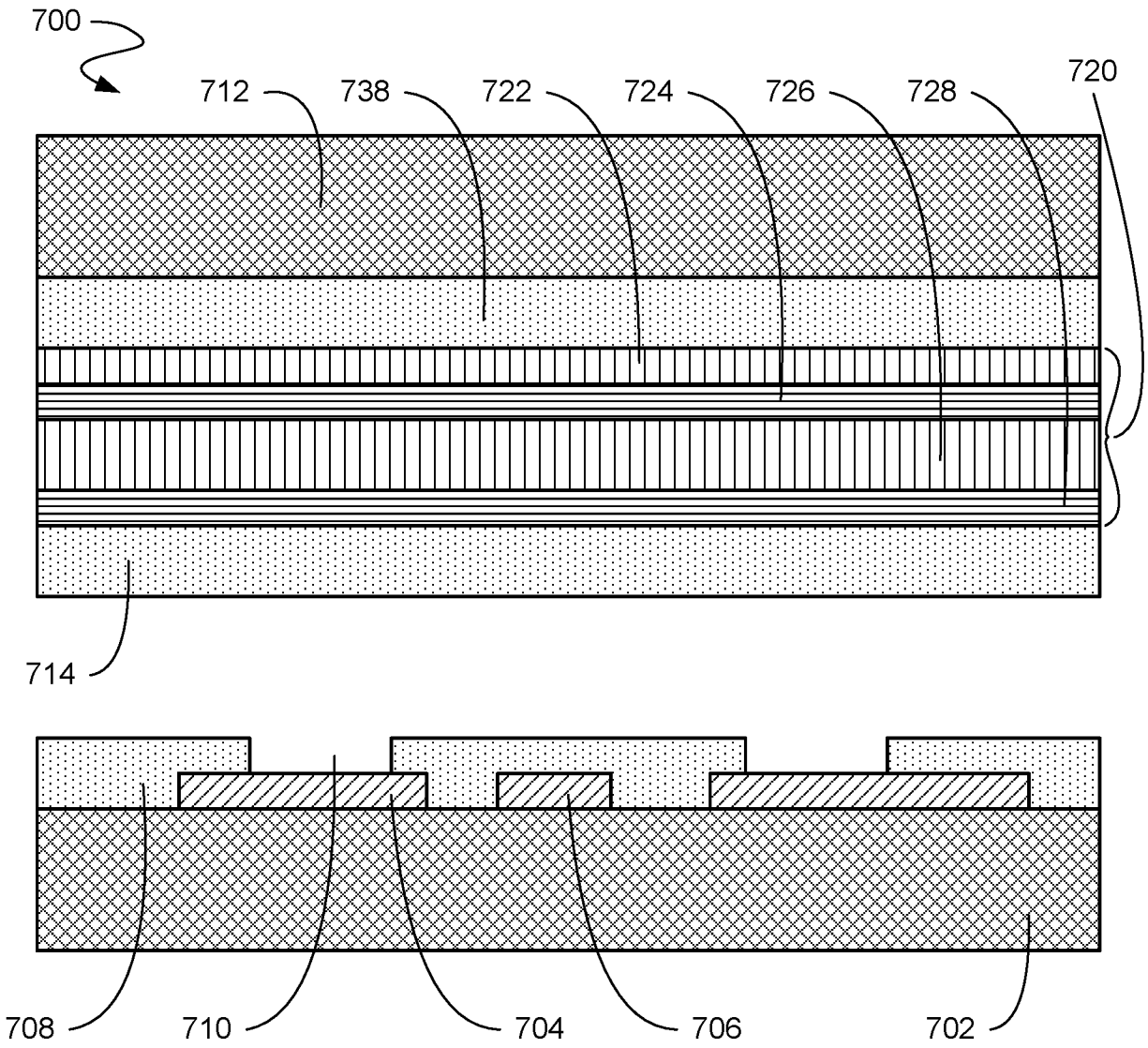


FIG. 7

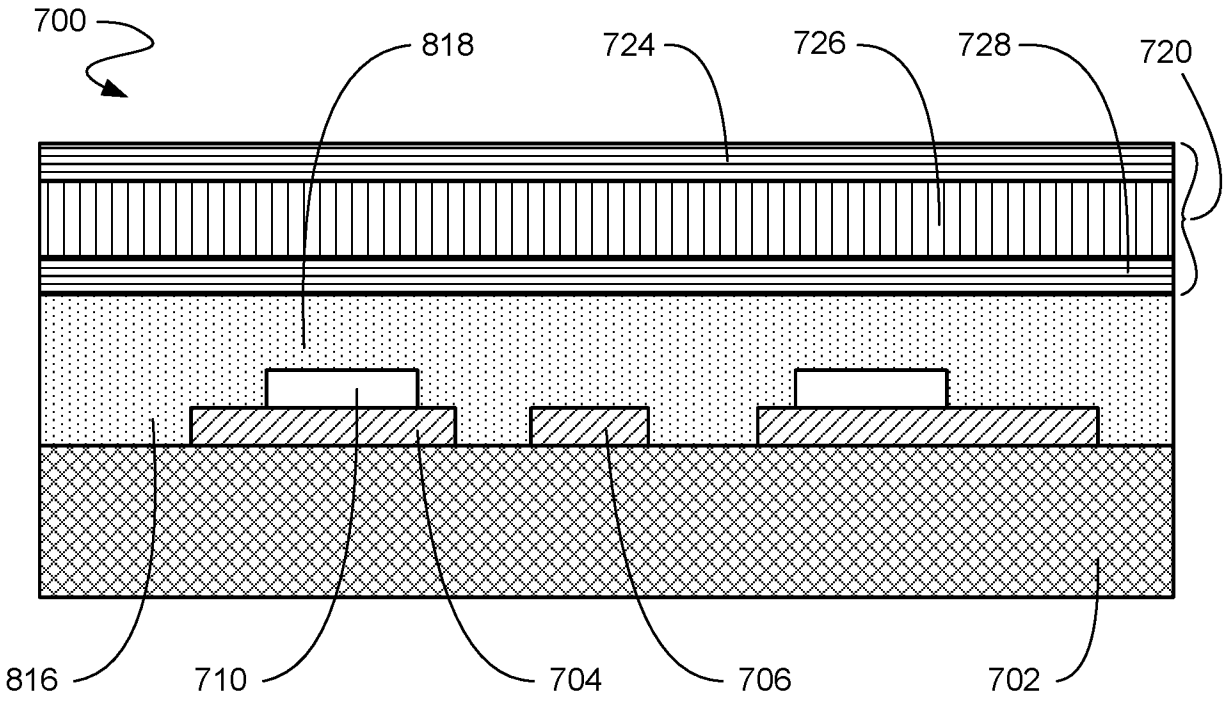

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702

FIG. 8

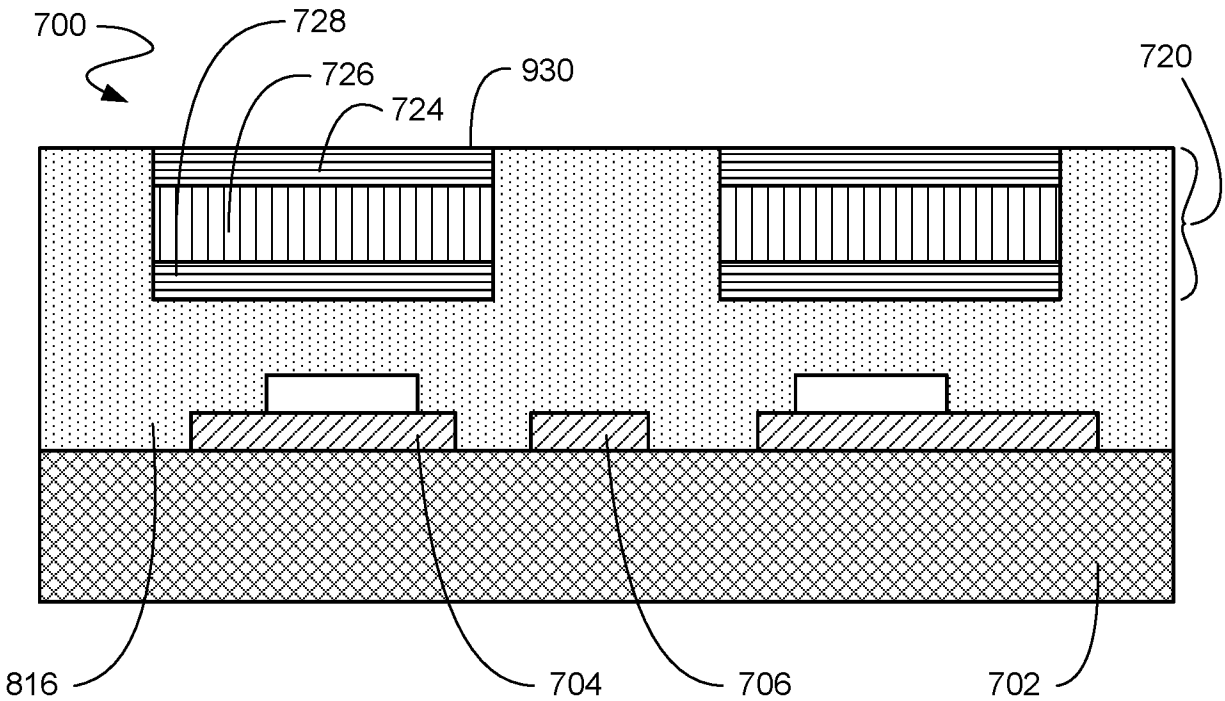

700
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726
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706
702

FIG. 9

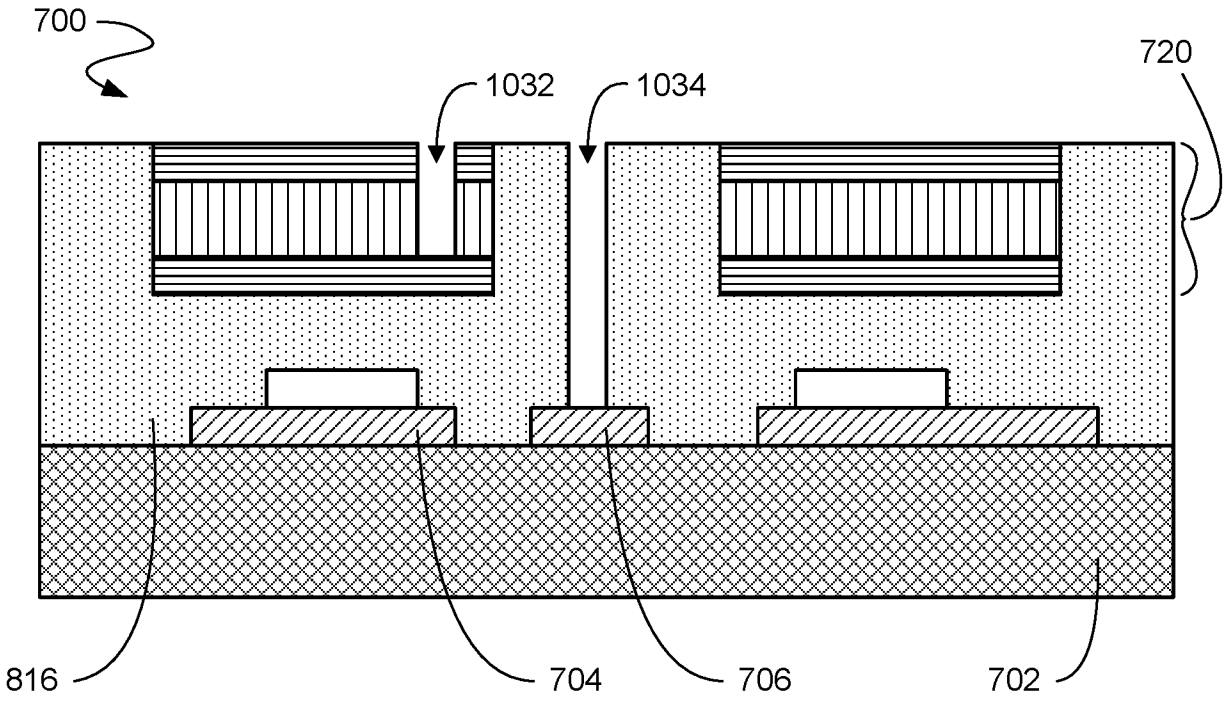

700
1032
1034
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816
704
706
702

FIG. 10

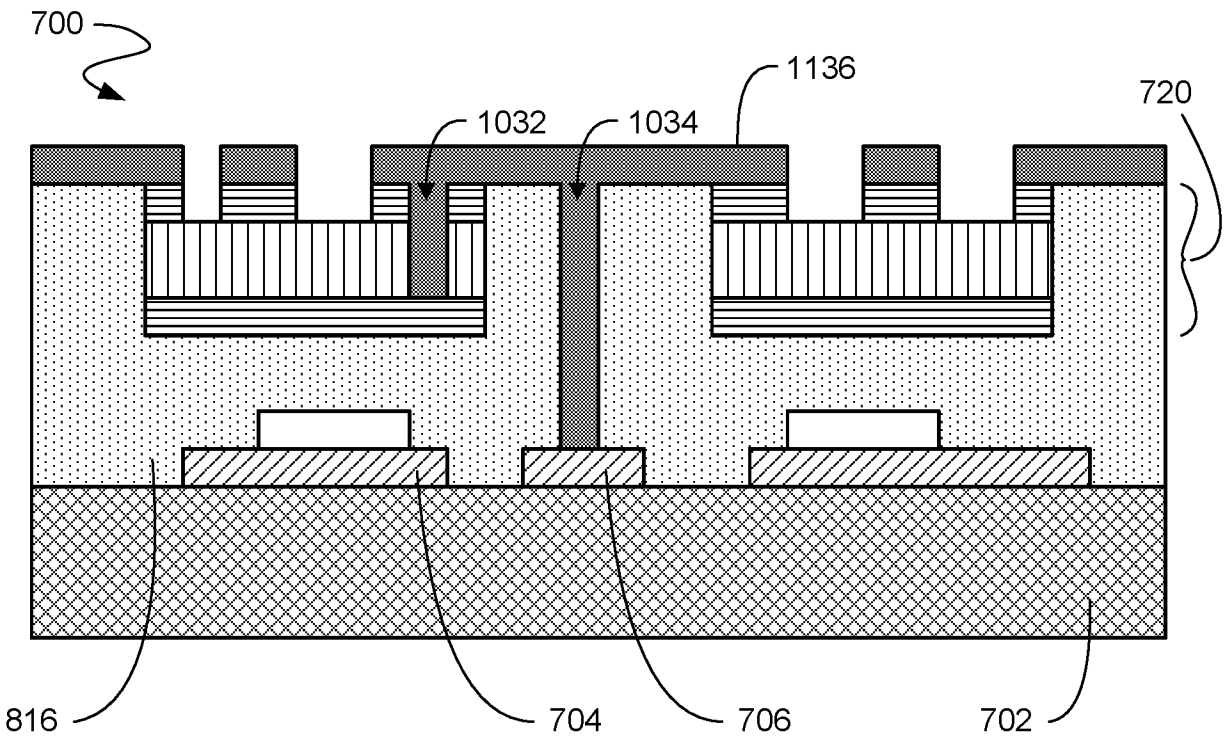
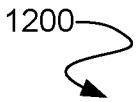

700
1136
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816
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706
702

FIG. 11



FUSION BONDING A FIRST OXIDE LAYER ON A CMOS TO A SECOND OXIDE LAYER ON A HANDLE SUBSTRATE, WHEREIN THE FUSION BONDING FORMS A UNIFIED OXIDE LAYER INCLUDING A DIAPHRAGM OVERLYING A CAVITY ON THE CMOS
1202

REMOVING THE HANDLE SUBSTRATE LEAVING THE UNIFIED OXIDE LAYER
1204

DEPOSITING A PIEZOELECTRIC FILM STACK OVER THE UNIFIED OXIDE LAYER
1206

FORMING VIAS IN THE PIEZOELECTRIC FILM STACK AND THE UNIFIED OXIDE LAYER
1208

DEPOSITING AN ELECTRICAL CONTACT LAYER, WHEREIN THE ELECTRICAL CONTACT LAYER ELECTRICALLY CONNECTS THE PIEZOELECTRIC FILM STACK TO AN ELECTRODE ON THE CMOS
1210

FIG. 12

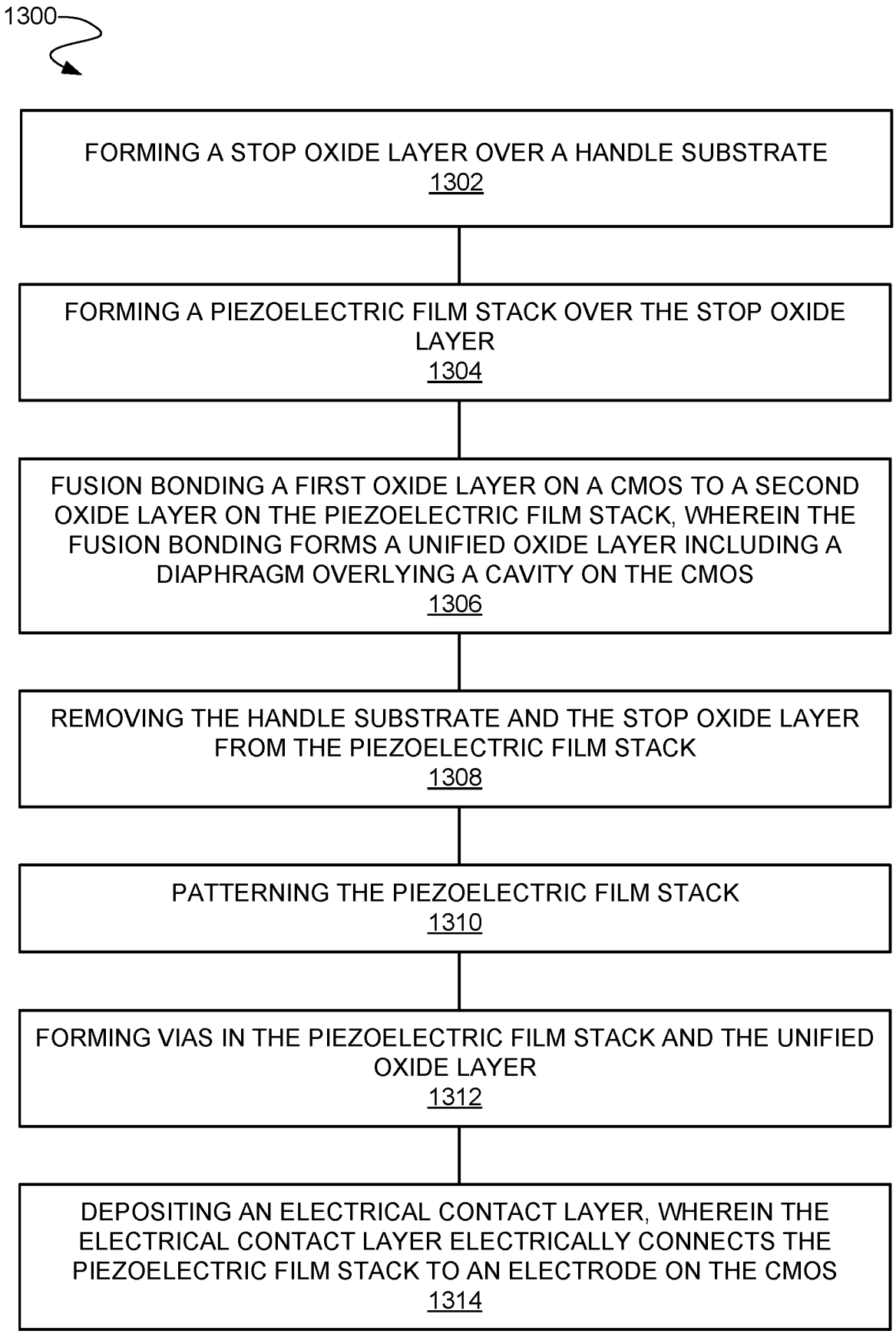

1300
FORMING A STOP OXIDE LAYER OVER A HANDLE SUBSTRATE
1302
FORMING A PIEZOELECTRIC FILM STACK OVER THE STOP OXIDE LAYER
1304
FUSION BONDING A FIRST OXIDE LAYER ON A CMOS TO A SECOND OXIDE LAYER ON THE PIEZOELECTRIC FILM STACK, WHEREIN THE FUSION BONDING FORMS A UNIFIED OXIDE LAYER INCLUDING A DIAPHRAGM OVERLYING A CAVITY ON THE CMOS
1306
REMOVING THE HANDLE SUBSTRATE AND THE STOP OXIDE LAYER FROM THE PIEZOELECTRIC FILM STACK
1308
PATTERNING THE PIEZOELECTRIC FILM STACK
1310
FORMING VIAS IN THE PIEZOELECTRIC FILM STACK AND THE UNIFIED OXIDE LAYER
1312
DEPOSITING AN ELECTRICAL CONTACT LAYER, WHEREIN THE ELECTRICAL CONTACT LAYER ELECTRICALLY CONNECTS THE PIEZOELECTRIC FILM STACK TO AN ELECTRODE ON THE CMOS
1314

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/022201

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L41/113 H01L41/31 B81C1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L B81C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/357375 A1 (TSAI JULIUS MING-LIN [US] ET AL) 10 December 2015 (2015-12-10) paragraph [0083] - paragraph [0089]; figures 9C-9K -----	15-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 June 2017	23/06/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Angermeier, Detlef

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2017/022201

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015357375 A1	10-12-2015	NONE	