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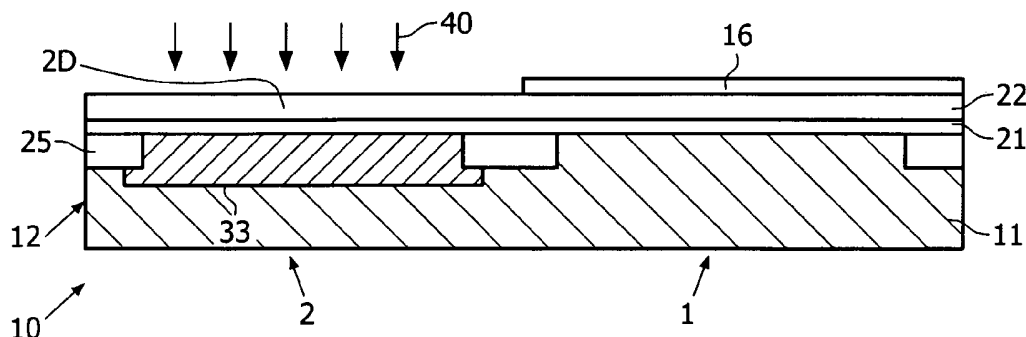
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(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SUCH A SEMICONDUCTOR DEVICE



(57) Abstract: The invention relates to a CMOS device (10) with an NMOST 1 and PMOST 2 having gate regions (1D, 2D) comprising a compound containing both a metal and a further element. According to the invention the first and second conducting material both comprise a compound containing as the metal a metal selected from the group comprising molybdenum and tungsten and both comprise as the further element an element selected from the group comprising carbon, oxygen and the chalcogenides. Preferably both the first and second conducting material comprise a compound of molybdenum and carbon or oxygen. The invention also provides an attractive method of manufacturing such a device.

Semiconductor device and method of manufacturing such a semiconductor device

The invention relates to a semiconductor device with a substrate and a semiconductor body comprising a first field effect transistor with a first source and drain region and a first channel of a first conductivity type and with separated from the first channel by a first dielectric region a first gate region comprising a first conducting material and a second field effect transistor with a second source and drain region and a second channel of a second, opposite to the first, conductivity type and with separated from the second channel by a second dielectric region a second gate region comprising a second conducting material different from the first conducting material, wherein the first and second conducting material comprise a compound containing both a metal and a further element. In advanced CMOS (= Complimentary Metal Oxide Semiconductor) devices below the sub 0,1 micron region, the replacement of polysilicon gates by metal gates or alloys thereof is desirable for various reasons. The invention also relates to a method of manufacturing such a device.

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A device as mentioned in the opening paragraph is known from US patent 6,130,123 that has been published on October 10, 2000. Therein various electrically conducting materials are described that are suitable for use in the NMOST (= N-type MOS Transistor) and PMOST of a CMOS device. Examples of metals or metal alloys that are suitable for the former of which the workfunction is about 4.2 eV are Ru, Zr, Nb, Ta, MoSi and TaSi. For the latter, having a workfunction of about 5.2 eV Ni, RuO₂, MoN and TaN are suitable material among others.

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A drawback of the known conducting materials is that they are not always very compatible with existing IC technology. This includes the requirement that the materials should be compatible with the materials of the gate stack comprising the materials of the gate dielectric, the capping layer and the spacers.

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It is therefore an object of the present invention to avoid the above drawbacks and to provide a device which is very compatible with IC technology and easy to manufacture.

To achieve this, a device of the type mentioned in the opening paragraph is characterized in that the first and second conducting material both comprise a compound containing as the metal a metal selected from the group comprising molybdenum and tungsten and both comprise as the further element an element selected from the group comprising carbon, oxygen and the chalcogenides, the latter comprising S, Se and Te. On the one hand the material contains a metal that is very common in present IC technology, e.g. for conduction tracks and in particular for use as a connection between conduction tracks at different levels. On the other hand the further elements in a device according to the invention provide several advantages. Firstly, they allow for a full coverage of the workfunction range desired, i.e. from about 4.1 eV to about 5.2 eV. Furthermore, this may be realized by having the metal in common for both the first and the second transistor which simplifies the manufacture. To the latter also contributes the fact that the conducting material may be formed using gaseous compounds of the further elements mentioned, e.g. CH₄, O₂ and H₂Se.

In a preferred embodiment both the first and second conducting material comprise a compound of molybdenum and carbon or oxygen. These compounds are very suitable to obtain the objectives of the invention. In a first modification the first conductivity type comprises the n-type and the first conducting material comprises a compound of molybdenum and carbon and the second conducting material comprises a compound of molybdenum and oxygen. In another variant, in which the first conductivity type comprises the n-type, the first conducting material comprises a compound of molybdenum and oxygen with a higher oxygen content and in that the second conducting material comprises a compound of molybdenum and oxygen with a lower oxygen content. Since in this case both the N-metal and the P-metal can be formed with only two elements, the manufacture is relatively simple in particular when using a method of manufacturing according to the invention as described below.

A method of manufacturing a semiconductor device with a substrate and a semiconductor body comprising a first field effect transistor with a first source and drain region and a first channel of a first conductivity type and with separated from the first channel by a first dielectric region a first gate region comprising a first conducting material and a second field effect transistor with a second source and drain region and a second

channel of a second, opposite to the first, conductivity type and with separated from the second channel by a second dielectric region a second gate region comprising a second conducting material different from the first conducting material, wherein for the first and second conducting materials a material is chosen comprising a compound containing both a metal and a further element, is according to the invention characterized in that for the first and second conducting material both a material is chosen comprising a compound containing as the metal a metal selected from the group comprising molybdenum and tungsten and comprising as the further element an element selected from the group comprising carbon, oxygen and the chalcogenides. In this way a semiconductor device according to the invention is obtained.

In a preferred embodiment of the method according to the invention for both the first and second conducting material a material is chosen comprising a compound of molybdenum and carbon or oxygen.

A first modification is characterized in that on the first and second dielectric regions a layer of the metal is formed which is at the location of the first dielectric region made to react with a gaseous compound of the further element while the layer of the metal at the location of the second dielectric region is protected against the gaseous compound by a mask and which after removal of the mask is at the location of the second dielectric region made to react with a gaseous compound of the further element while the layer of the metal at the location of the first dielectric region is protected against the gaseous compound by a further mask. In this way, only a single metal layer needs to be deposited to form the conducting material. Furthermore, a gaseous compound containing e.g. oxygen can be used to locally transfer the metal in the compound with the desired workfunction while the other gate region is protected by a mask which is impermeable for such a gaseous compound. A suitable material for the latter is TiN or MoN. While it is preferred to do the reaction with the gaseous compound at the layer stage, it also may be done if the gate regions already have been formed from a layer (structure) by etching.

Another modification is characterized in that on the first and second dielectric regions a layer of the first conducting material is deposited which is at the location of the second dielectric region made to react with a gaseous compound of the further element while the layer of the first conducting material at the location of the first dielectric region is protected against the gaseous compound by a mask. In this way only one masking step is needed which simplifies the manufacturing. The layer of the first conducting material may be formed by a physical deposition technique like sputtering in a gaseous atmosphere, e.g.

sputtering of Mo in an O₂ containing atmosphere, or by another technique like CVD (= Chemical Vapor Deposition).

Preferably the layer of the first conducting material is formed by depositing a layer of the metal and reacting the metal layer with a gaseous compound of the further
5 element. In particular if the metal layer has a porous structure or forms a very thin film (e.g. with a thickness < 10nm), it may easily react with gasses like CH₄ or O₂ or the like.

These and other aspects of the invention will be apparent from and elucidated
10 with reference to the embodiments described hereinafter, to be read in conjunction with the drawing, in which

Figs. 1 through 4 are sectional views of a first example of a semiconductor device according to the invention at various stages in the manufacture of the device by means of a first embodiment of a method in accordance with the invention,

15 Figs. 5 through 7 are sectional views of a second example of a semiconductor device according to the invention at various stages in the manufacture of the device by means of a second embodiment of a method in accordance with the invention, and

Fig. 8 is a sectional views of a third example of a semiconductor device according to the invention at a relevant stage in the manufacture of the device by means of a
20 third embodiment of a method in accordance with the invention.

The Figures are diagrammatic and not drawn to scale, the dimensions in the thickness direction being particularly exaggerated for greater clarity. Corresponding parts are
25 generally given the same reference numerals and the same hatching in the various Figures.

Figs. 1 through 4 show sectional views of a first example of a semiconductor device according to the invention at various stages in the manufacture of the device by means of a first embodiment of a method in accordance with the invention. The (nearly) finished device 10 (see Fig. 4) comprises a semiconductor body 12, here of p-type silicon which here
30 is formed by a substrate 11 and in which a first transistor 1 is formed as an NMOST. In a N-well region 33 a second transistor 2 is formed as a PMOST. The transistors 1,2 comprise source and drain regions 1A,1B,2A,2B, respectively of the n- and p-type conductivity, dielectric regions 1C,2C, here comprising silicon dioxide, and gate regions 1D,2D. In the

surface of the semiconductor body 12 isolation regions 25 are formed, here in the form of trenches filled with silicondioxide (or with another gate dielectric ,e.g. a metal oxide).

The gate region 1D of the NMOST 1 comprises in this example a compound comprising Mo and C and with a composition of MoC_x where $x \leq 1$. e.g. Mo_2C , of which the work function is about 3.6 to 3.8 eV and thus close to the optimal value of about 4.2 eV. The gate region 2D of the PMOST 2 comprises in this example a compound comprising Mo and O and with a composition of MoO_x , where $x \leq 2$, e.g. MoO_2 , of which the work function is about 4.6 to 5.5 eV and thus can be tuned to the optimal value of about 5.2 eV.

The device 10 is manufactured as follows. Starting point (see Fig. 1) is a p-type substrate 11 in which the n-well 33 and the STI (=Shallow Trench Isolation) regions 25 are formed. Next a dielectric layer 21 is formed and on thereon a metal layer 22, here comprising porous Mo, is deposited by vapor deposition.

Subsequently (see Fig. 2) a mask 15 is formed at the location of the PMOST 2 and the metal layer 22 is under heating to $T > 250$ degrees Celsius exposed to a gaseous compound 30 comprising C, here CH_4 , preferably also aided by plasma. The metal layer 22 is at the location of the NMOST 1 converted to the desired compound Mo_2C , or to a compound with a composition in the range indicated before. which will form later on the gate region 1D. The mask 15 comprises here TiN and is formed by deposition of a TiN layer which is patterned using photolithography and etching.

Hereinafter, a similar procedure is done (see Fig. 3) for the PMOST 2. Now the NMOST 1 is protected by a mask 16 and the Mo layer 22 is exposed to a gaseous compound comprising O, here O_2 under heating to $T > 250$ degrees Celsius. The conditions are such that the Mo layer 22 is locally converted to MoO_2 (or to a compound with a composition in the range indicated before) which will form the gate region 2D of the PMOST 2.

The manufacturing is then continued in a usual manner in that gate stacks are formed by photolithography and etching. Formation of shallow parts of the source and drain regions 1A,1B,2A,2B is followed by the formation of spacers 44 and the deep source and drain implantations. Further steps like the deposition of pre-metal dielectric, patterning thereof, contact metal deposition and patterning thereof are not shown in the drawing.

Figs. 5 through 7 are sectional views of a second example of a semiconductor device according to the invention at various stages in the manufacture of the device by means of a second embodiment of a method in accordance with the invention. The device 10 of this example is identical to that of the previous example. The first step (see Fig. 5) is the same as

described above. Next (see Fig. 6) the metal layer 22 comprising porous Mo is completely exposed to the treatment with the gaseous compound 30 comprising CH₄. In this way the metal layer 22 is converted in both transistors 1,2 to Mo₂C. Then (see Fig. 7) a mask 17 is formed in the region of the NMOST 1 and the Mo₂C layer is treated with a gaseous compound 40 comprising oxygen and converted to MoO₂. In this process the C atoms in the gate region 2D are converted to a gaseous compound of C and O and released from the gate region 2D.

The manufacturing is continued as described in the first example.

Fig. 8 is a sectional views of a third example of a semiconductor device according to the invention at a relevant stage in the manufacture of the device by means of a third embodiment of a method in accordance with the invention. In this example both gate regions 1D,2D comprise a compound of Mo and O. The gate region 1D of the NMOST 1 comprises MoO₃ which has a work function of 3.9 to 4.1 eV and thus is nearly optimal for this transistor. The gate region 2D of the PMOST 2 comprises MoO₂ as in the previous examples. The manufacture starts as shown in Fig. 5 and described above. The Mo layer 22 then is then (see Fig. 6) converted into MoO₂ layer 23 using the treatment with gaseous compound 40 containing O. Next (see Fig. 8) the PMOST 2 area is protected by mask 18 and the MoO₂ layer 23 is locally – at the location of the NMOST 1 – further oxidized to MoO₃, the latter material having a workfunction of about 3.9 to 4.1 eV which is nearly optimal for the latter transistor 1. The manufacture then continues as described before.

Furthermore, good results were also obtained with a compound of Mo and oxygen as the conducting material for a PMOST and with a compound of Mo and a chalcogenide like Tellurium for a NMOST. The first mentioned compound was obtained by local oxidation of a Mo layer, the second mentioned compound was obtained by locally implanting Tellurium ions in the Mo layer.

It will be obvious that the invention is not limited to the examples described herein, and that within the scope of the invention many variations and modification are possible to those skilled in the art. It is for example to be noted that also mixed compounds, i.e. compound containing more than two of the elements mentioned, e.g. a compound comprising Mo, C and O, can advantageously be applied.

CLAIMS:

1. Semiconductor device (10) with a substrate (11) and a semiconductor body (12) comprising a first field effect transistor (1) with a first source and drain region (1A,1B) and a first channel of a first conductivity type and with separated from the first channel by a first dielectric region (1C) a first gate region (1D) comprising a first conducting material and
5 a second field effect transistor (2) with a second source and drain region (2A,2B) and a second channel of a second, opposite to the first, conductivity type and with separated from the second channel by a second dielectric region (2C) a second gate region (2D) comprising a second conducting material different from the first conducting material, wherein the first and
10 element, characterized in that the first and second conducting material both comprise a compound containing as the metal a metal selected from the group comprising molybdenum and tungsten and both comprise as the further element an element selected from the group comprising carbon, oxygen and the chalcogenides.
- 15 2. Semiconductor device (10) according to claim 1, characterized in that both the first and second conducting material comprise a compound of molybdenum and carbon or oxygen.
- 20 3. Semiconductor device (10) according to claim 1 or 2, characterized in that the first conductivity type comprises the n-type and in that the first conducting material comprises a compound of molybdenum and carbon and the second conducting material comprises a compound of molybdenum and oxygen.
- 25 4. Semiconductor device (10) according to claim 1 or 2, characterized in that the first conductivity type comprises the n-type and in that the first conducting material comprises a compound of molybdenum and oxygen with a higher oxygen content and in that the second conducting material comprises a compound of molybdenum and oxygen with a lower oxygen content.

5. Semiconductor device (10) according to claim 1, characterized in that the first conducting material comprises a chalcogenide as the further element and the second conducting material comprises oxygen as the further element.

5 6. Method of manufacturing a semiconductor device (10) with a substrate (11) and a semiconductor body (12) comprising a first field effect transistor (1) with a first source and drain region (1A,1B) and a first channel of a first conductivity type and with separated from the first channel by a first dielectric region (1C) a first gate region (1D) comprising a first conducting material and a second field effect transistor (2) with a second source and
10 drain region (2A,2B) and a second channel of a second, opposite to the first, conductivity type and with separated from the second channel by a second dielectric region (2C) a second gate region (2D) comprising a second conducting material different from the first conducting material, wherein for the first and second conducting material a material is chosen comprising a compound containing both a metal and a further element, characterized in that
15 for the first and second conducting material both a material is chosen comprising a compound containing as the metal a metal selected from the group comprising molybdenum and tungsten and comprising as the further element an element selected from the group comprising carbon, oxygen and the chalcogenides.

20 7. Method according to claim 6, characterized in that for both the first and second conducting material a material is chosen comprising a compound of molybdenum and carbon or oxygen.

8. Method according to claim 6 or 7, characterized in that on the first and second
25 dielectric regions (1C,2C, 21) a layer (22) of the metal is formed which is at the location of the first dielectric region (1C) made to react with a gaseous compound (30) of the further element while the layer (22) of the metal at the location of the second dielectric region (2C) is protected against the gaseous compound (30) by a mask (15) and which after removal of the mask (15) is at the location of the second dielectric region (2C) made to react with a
30 gaseous compound (40) of the further element while the layer (22) of the metal at the location of the first dielectric region (1C) is protected against the gaseous compound (40) by a further mask (16).

9. Method according to claim 6 or 7, characterized in that on the first and second dielectric regions (1C,2C,21) a layer (23) of the first conducting material is deposited which is at the location of the second dielectric region (2C) is made to react with a gaseous compound (40) of the further element while the layer (23) of the first conducting material at the location of the first dielectric region (1C) is protected against the gaseous compound by a mask (17,18).

10. Method according to claim 9, characterized in that the layer (23) of the first conducting material is formed by depositing a layer (22) of the metal and reacting the metal layer (22) with a gaseous compound (30,40) of the further element.

11. Method according to claim 9, characterized in that the layer (23) of the first conducting material is formed by deposition of the metal layer (22) in an atmosphere comprising a gaseous compound.

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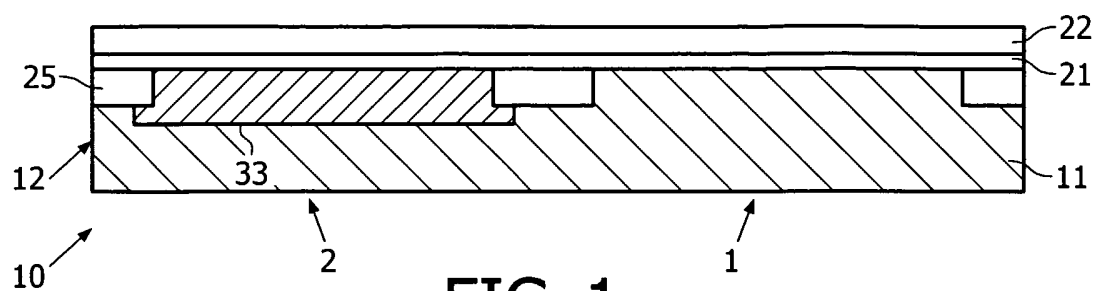


FIG. 1

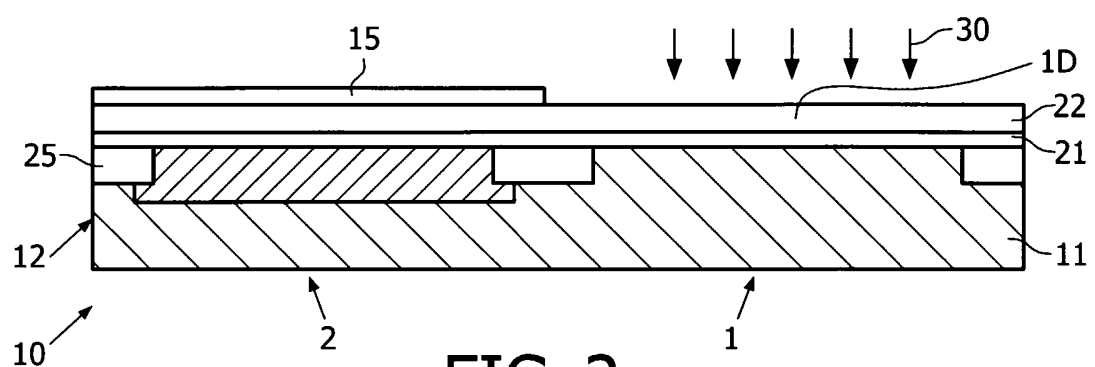


FIG. 2

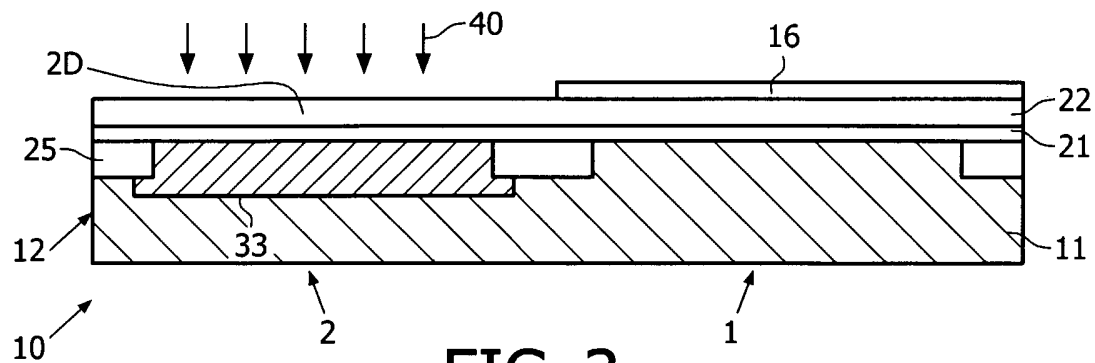


FIG. 3

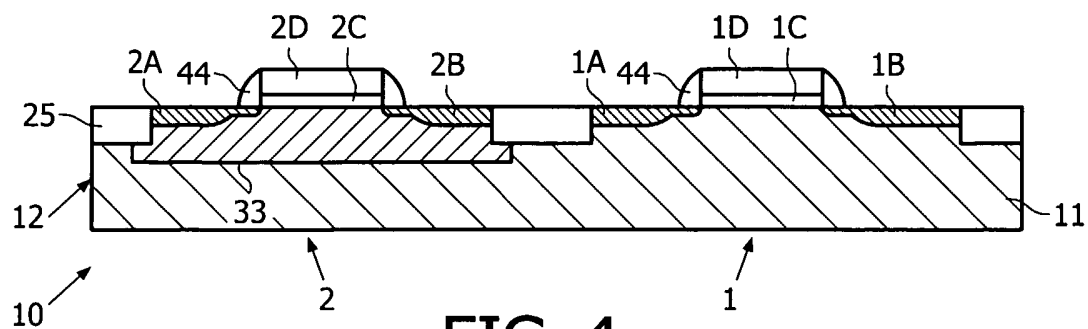


FIG. 4

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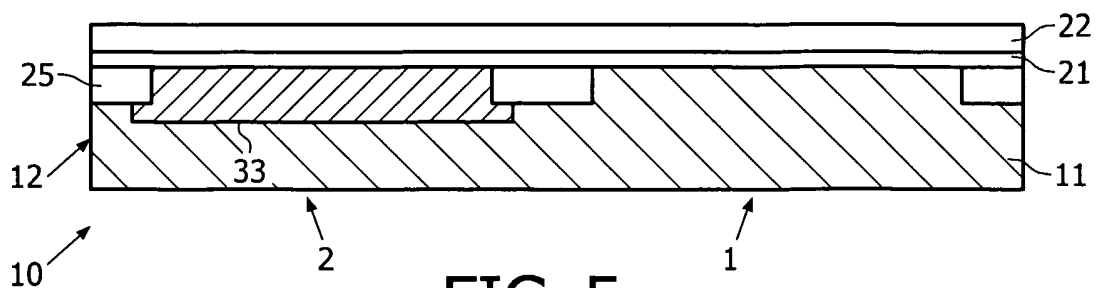


FIG. 5

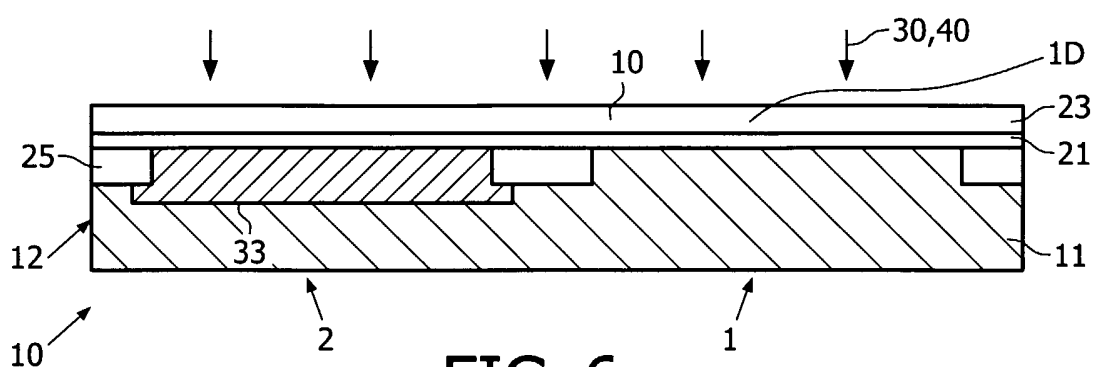


FIG. 6

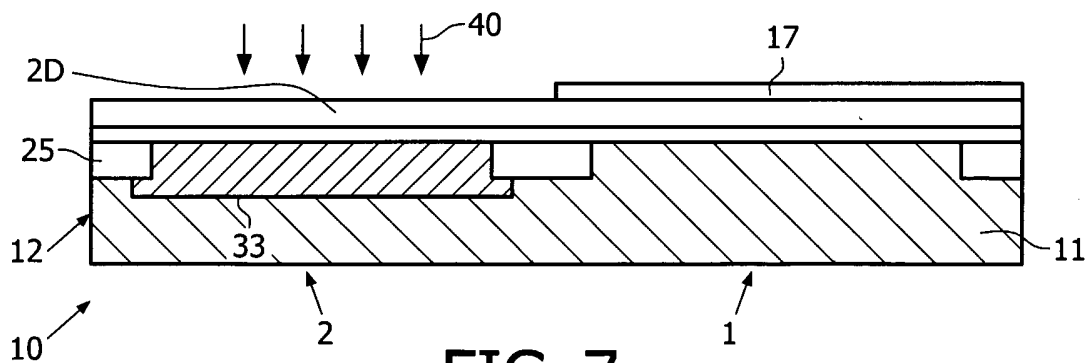


FIG. 7

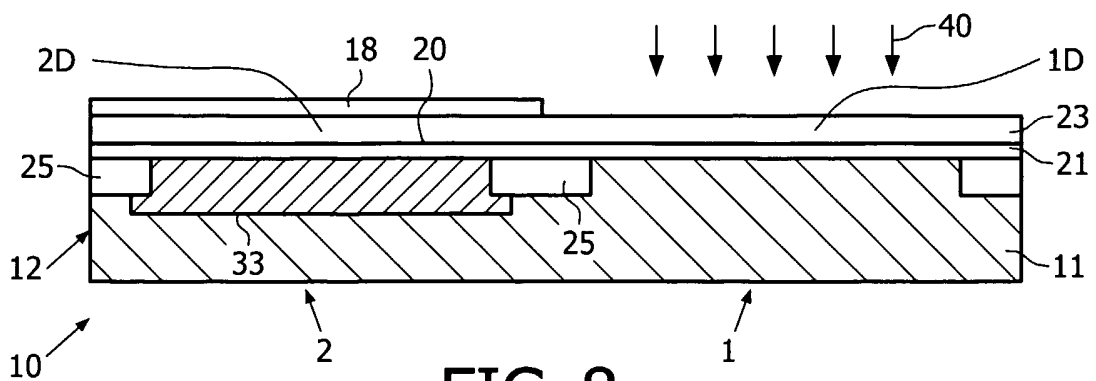


FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/052646

A. CLASSIFICATION OF SUBJECT MATTER

H01L21/8238

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/132239 A1 (LIN WENHE ET AL) 8 July 2004 (2004-07-08) abstract; claims; figures -----	1-11
Y	WO 03/079444 A (NEC CORPORATION; YOSHIHARA, TAKUYA) 25 September 2003 (2003-09-25) abstract; figures	1-11
P, Y	-& US 2005/110098 A1 (YOSHIHARA TAKUYA) 26 May 2005 (2005-05-26) abstract; figures -----	1-11
A	US 6 091 122 A (BUCHANAN ET AL) 18 July 2000 (2000-07-18) abstract; claims; figures -----	1-11
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

17 November 2005

Date of mailing of the international search report

25/11/2005

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Wirner, C

INTERNATIONAL SEARCH REPORT

Inte 1al Application No
PCT/IB2005/052646

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 2003, no. 12, 5 December 2003 (2003-12-05) -& JP 2004 207481 A (RENESAS TECHNOLOGY CORP), 22 July 2004 (2004-07-22) abstract; figures -----	1-11
A	US 2004/124492 A1 (MATSUO KOUJI) 1 July 2004 (2004-07-01) abstract; figures -----	1-11
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A	OHJUFU S-I ET AL: "OXYGEN-DOPED MOLYBDENUM FILMS FOR MOS GATE APPLICATION" JOURNAL OF THE ELECTROCHEMICAL SOCIETY, ELECTROCHEMICAL SOCIETY. MANCHESTER, NEW HAMPSHIRE, US, vol. 131, no. 2, February 1984 (1984-02), pages 446-450, XP001073829 ISSN: 0013-4651 abstract -----	1-11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/IB2005/052646

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