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[Continued on next page]

(54) Title: MICROELECTRONIC DEVICE AND METHOD OF MANUFACTURING SAME

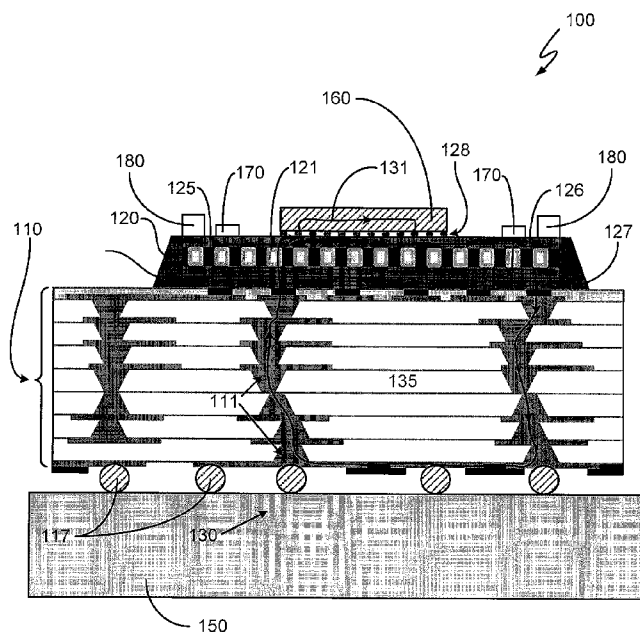


FIG. 1

(57) Abstract: A microelectronic device comprises a first substrate (110) having a first electrically conductive path (111) therein and a second substrate (120) above the first substrate and having a second electrically conductive path (121) therein, wherein the first electrically conductive path and the second electrically conductive path are electrically connected to each other and form a portion of a current loop (131) of an inductor (130).



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MICROELECTRONIC DEVICE AND METHOD OF MANUFACTURING
SAME

FIELD OF THE INVENTION

5 The disclosed embodiments of the invention relate generally to microelectronic device packaging, and relate more particularly to inductive loops in microelectronic device packaging.

BACKGROUND OF THE INVENTION

10 Integrated circuit dies and other microelectronic devices are typically enclosed within a package that, among other functions, enables electrical connections to be made between the die and a socket, a motherboard, or another next-level component. As die sizes shrink and interconnect densities increase, such electrical connections must be scaled so as to match both the smaller pitches typically found at the die and the larger pitches typically found at the next-level component.

15 One approach to interconnect scaling within microelectronic packages is to use multiple substrates to handle the space transformation from die bump pitch, where a typical pitch value may be 150 micrometers (microns or μm) to system board level pitch, where a typical pitch value may be 1000 μm , i.e., 1.0 millimeter (mm). This multiple-substrate architecture requires one or more of the substrates to be thinner than a typical
20 server substrate (having a 400 μm core compared to an 800 μm core, for example), in order to stay within maximum height requirements and to provide a solution for high speed input/output (I/O) signals.

BRIEF DESCRIPTION OF THE DRAWINGS

25 The disclosed embodiments will be better understood from a reading of the following detailed description, taken in conjunction with the accompanying figures in the drawings in which:

 FIG. 1 is a cross-sectional view of a microelectronic device according to an embodiment of the invention;

30 FIG. 2 is a flowchart illustrating a method of manufacturing a microelectronic device according to an embodiment of the invention; and

 FIG. 3 is a conceptualized plan view of a current loop of the microelectronic device of FIG. 1 according to an embodiment of the invention.

 For simplicity and clarity of illustration, the drawing figures illustrate the general

manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the discussion of the described embodiments of the invention. Additionally, elements in the drawing figures are not necessarily drawn to scale. For example, the dimensions of some of the elements in the
5 figures may be exaggerated relative to other elements to help improve understanding of embodiments of the present invention. The same reference numerals in different figures denote the same elements, while similar reference numerals may, but do not necessarily, denote similar elements.

The terms “first,” “second,” “third,” “fourth,” and the like in the description and in
10 the claims, if any, are used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in sequences other than those illustrated or otherwise described herein. Similarly, if a method
15 is described herein as comprising a series of steps, the order of such steps as presented herein is not necessarily the only order in which such steps may be performed, and certain of the stated steps may possibly be omitted and/or certain other steps not described herein may possibly be added to the method. Furthermore, the terms “comprise,” “include,” “have,” and any variations thereof, are intended to cover a non-exclusive inclusion, such
20 that a process, method, article, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

The terms “left,” “right,” “front,” “back,” “top,” “bottom,” “over,” “under,” and the like in the description and in the claims, if any, are used for descriptive purposes and
25 not necessarily for describing permanent relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein. The term “coupled,” as used herein, is defined as directly or indirectly connected in an electrical or non-
30 electrical manner. Objects described herein as being “adjacent to” each other may be in physical contact with each other, in close proximity to each other, or in the same general region or area as each other, as appropriate for the context in which the phrase is used. Occurrences of the phrase “in one embodiment” herein do not necessarily all refer to the

same embodiment.

DETAILED DESCRIPTION OF THE DRAWINGS

In one embodiment of the invention, a microelectronic device comprises a first substrate having a first electrically conductive path therein and a second substrate above the first substrate and having a second electrically conductive path therein, wherein the first electrically conductive path and the second electrically conductive path are electrically connected to each other and form a portion of a current loop of an inductor.

It was mentioned above that a proposed multiple-substrate architecture requires one or more of the substrates to be thinner than a typical server substrate in order to stay within maximum height requirements and to provide a solution for high speed I/O signals. A key component for enabling a fully integrated voltage regulator (FIVR) on future generation products is an inductor contained within the microelectronic package. Currently, the best inductor structures use thick-core substrates with large plated through holes (PTHs), but high speed I/O demands require the use of thinner substrate cores with smaller PTHs. Cost pressures are also driving a trend toward thinner substrate cores. The need to use a thinner core, however, dictates that the current loop area in the inductor is reduced, leading to lower inductor performance.

On-package inductance is critical for enabling FIVR and future power delivery architectures. Embodiments of the invention address the inductor performance concerns by forming inductor structures continuously through both the first and second substrates. This architecture effectively increases the area (e.g., the length) of the current loop, leading to higher inductor performance. In other words, embodiments of the invention enable an increased separation (z-height) between inductor coils and back side metal, which is a key parameter to increase the inductor performance in an air core inductor. Embodiments of the invention thus address and resolve an inherent conflict between power delivery requirements and signal integrity requirements in future substrates.

Referring now to the drawings, FIG. 1 is a cross-sectional view of a microelectronic device 100 according to an embodiment of the invention. As illustrated in FIG. 1, microelectronic device 100 comprises a substrate 110 having an electrically conductive path 111 therein.

Substrate 110 may comprise any suitable type of package substrate or other die carrier. In one embodiment, the substrate 110 comprises a multilayer substrate including a

number of alternating layers of metallization and dielectric material. Each layer of metallization comprises a number of conductors (e.g., traces), and these conductors may comprise any suitable conductive material, such as copper. Further, each metal layer is separated from adjacent metal layers by the dielectric layers, and adjacent metal layers may be electrically interconnected by microvias or other conductive vias. The dielectric layers may comprise any suitable insulating material—e.g., polymers, including both thermoplastic and thermosetting resins or epoxies, ceramics, etc.—and the alternating layers of metal and dielectric material may be built-up over a core layer of a dielectric material (or perhaps a metallic core).

As an example, and as illustrated in FIG. 1, electrically conductive path 111 can comprise one or more microvias that electrically connect adjacent internal layers of substrate 110. Such microvias can be arranged one on top of another in a straight line or they can be staggered such that they only partially overlap. Another possible microvia arrangement is one in which the microvias do not overlap at all but rather are connected by electrically conductive traces that run between them. As another example, electrically conductive path 111 can comprise a plated through hole or the like that extends throughout the entire extent of substrate 110.

Microelectronic device 100 further comprises a substrate 120 that is located above substrate 110 and has an electrically conductive path 121 therein, and a die 160 located above substrate 120. Although electrically conductive path is shown as passing into die 160, corresponding electrically conductive paths of other (non-illustrated) embodiments may instead pass underneath the die without extending into it. Microelectronic device 100 may further comprise die-side capacitors 170 and/or additional components 180, which, for example, could be resistors, capacitors, inductors, active devices, stiffeners, or the like.

In one embodiment, substrate 120 has a substrate core having a thickness that is no greater than 400 μm . As an example, electrically conductive path 121 can comprise a plated through hole or the like that extends through a core 125 of substrate 120. Electrically conductive path 121 may then further comprise a metal trace or the like that passes through build-up or similar layers 126 that surround core 125. Alternatively, substrate 120 may be made up entirely of such build-up or similar layers and may not have a core, in which case substrate 120 may have a total thickness in a range of approximately 200-500 μm .

Whatever their details, electrically conductive paths 121 and 111 are electrically

connected to each other and form a portion of a current loop 131 of an inductor 130. A conceptualized depiction of current loop 131 is shown in plan view in FIG. 3, described below.

To reiterate concepts that were touched upon earlier herein, or that are otherwise relevant to the current discussion, the precise regulation of power is an increasingly-
5 important function of high-density, high-performance microelectronic devices. Local voltage regulators, including FIVRs, are essential components of this effort; high-quality integrated passive devices, including inductors, are, in turn, important components of functioning voltage regulators. Accordingly, inductor 130 may be useful in managing
10 power regulation for microelectronic device 100. Among other things, this means that inductor 130 may be a component of, or may be connected to, voltage regulation circuitry in die 160.

The inductor structure of embodiments of the invention may experience increased performance by voiding metal (e.g., copper) in the region of substrate 110 that lies within
15 the inductor core area during manufacture of the substrate. This process does not require any special procedures and thus does not increase costs over those associated with the normal manufacturing process of substrate 110. Accordingly, in one embodiment inductor 130 has a core 135 that is characterized by an absence of metal. In other words, in one embodiment, inductor 130 acts like an air core inductor.

20 In one embodiment, microelectronic device 100 may be used as a way to achieve pitch translation between a die and an associated printed circuit board (PCB) or the like. To that end, the system level interface at the PCB (indicated by reference numeral 150 in FIG. 1) may be handled by substrate 110, while the die level interface may be handled by substrate 120. In a particular manifestation of this (or another) embodiment, substrate 110
25 has a first surface area and comprises a set of interconnects 117 having a first pitch, substrate 120 has a second surface area and comprises a set of interconnects 127 having a second pitch at a first surface thereof and a set of interconnects 128 having a third pitch at a second surface thereof. It should be noted that substrate 120 is coupled to substrate 110 using interconnects 127, the first pitch is larger than the second pitch, which in turn is
30 larger than the third pitch, and the first surface area is larger than the second surface area. In this embodiment, interconnects 117 form part of electrically conductive path 111 and interconnects 127 and 128 form part of electrically conductive path 121.

FIG. 2 is a flowchart illustrating a method 200 of manufacturing a microelectronic

device according to an embodiment of the invention. As an example, method 200 may result in the formation of a microelectronic device that is similar to microelectronic device 100 that is first shown in FIG. 1.

A step 210 of method 200 is to provide a first substrate having a first electrically
5 conductive path therein. As an example, the first substrate and the first electrically conductive path can be similar to, respectively, substrate 110 and electrically conductive path 111 that are both shown in FIG. 1. In one embodiment, step 210 comprises forming a first plurality of vias and a first plurality of traces therein. As an example, these can include components that are similar to those shown in FIG. 1.

10 A step 220 of method 200 is to provide a second substrate having a second electrically conductive path therein. As an example, the second substrate and the second electrically conductive path can be similar to, respectively, substrate 120 and electrically conductive path 121 that are both shown in FIG. 1. In one embodiment, step 220 comprises forming a second plurality of vias and a second plurality of traces therein. As an
15 example, these can include components that are similar to those shown in FIG. 1.

A step 230 of method 200 is to connect a die to the second substrate. As an example, the die can be similar to die 160 that is shown in FIG. 1.

A step 240 of method 200 is to connect the first substrate and the second substrate to each other such that the first electrically conductive path and the second electrically
20 conductive path are electrically connected to each other and form a portion of a current loop of an inductor. As an example, the inductor and the current loop can be similar to, respectively, inductor 130 and current loop 131 that are both shown in FIG. 1. In one embodiment, step 240 comprises arranging the first and second pluralities of vias and the first and second pluralities of traces such that the portion of the current loop comprises a
25 first one of the first plurality of vias, a first one of the second plurality of vias, a first one of the second plurality of traces, a second one of the second plurality of vias, a second one of the first plurality of vias, and a first one of the first plurality of traces.

In one embodiment, step 210, step 220, and/or another step of method 200 comprises voiding metal in a core of the inductor. As an example, this can comprise
30 applying to at least one of the first substrate and the second substrate a mask that prevents metal from being formed in the inductor core.

FIG. 3 is a plan view of current loop 131 of microelectronic device 100 according to an embodiment of the invention. It will be readily apparent from its appearance that

FIG. 3 is a highly-conceptualized drawing, included herein more for its broad structural overview than for its illustration of details. As shown, FIG. 3 is related to FIG. 1 in that FIG. 1 is a cross-section taken along line 1-1 in FIG. 3.

Visible in FIG. 3 is a top portion of electrically conductive path 121 as introduced in FIG. 1. Underneath that top portion, and thus not visible in FIG. 3, would be the balance of electrically conductive path 121 as well as electrically conductive path 111, along with other portions of current loop 131. The portion of current loop 131 represented in FIG. 3 by electrically conductive path 121, trace 322, and feature 323 corresponds roughly to the portion of current loop 131 that is visible in FIG. 1. Current loop 131 continues with additional electrically conductive features that correspond to those mentioned above and that collectively loop around a space that acts as a core of inductor 130.

Although the invention has been described with reference to specific embodiments, it will be understood by those skilled in the art that various changes may be made without departing from the spirit or scope of the invention. Accordingly, the disclosure of embodiments of the invention is intended to be illustrative of the scope of the invention and is not intended to be limiting. It is intended that the scope of the invention shall be limited only to the extent required by the appended claims. For example, to one of ordinary skill in the art, it will be readily apparent that the microelectronic device and the related structures and methods discussed herein may be implemented in a variety of embodiments, and that the foregoing discussion of certain of these embodiments does not necessarily represent a complete description of all possible embodiments.

Additionally, benefits, other advantages, and solutions to problems have been described with regard to specific embodiments. The benefits, advantages, solutions to problems, and any element or elements that may cause any benefit, advantage, or solution to occur or become more pronounced, however, are not to be construed as critical, required, or essential features or elements of any or all of the claims.

Moreover, embodiments and limitations disclosed herein are not dedicated to the public under the doctrine of dedication if the embodiments and/or limitations: (1) are not expressly claimed in the claims; and (2) are or are potentially equivalents of express elements and/or limitations in the claims under the doctrine of equivalents.

CLAIMS

What is claimed is:

1. A microelectronic device comprising:
 - 5 a first substrate having a first electrically conductive path therein; and
 - a second substrate above the first substrate, the second substrate having a second electrically conductive path therein,wherein:
 - 10 the first electrically conductive path and the second electrically conductive path are electrically connected to each other and form a portion of a current loop of an inductor.
2. The microelectronic device of claim 1 wherein:
 - the inductor has an inductor core that is characterized by an absence of metal.
3. The microelectronic device of claim 1 further comprising:
 - 15 a die containing voltage regulation circuitry, wherein the inductor is connected to the voltage regulation circuitry.
4. The microelectronic device of claim 1 wherein:
 - the second substrate comprises a substrate core; and
 - a thickness of the substrate core is no greater than 400 micrometers.
5. The microelectronic device of claim 1 wherein:
 - 20 the first substrate has a first surface area and comprises a first set of interconnects having a first pitch; and
 - the second substrate has a second surface area and comprises a second set of interconnects having a second pitch at a first surface thereof and a third set of
 - 25 interconnects having a third pitch at a second surface thereof,wherein:
 - the second substrate is coupled to the first substrate using the second set of interconnects;
 - the first pitch is larger than the second pitch;
 - 30 the second pitch is larger than the third pitch; and
 - the first surface area is larger than the second surface area.
6. The microelectronic device of claim 5 wherein:
 - the first set of interconnects form part of the first electrically conductive path; and

the second set of interconnects form part of the second electrically conductive path.

7. A microelectronic device comprising:

a first substrate having a first electrically conductive path therein;

5 a second substrate above the first substrate, the second substrate having a second electrically conductive path therein; and

a die above the second substrate,

wherein:

10 the first electrically conductive path and the second electrically conductive path are electrically connected to each other and form a portion of a current loop of an inductor.

8. The microelectronic device of claim 7 wherein:

the inductor has an inductor core that is characterized by an absence of metal.

9. The microelectronic device of claim 7 wherein:

the second substrate comprises a substrate core; and

15 a thickness of the substrate core is no greater than 400 micrometers.

10. The microelectronic device of claim 7 wherein:

the first substrate has a first surface area and comprises a first set of interconnects having a first pitch; and

20 the second substrate has a second surface area and comprises a second set of interconnects having a second pitch at a first surface thereof and a third set of interconnects having a third pitch at a second surface thereof,

wherein:

the second substrate is coupled to the first substrate using the second set of interconnects;

25 the first pitch is larger than the second pitch;

the second pitch is larger than the third pitch; and

the first surface area is larger than the second surface area.

11. The microelectronic device of claim 10 wherein:

the first set of interconnects form part of the first electrically conductive path; and

30 the second set of interconnects form part of the second electrically conductive path.

12. A method of manufacturing a microelectronic device, the method comprising:

providing a first substrate having a first electrically conductive path therein;

providing a second substrate having a second electrically conductive path therein;

and

connecting the first substrate and the second substrate to each other such that the first electrically conductive path and the second electrically conductive path are electrically connected to each other and form a portion of a current loop of an inductor.

5 13. The method of claim 12 further comprising:

connecting a die to the second substrate.

14. The method of claim 13 wherein:

providing the first substrate comprises forming a first plurality of vias and a first plurality of traces therein;

10 providing the second substrate comprises forming a second plurality of vias and a second plurality of traces therein; and

physically connecting the first substrate and the second substrate to each other comprises arranging the first and second pluralities of vias and the first and second pluralities of traces such that the portion of the current loop comprises a first one of the first plurality of vias, a first one of the second plurality of vias, a first one of the second plurality of traces, a second one of the second plurality of vias, a second one of the first plurality of vias, and a first one of the first plurality of traces.

15 15. The method of claim 13 further comprising:

voiding metal in a core of the inductor.

20 16. The method of claim 15 wherein:

voiding metal in the core of the inductor comprises applying to at least one of the first substrate and the second substrate a mask that prevents metal from being formed in the core.

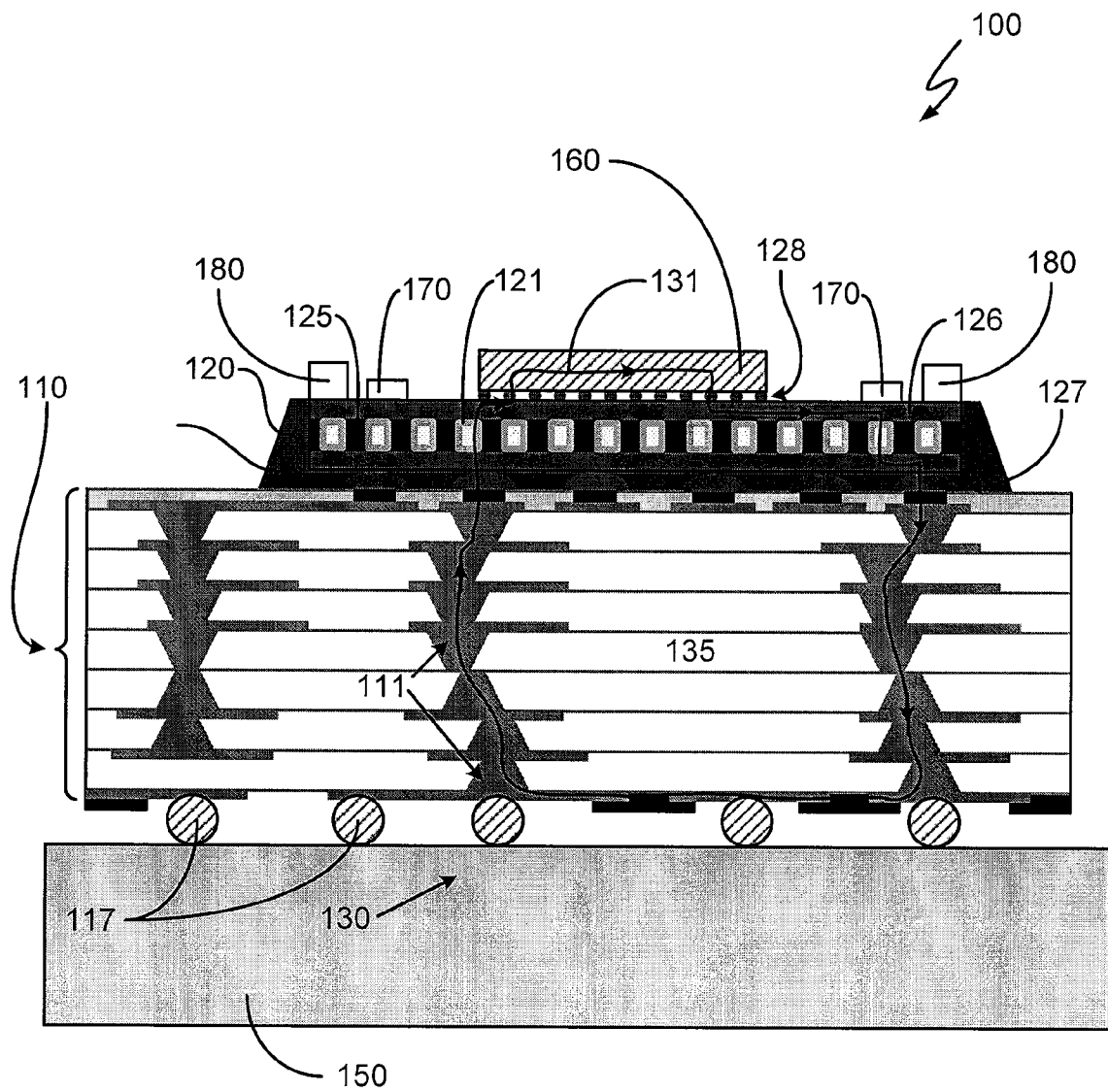
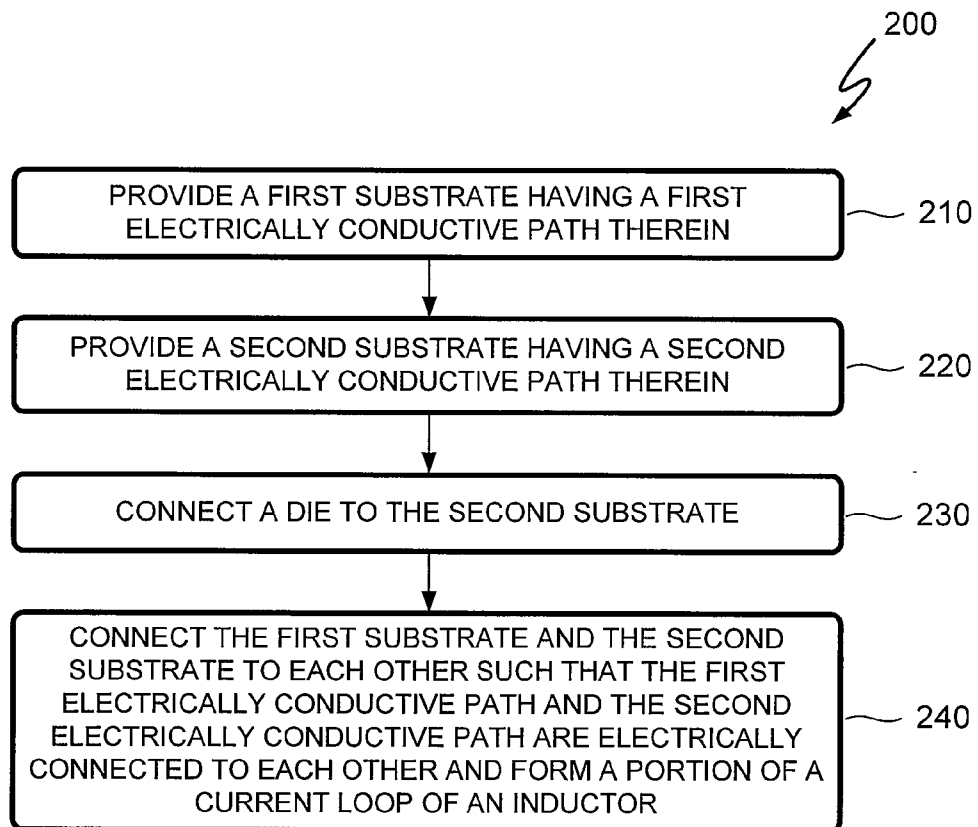


FIG. 1

*FIG. 2*

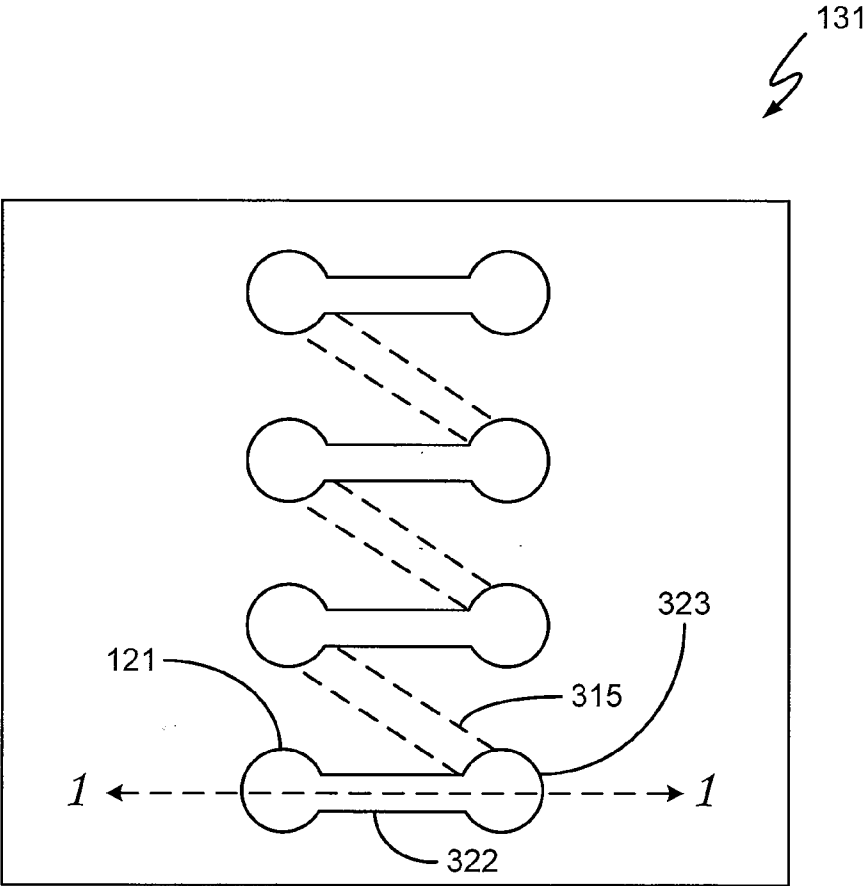


FIG. 3

A. CLASSIFICATION OF SUBJECT MATTER***H01L 23/485(2006.01)i, H01L 23/50(2006.01)i, H01L 23/12(2006.01)i, H01L 23/14(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/485; H01L 29/00; H01L 21/60; H01L 23/48; H01L 29/40; H01L 23/02; H01L 23/552

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: electronic device, substrate, inductor and current loop

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 2003-0218235 A1 (DAMION, T. SEARLS et al.) 27 November 2003 See the abstract, paragraphs [0003], [0021]-[0029], claims 1,10 and figures 1,8-12.	1-16
A	US 6323735 B1 (WELLAND; DAVID R. et al.) 27 November 2001 See the abstract, and columns 12-18, figures 5A-11.	1-16
A	US 2007-0194427 A1 (YUN-SEOK CHOI et al.) 23 August 2007 See the abstract, paragraphs [0025]-[0029], [0036], claims 1-5 and figures 1,2.	1-16
A	US 7141883 B2 (DERRICK C. WEI et al.) 28 November 2006 See the abstract, column 4, line 4 - column 5, line 60, claim 15 and figures 1-10.	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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