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(54) Title: METHODS OF REDUCING SUBSTRATE DISLOCATION DURING GAPFILL PROCESSING

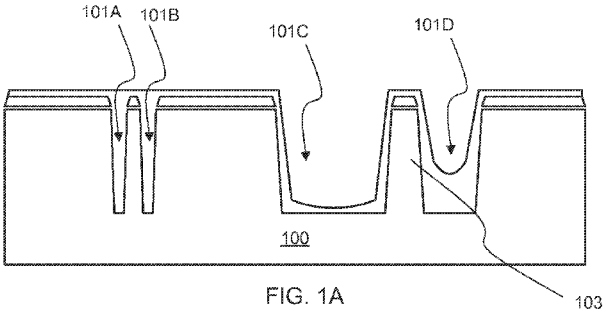

FIG. 1A

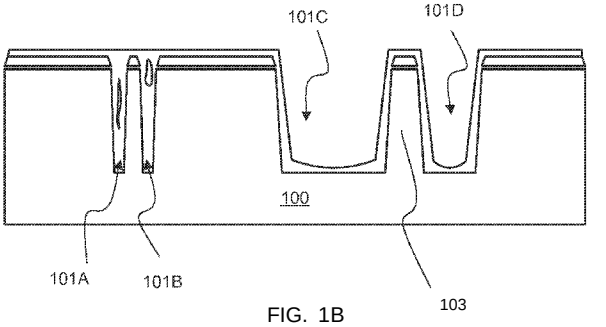

FIG. 1B

(57) Abstract: Methods of reducing dislocation in a semiconductor substrate between asymmetrical trenches are described. The methods may include etching a plurality of trenches on a semiconductor substrate and may include two adjacent trenches of unequal width separated by an unetched portion of the substrate. The methods may include forming a layer of dielectric material on the substrate. The dielectric material may form a layer in the trenches located adjacent to each other of substantially equivalent height on both sides of the unetched portion of the substrate separating the two trenches. The methods may include densifying the layer of dielectric material so that the densified dielectric within the two trenches of unequal width exerts a substantially similar stress on the unetched portion of the substrate that separates them.

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METHODS OF REDUCING SUBSTRATE DISLOCATION DURING GAPFILL PROCESSING

BRIEF DESCRIPTION OF THE DRAWINGS

A further understanding of the nature and advantages of the disclosed embodiments may be realized by reference to the remaining portions of the specification and the drawings.

FIG. 1A shows a cross-sectional view of a semiconductor substrate on which a dielectric material has been deposited.

FIG. 1B shows a cross-sectional view of a semiconductor substrate on which a dielectric material has been deposited.

FIG. 2 shows a cross-sectional view of a semiconductor substrate on which methods according to disclosed embodiments have been performed.

FIG. 3 shows a cross-sectional view of a semiconductor substrate on which trenches have been etched.

FIG. 4 shows a flowchart of a method of reducing dislocation caused by a deposited dielectric material on a semiconductor substrate.

In the appended figures, similar components and/or features may have the same numerical reference label. Further, various components of the same type may be distinguished by following the reference label by a letter that distinguishes among the similar components and/or features. If only the first numerical reference label is used in the specification, the description is applicable to any one of the similar components and/or features having the same first numerical reference label irrespective of the letter suffix.

DETAILED DESCRIPTION OF THE INVENTION

Methods are described herein for reducing dislocation of a silicon lattice in a semiconductor substrate on which trench filling is performed simultaneously in both dense and less densely patterned regions. The methods allow for the forming of a dielectric layer on a semiconductor substrate that has both a densely patterned region as well as a region having wider trenches. The two regions may have the dielectric material formed simultaneously in a single deposition processing step. The deposition may allow the trenches in the dense region to be substantially filled with the dielectric material without the formation of voids or seams, while filling wider trenches in the other region to a substantially equivalent height. A

substantially equivalent height, regardless of the width of the trenches, may provide a reduction of dislocation of the substrate in the region with wider trenches during a subsequent densification of the dielectric material.

Dielectric layers deposited on substrates during semiconductor fabrication may take a variety of forms. For example, more flowable films may be used to fill narrow gaps, but may deposit a less dense, lower quality film. Conformal films may be used to fill wider trenches with a denser dielectric layer, but may create voids or seams if utilized for filling narrow trenches. Another potential issue with some flowable films is that if a thick film is deposited, subsequent densification of the film may create large stresses that are imposed on the underlying substrate. By creating a more conformal dielectric film that also possesses flowable properties, a dielectric may be formed that fills a narrow trench without voids, while at the same time produces a substantially conformal fill of wider trenches.

For example, as shown in FIG.1A, a semiconductor substrate 100 may have a region with several narrow trenches 101A, 101B and a separate region with wider trenches 101C, 101D. If a more conventional flowable film is used for gapfilling over the entire substrate, narrow gaps 101A, 10IB may be filled seamlessly because the deposited film may initially flow when deposited from the tops of the trenches towards the bottom. However, as may occur with flowable dielectrics, in wider trenches 101C, 101D an equivalent volume of dielectric may be deposited in both trenches. Hence, less wide trench 101D may be filled to a greater height than wider trench 101C. Because flowable films have a lower density, the subsequent densification of the film may be accompanied by film shrinkage. As the film shrinks, a stress is imposed on the underlying substrate. The more material that shrinks, i.e. a trench that is filled to a greater height, the more stress may be imposed on the substrate. Hence for trenches of unequal width 101C, 101D the portion of the substrate in between the trenches 103 may have a disproportionate stress imposed on each side due to the unequal height of the fill. If the stress is great enough, the structure of the substrate, e.g., a silicon lattice, may have deformation occur or stacking faults form, which may weaken the integrity of the substrate. In more extreme cases, this deformation may result in unetched portion 103 collapsing.

Alternatively, as shown in FIG. IB, the same substrate trenches may be filled with a more conventional conformal film that fills trenches from the sidewalls in toward the center, regardless of the width of the trench. A higher quality film may be formed that fills wider trenches 101C, lOlD to a substantially similar height, thereby producing a substantially equivalent stress on the unetched portion of the substrate 103 between the two trenches.

However, in the narrower trenches 101A, 101B, the more conformal filling that forms from the sidewalls of the trench towards the center, may produce seams or breadloafing, which occurs when the film pinches off the top of the trench despite that the trench has not been filled. Because of these issues occurring between narrower and wider trenches, many conventional methods of substrate processing may involve separately patterning and subsequently filling more densely patterned regions of the substrate separately from less densely patterned regions. In this way, a more flowable film may be used for deposition in the narrow regions, and a more conformal film may be used for deposition in the wider regions. The inventors have surprisingly found that a more conformal film displaying flowable properties may be able to overcome the separate issues described above, and be used to fill narrow trenches without producing voids, while filling wider trenches in a more conformal manner to a similar height.

Methods of reducing dislocation in a semiconductor substrate between asymmetrical trenches are described. The methods may include etching a plurality of trenches on a semiconductor substrate, and may include two adjacent trenches of unequal width that are separated by an unetched portion of the substrate. The methods may further include forming a layer of dielectric material on the substrate. The dielectric material may form a substantially uniform layer in the trenches so that the two trenches of unequal width are filled to a substantially equivalent height on both sides of the unetched portion of the substrate separating them. The methods may include densifying the layer of dielectric material so that the densified dielectric within the two trenches of unequal width exerts a substantially similar stress on the unetched portion of the substrate that separates them.

FIG. 2 is a cross-sectional view of a semiconductor substrate 200. Although not to scale, the substrate illustrates two configured regions 205 and 207. In one embodiment, the substrate may represent the cell region and periphery circuit region of a flash semiconductor substrate. A manufacturing process may be performed to create the structure as illustrated in the figure, and described herein. An insulating layer of dielectric material 210 may be deposited on the substrate regions 205, 207 and may serve as an insulating layer, or tunnel oxide as it is referred for a cell region and a gate insulating layer in a peripheral region. The tunnel oxide 210 may be a high quality dielectric such as a thermal oxide, or may alternatively be deposited by other HDP-CVD or LPCVD processes. The tunnel oxide 210 may be any high quality oxide, and may be, for example, a thermally grown silicon oxide.

For semiconductor substrates used for flash devices such as NAND type flash, gate electrodes may be formed in both the cell region and the peripheral circuit region. A floating gate material 215 may be deposited on the tunnel oxide 210. The floating gate material 215 may be a polysilicon, silicon nitride, silicon oxide, or silicon oxy-nitride, a metalized oxide, or another material that may limit back-tunneling of stored charge. The floating gate material 215 may be deposited by an HDP-CVD, LPCVD, PVD, or other process for depositing suitable films.

Subsequent deposition of protective layers such as a nitride stop-layer, and an oxide mask layer (neither shown) may be deposited. The mask layer may be deposited to create a pattern for the isolation of structures on the substrate. As shown in FIG. 2, trenches may be etched in both the cell region 205 and the peripheral circuit region 207. The trenches may be of various depths and widths, and may be from less than about 10 nm in width to more than about 2 μιη in width. The trenches etched in the cell region may have cell widths that are less than about 200 nm, and may also be less than about 150 nm, about 100 nm, about 80 nm, about 60 nm, about 50 nm, about 40 nm, about 30 nm, about 20 nm, about 10 nm, etc. or less. The trenches in the periphery circuit region may have cell widths that are greater than about 100 nm, and may also be greater than about 150 nm, about 200 nm, about 350 nm, about 500 nm, about 750 nm, about 1 μιη, about 1.5 μιη, about 2 μιη, etc. or more.

The patterning may be performed simultaneously over both the dense cell region as well as the peripheral circuit region thereby reducing the number of processing steps required for the manufacturing of the substrate. The trenches etched in the structure may vary between the cell region and the peripheral circuit region. For example, the trenches etched in the cell region may have trench widths that are less than about 50 nanometers, while the trenches etched in the peripheral circuit region may have trench widths that are greater than about 150 nm wide.

After the trenches have been etched, a dielectric material 220 may be deposited to create isolation regions on the semiconductor substrate. The dielectric may be deposited simultaneously on both the dense cell region of the substrate and the peripheral region that may contain wider trenches. The dielectric material 220 may exhibit a balance between flowable and conformal properties so that it may display the following properties: the dielectric may substantially fill the trenches in the dense cell region without producing voids or seams, and may also form a layer of dielectric in the peripheral region that may fill trenches of different width to a substantially equivalent height. The filling of the dense cell

regions without voids and seams may be performed by utilizing a dielectric material that displays flowable properties upon deposition such that a portion of the dielectric material deposited near the top of the trench flows toward the bottom. The dielectric material may also be limited in the flowable properties such that dielectric material deposited in the peripheral circuit region may fill asymmetrical trenches to a substantially equivalent height. The balance of properties may be provided by increasing the amount of a radical precursor gas and carrier gas, which provides a more conformal deposition to a flowable film.

After the dielectric material 220 has been deposited, a second layer of dielectric material 225, or a capping layer, may be deposited that fills the trenches in the peripheral region as well as completing the filling of any trenches in the cell region that were not filled by the initial dielectric material 220. The capping layer 225 may be deposited in the same or a different manner as dielectric 220, and may be deposited via HARP or E-HARP, for example. Subsequent to the deposition of the dielectric material layers, additional processing steps may be performed. For example, an etching or planarization step may be performed in order to remove excess material and expose the floating gate dielectric 215 in the cell region 205. An inter-gate dielectric may be deposited thereon in preparation for the deposition of a control gate to create a stacked gate structure in the cell region. The peripheral circuit region may contain electrodes of a single gate structure. Additional materials may then be deposited to form additional layers of structure.

The peripheral region 207 may have multiple trenches etched, as illustrated in FIG. 3. For example, the peripheral circuit region 207 may include two trenches of unequal width 350A, 350B that are located adjacently to one another. The trenches are thus separated by an unetched portion of the semiconductor substrate 309. Because flowable dielectrics may deposit a certain volume of dielectric material, if a general flowable dielectric were deposited in the trenches, the wider trench 350A may not be filled to the same height as the other trench 350B, because the same amount of dielectric deposited in each trench would fill to a disparate height. Were this to happen, when the deposited film was cured, an unequal stress may be imposed on each side of the unetched portion of the semiconductor substrate 309. In certain scenarios, the unequal stress may create stacking faults or dislocation within the silicon lattice, or may even cause the structure 309 to deform. Thus, the dielectric material that may be used in the trenches may be less flowable so that the dielectric material fills the trenches of unequal width 350A, 350B to a substantially similar height, although the material may still display flowable properties.

FIG. 4 shows a method 400 for reducing dislocation caused by a deposited dielectric material on a semiconductor substrate. The semiconductor substrate may be an unpatterned or patterned substrate, e.g. an unpatterned 300 mm silicon wafer for use as a nonvolatile semiconductor memory device such as a NAND type flash device. The method may initially include the optional step 410 of depositing material on the semiconductor substrate. The deposition 410 may include an initial layer of dielectric material that may function as a tunnel oxide, for example. A gate material such as, for example, polysilicon may be deposited on the tunnel oxide. Additional protective material and mask material may be deposited to form a pattern for etching.

Trenches may be etched 415 that create trenches for use in both a cell region of the substrate as well as a peripheral circuit region on the substrate. The trenches may be of various widths, and the trenches in the peripheral circuit region may be wider than the trenches etched in the cell region. The trenches may be etched in both the cell region and the peripheral circuit region simultaneously to limit the number of processing steps required overall. The trenches etched in the peripheral region may include two adjacent trenches of unequal width that are separated by an unetched portion of the semiconductor substrate.

A dielectric layer may be formed 420 over the semiconductor substrate on both the cell region and the peripheral circuit region. The dielectric material may be deposited by a CVD process and display flowable properties such that a portion of the dielectric material deposited near the top of a trench flows toward the bottom. Additionally, the dielectric material may form in the peripheral circuit region such that the adjacent trenches of unequal width are filled to a substantially similar height.

Subsequent to the deposition of the dielectric material, the dielectric may be densified 425 to convert the structure that may include Si-H and Si-N bonds to Si-0 bond, and reduce the porosity of the dielectric material. The densification may include a curing performed in an ozone environment as well as an annealing performed in a steam environment. The curing and annealing may be performed while the temperature of the substrate is maintained below about 600°C, or alternatively below about 500°C, about 400°C, about 300°C, about 200°C, about 100°C, etc. or less. Alternatively, the curing step may be performed while the temperature of the substrate is maintained between about 100°C and about 300°C, or between about 150°C and about 200°C. The annealing step may be performed while the temperature of the substrate is maintained between about 100°C and about 500°C, or between about 200°C and about 400°C. The densification may result in a shrinkage of the deposited

dielectric. As the material shrinks, the material may impose a tensile stress on the surrounding substrate structure. The lattice structure of the substrate may deform to an extent to address the imposed stress, and may shift to accommodate the stress. In areas where a disproportionate stress is imposed on the same structure, such as, for example, in adjacent trenches of unequal width, the competing stresses of differing magnitude may cause dislocations and/or stacking faults in the underlying structure, which may cause the substrate to deform or collapse. Thus, the height of the dielectric material deposited in the trenches may be substantially equal to reduce the chance of deformation.

Additional dielectric materials may be deposited 430 to fill any remaining trench volume on the substrate. The additional material may be deposited by a similar process, or alternatively may be deposited with a separate deposition technique such as, for example, a CVD technique such as E-HARP. The additional material may also be annealed after deposition and, the annealing may be performed above about 600°C, or alternatively above about 700°C, about 800°C, about 900°C, about 1000°C, about 1200°C, etc. or more.

Methods are also described for forming a layer of dielectric material on a patterned semiconductor substrate. The methods may include etching a plurality of trenches on a semiconductor substrate to form a pattern. The pattern may have a cell region of the substrate and a periphery circuit region of the substrate. The plurality of trenches may include at least two trenches in the periphery circuit region that are of unequal width and are located adjacent to each other such that an unetched portion of the substrate separates the two trenches. The plurality of trenches may also include at least one trench in the cell region of the substrate. The methods may include flowing a plurality of precursor gases into the deposition chamber, where the precursor gases include a silicon containing precursor, a nitrogen containing precursor, and an inert carrier gas. The flow rate of the nitrogen containing precursor may be at least about two times the flow rate of the silicon containing precursor, and the flow rate of the inert carrier gas may be at least about five times the flow rate of the silicon containing precursor. The methods may also include forming a layer of dielectric material on the semiconductor substrate on both the cell region and the periphery circuit region simultaneously. The dielectric material may be initially flowable upon deposition so that a portion of the dielectric material deposited near the top of a trench flows toward the bottom of the trench. The methods may further include subsequently densifying the layer of dielectric material.

The precursor gases may include a silicon-based precursor, and may include silyl-amines such as $H_2N(SiH_3)$, $HN(SiH_3)_2$, and $N(SiH_3)_3$, among other silyl-amines. These silyl-amines may be mixed with additional gases that may act as carrier gases, reactive gases, or both. Examples of carbon-free silicon precursors may also include silane (SiH_4) either alone or mixed with other silicon (e.g., $N(SiH_3)_3$), hydrogen (e.g., H_2), and/or nitrogen (e.g., N_2, NH_3) containing gases. The silicon-containing precursors may also include silicon compounds that have no carbon or nitrogen, such as silane, disilane, etc. If the deposited oxide film is a doped oxide film, dopant precursors may also be used such as TEB, TMB, $B_2I¾$, TEPO, PH_3, P_2H_6, and TMP, among other boron and phosphorous dopants. The flow rate of the silicon precursor may be greater than or about 100 seem, greater than or about 200 seem, greater than or about 250 seem, greater than or about 275 seem, greater than or about 300 seem, greater than or about 350 seem, greater than or about 400 seem, etc. or more in different embodiments

The precursors may include a nitrogen based precursor, and may include nitrogen as a radical precursor that passes through a remote plasma region prior to entering into the deposition chamber. When nitrogen is present in the radical precursor, it may be referred to as a radical-nitrogen precursor. The radical-nitrogen precursor includes plasma effluents created by exciting a more stable nitrogen-containing precursor in a plasma. For example, a relatively stable nitrogen-containing precursor containing NH_3 and/or hydrazine (N_2H_4) may be activated in a chamber plasma region or a remote plasma system (RPS) outside the processing chamber to form the radical-nitrogen precursor, which is then transported into a plasma-free substrate processing region. The stable nitrogen precursor may also be a mixture comprising NH_3 and N_2; NH_3 and H_2; NH_3, N_2, and H_2; and N_2 and H_2, in different embodiments. Hydrazine may also be used in place of or in combination with NH_3 in the mixtures with N_2 and H_2. The flow rate of the stable nitrogen precursor may be greater than or about 300 seem, greater than or about 400 seem, greater than or about 500 seem, greater than or about 600 seem, greater than or about 650 seem, greater than or about 700 seem, greater than or about 750 seem, greater than or about 800 seem, etc. or more in different embodiments. Nitrogen-containing precursors may also include N_20, NO, $N0_2$ and NH_4OH. The radical-nitrogen precursor produced may include one or more of -N, -NH, $-NH_2$, etc., and may also be accompanied by ionized species formed in the plasma. In other embodiments, the radical-nitrogen precursor is generated in a section of the processing chamber partitioned from the substrate processing region where the precursors mix and react to deposit the

silicon-and-nitrogen layer on a deposition substrate (e.g., a semiconductor wafer). The partition may be interchangeably referred to as a showerhead. The radical-nitrogen precursor may also be accompanied by a carrier gas such as argon, helium, etc.

The flowability may be due, at least in part, to a significant hydrogen component in the deposited film. For example the deposited film may have a silazane-type, Si-NH-Si backbone *(i.e.,* a Si-N-H film). Flowability may also result from short chained polymers of the silazane type. The nitrogen which allows the formation of short chained polymers and flowability may originate from either the radical precursor or the silicon-containing precursor. When both the silicon precursor and the radical-nitrogen precursor are carbon-free, the deposited silicon-and-nitrogen-containing film is also substantially carbon-free. Of course, "carbon- free" does not necessarily mean the film lacks even trace amounts of carbon. Carbon contaminants may be present in the precursor materials that find their way into the deposited silicon-and-nitrogen-containing film. The amount of these carbon impurities however are much less than would be found in a silicon precursor having a carbon moiety *(e.g.,* TEOS, TMDSO, etc.).

One or more additional gases and carrier gases may be included with the precursors, such as O_2, H_20 , Ar, H_2, N_2, He, etc., and may have a flow rate that is greater than or about 100 seem. Alternatively, the one or more carrier gases may have a flow rate that is greater than or about 200 seem, greater than or about 500 seem, greater than or about 750 seem, greater than or about 1000 seem, greater than or about 1500 seem, greater than or about 2000 seem, greater than or about 2500 seem, greater than or about 3000 seem, greater than or about 3500 seem, etc. or more. Additional gases including molecular oxygen, ozone, and/or water vapor may be included with the precursor gases as well.

Without being limited to any particular theory, the ability to produce a substantially conformal film that displays flowable film properties may be a result of an increase of ammonia radicals during the deposition process. The increase in ammonia radicals may be as a result of increasing the amount of ammonia and carrier gas delivered to the processing chamber. The increased amount of ammonia provides additional gas from which the radicals may be formed, and the increased amount of carrier gas may allow for a greater amount of dissociation from the ammonia. Hence, an enhanced amount of ammonia radials may be created and may produce a more conformal film when deposited. A conformal film that displays flowable properties may be produced from the precursor gases as a function of the silicon precursor gas used. For example, the nitrogen containing precursor, which may be

ammonia in one embodiment, may have a flow rate that is at least about two times the flow rate of the silicon containing precursor. Alternatively, the nitrogen containing precursor may be at least about 2.1, about 2.2, about 2.3, about 2.4, about 2.5, about 2.6, about 2.7, about 2.8, about 2.9, about 3, about 3.5, about 4, or about 5 times the flow rate of the silicon containing precursor. Additionally, the carrier gas may be at least about five times the flow rate of the silicon containing precursor. Alternatively, the carrier gas may be at least about 6, about 7, about 8, about 9, about 10, about 11, about 12, about 13, about 15, about 17, about 20, or about 25 times the flow rate of the silicon containing precursor.

The deposition may be performed in a deposition chamber in which the temperature of the substrate is maintained below about 600°C, or alternatively below about 500°C, about 400°C, about 300°C, about 200°C, about 100°C, about 75°C, about 65°C, about 50°C, about 40°C, about 30°C, etc. or less. The pressure maintained in the chamber may be at or below about 760 Torr, and may alternatively be below about 600 Torr, about 400 Torr, about 200 Torr, about 100 Torr, about 50 Torr, about 25 Torr, about 15 Torr, about 10 Torr, about 8 Torr, about 6 Torr, about 5 Torr, about 4 Torr, about 3 Torr, about 2 Torr, about 1 Torr, about 0.5 Torr, etc. or less.

In the preceding description, for the purposes of explanation, numerous details have been set forth in order to provide an understanding of various embodiments of the present invention. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the disclosed embodiments. Additionally, a number of well known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of the invention.

It is noted that individual embodiments may be described as a process which is depicted as a flowchart, a flow diagram, or a block diagram. Although a flowchart may describe the method as a sequential process, many of the operations may be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may be terminated when its operations are completed, but could have additional steps not discussed or included in a figure. Furthermore, not all operations in any particularly described process

may occur in all embodiments. A process may correspond to a method, a function, a procedure, a subroutine, a subprogram, etc. When a process corresponds to a function, its termination corresponds to a return of the function to the calling function or the main function.

Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Each smaller range between any stated value or intervening value in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

As used herein and in the appended claims, the singular forms "a", "an", and "the" include plural references unless the context clearly dictates otherwise. Thus, for example, reference to "a dielectric material" includes a plurality of such materials, and reference to "the process" includes reference to one or more processes and equivalents thereof known to those skilled in the art, and so forth.

Also, the words "comprise", "comprising", "include", "including", and "includes", when used in this specification and in the following claims, are intended to specify the presence of stated features, integers, components, or steps, but they do not preclude the presence or addition of one or more other features, integers, components, steps, acts, or groups.

WHAT IS CLAIMED IS:

1. A method of reducing dislocation in a semiconductor substrate between asymmetrical trenches, the method comprising:

etching a plurality of trenches on a semiconductor substrate, wherein the plurality of trenches includes two trenches that are of unequal width and are located adjacent to each other such that an unetched portion of the substrate separates the two trenches of unequal width;

forming a layer of dielectric material on the semiconductor substrate, wherein the dielectric material forms a layer in the trenches located adjacent to each other of substantially equivalent height on both sides of the unetched portion of the substrate separating the two trenches; and

densifying the layer of dielectric material, wherein the densified dielectric within the two trenches of unequal width exerts substantially equal stress on the unetched portion of the substrate.

2. The method of claim 1, wherein the layer of dielectric material is initially formed over the entire semiconductor substrate during a simultaneous deposition process step.

3. The method of claim 1, wherein at least one trench etched in the substrate has a trench width less than about 100 nanometers, and wherein the two trenches of unequal width have a trench width greater than about 100 nanometers.

4. The method of claim 3, wherein at least one trench etched in the substrate has a trench width less than about 50 nanometers, and wherein the two trenches of unequal width have a trench width greater than about 150 nanometers.

5. The method of claim 1, wherein the dielectric material is initially flowable when it is deposited on the semiconductor substrate so that a portion of the dielectric material deposited at the top of a trench flows toward the bottom of the trench.

6. The method of claim 1, wherein the temperature of the substrate during the forming of the dielectric layer is maintained below about 100°C, and wherein the forming of the dielectric layer on the substrate occurs in a processing chamber having a pressure below about 50 Torr.

7. The method of claim 6, wherein the temperature of the substrate during the forming of the dielectric layer is maintained below about 50°C, and wherein the forming of the dielectric layer on the substrate occurs in a processing chamber having a pressure below about 5 Torr.

8. The method of claim 1, wherein the densifying comprises:

curing the dielectric material in an ozone (O_3) environment; and

annealing the cured dielectric material in a steam environment.

9. The method of claim 8, wherein the temperature of the substrate during the curing and annealing is maintained at or below about 400°C.

10. The method of claim 9, wherein the temperature of the substrate during the curing is maintained at or below about 200°C.

11. The method of claim 1, wherein the forming of the dielectric layer further comprises:

flowing a nitrogen-containing precursor into a semiconductor deposition chamber in which the etched semiconductor substrate resides; and

flowing a silicon-containing precursor into the deposition chamber to come into contact with the nitrogen-containing precursor over the etched semiconductor substrate.

12. The method of claim 11, wherein the nitrogen-containing precursor is ammonia.

13. The method of claim 12, wherein the ammonia has been flowed through a remote plasma region prior to entering the semiconductor deposition chamber to create ammonia radicals.

14. A method of forming a layer of dielectric material on a patterned semiconductor substrate, the method comprising:

etching a plurality of trenches on a semiconductor substrate, wherein the plurality of trenches includes two trenches that are of unequal width and are located adjacent to each other such that an unetched portion of the substrate separates the two trenches of unequal width;

flowing a plurality of precursor gases into the deposition chamber, wherein:

the precursor gases comprise a silicon containing precursor, a nitrogen containing precursor, and an inert carrier gas,

the flow rate of the nitrogen containing precursor is at least about two times the flow rate of the silicon containing precursor, and

the flow rate of the inert carrier gas is at least about five times the flow rate of the silicon containing precursor;

forming a layer of dielectric material on the semiconductor substrate, wherein the dielectric material is initially flowable upon deposition so that a portion of the dielectric material deposited near the top of a trench flows toward the bottom of the trench; and

densifying the layer of dielectric material.

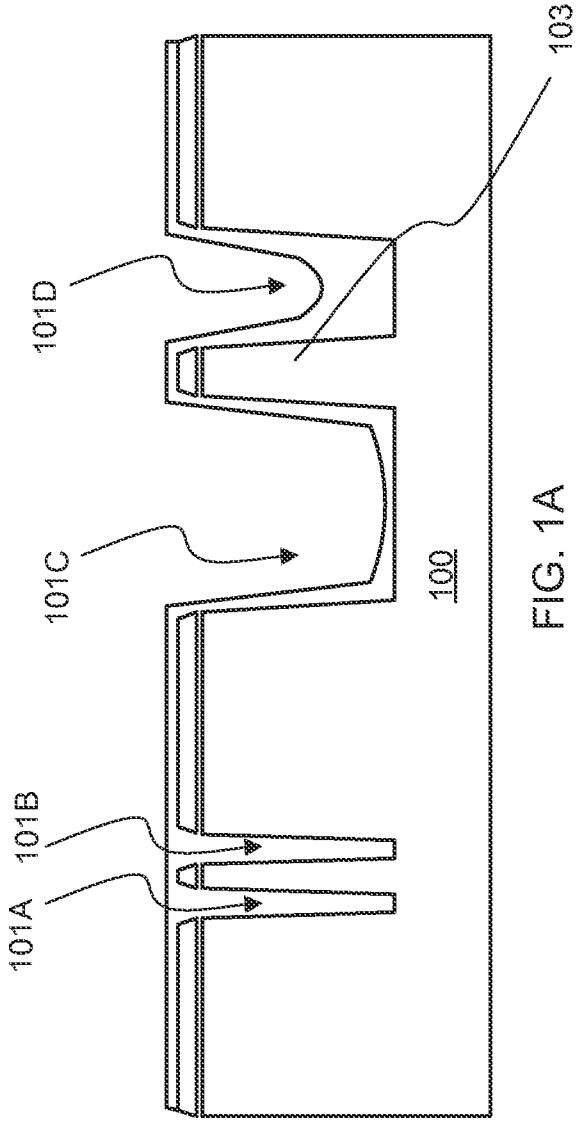

FIG. 1A

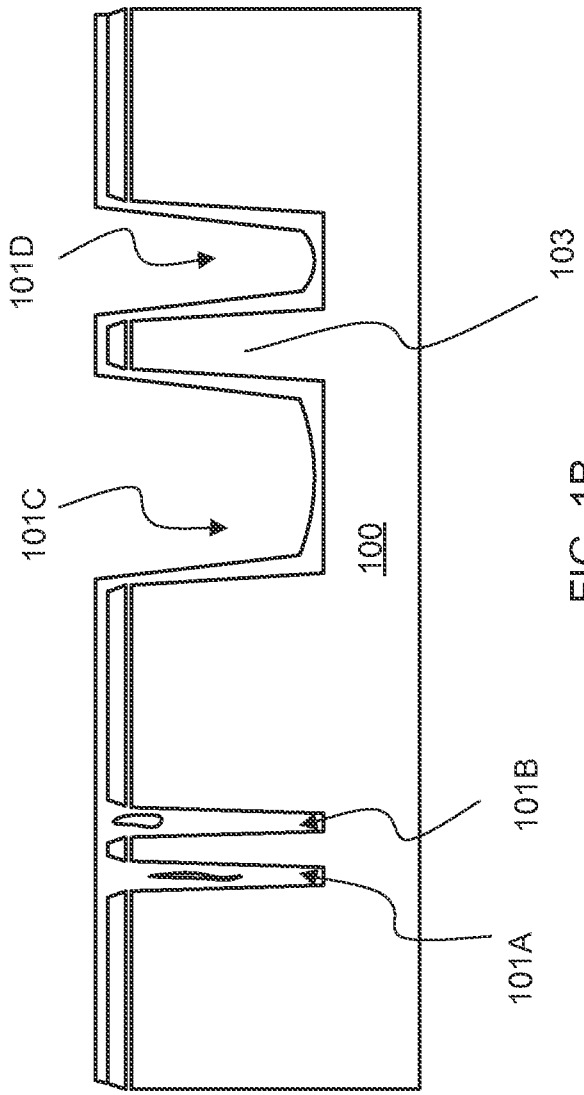

FIG. 1B

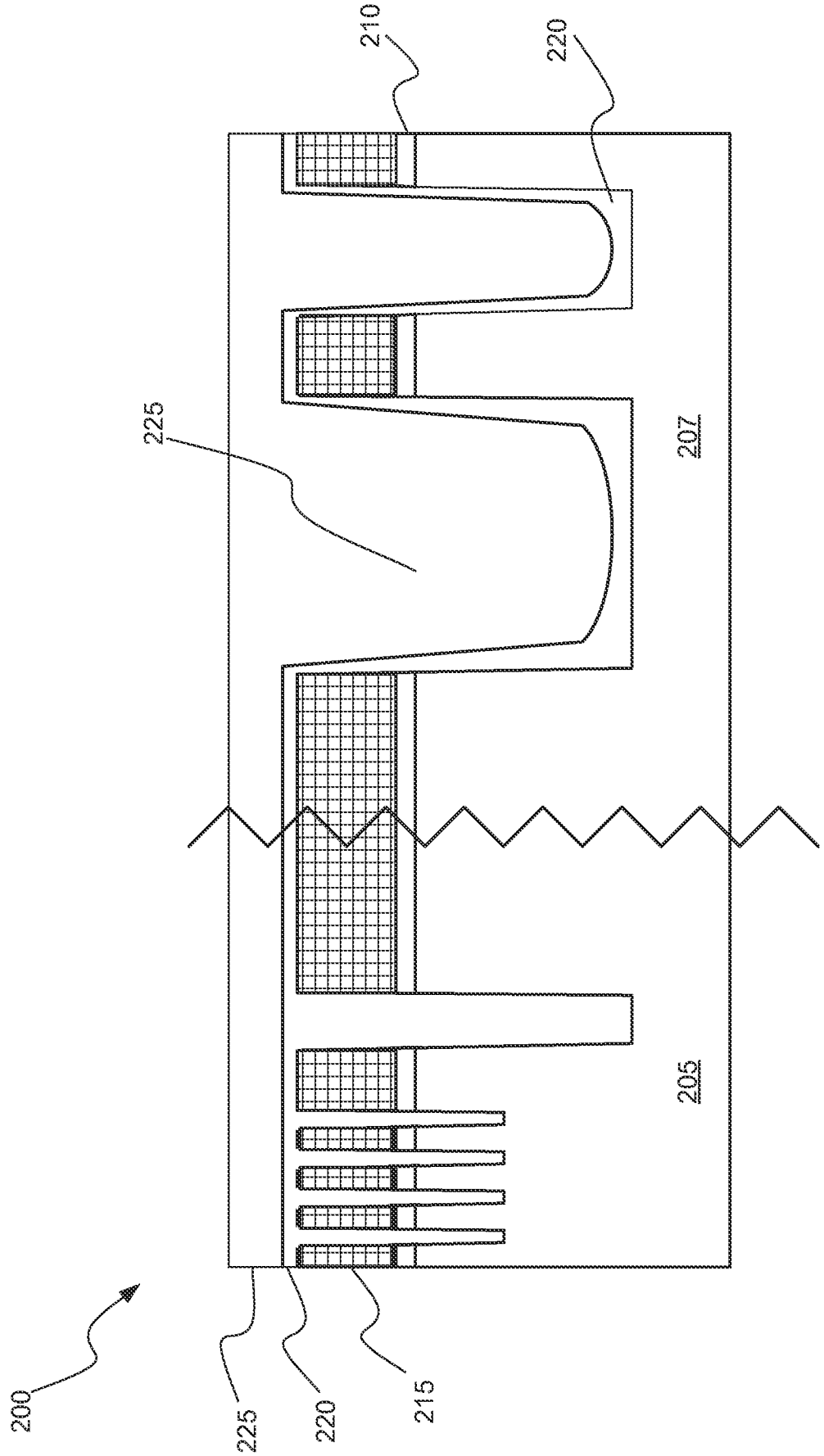

FIG. 2

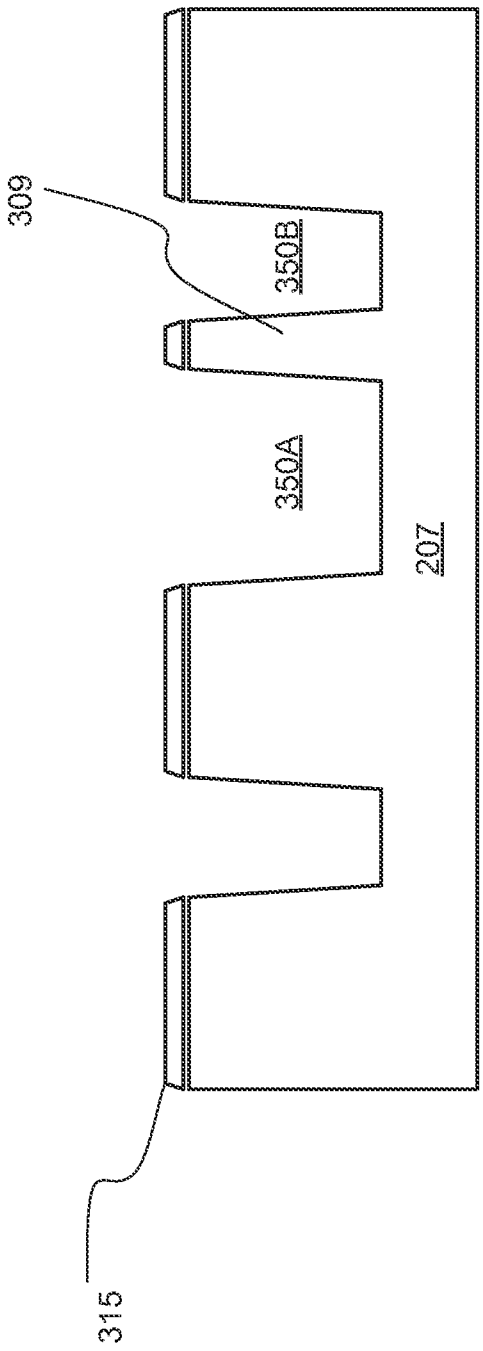

FIG. 3

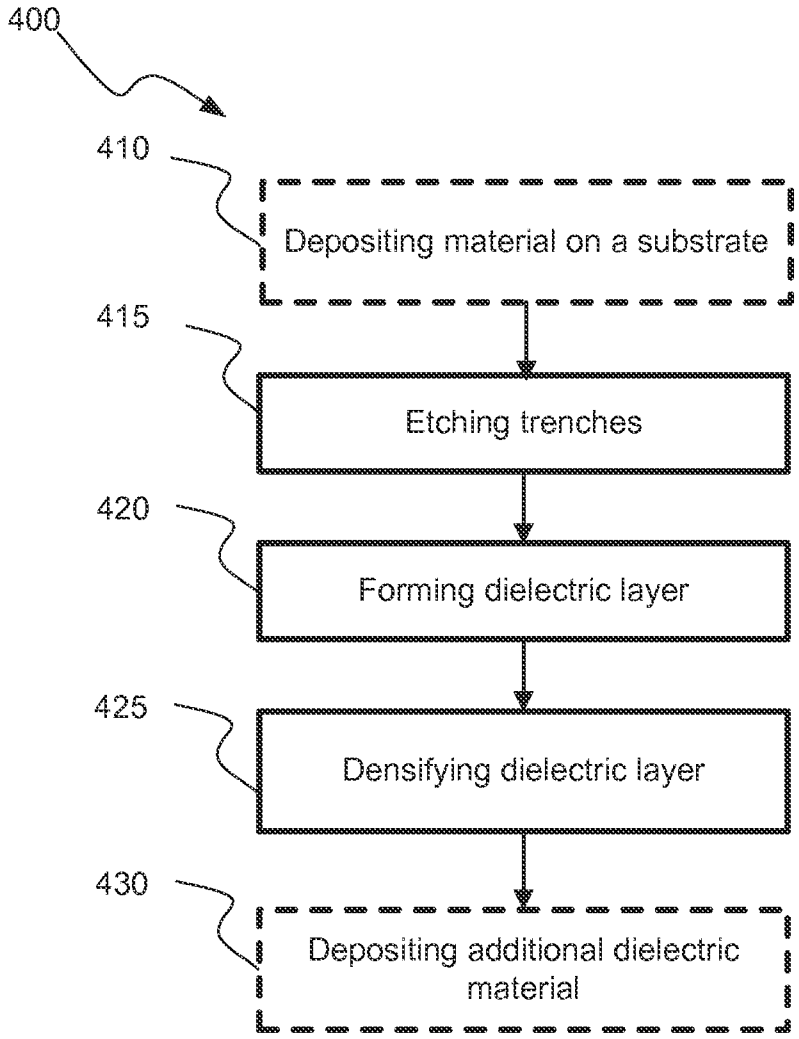
400
410
Depositing material on a substrate
415
Etching trenches
420
Forming dielectric layer
425
Densifying dielectric layer
430
Depositing additional dielectric material

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/061726

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/31(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/31; H01L 21/324; H01L 21/316; H01L 21/76; H01L 21/265

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: dislocation, gapfill, annealing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 09-205140 A (TOSHIBA CORP) 05 August 1997 See the entire document.	1-14
A	KR 10-2010-0074508 A (DONGBU HITEK CO. , LTD.) 02 July 2010 See the entire document.	1-14
A	KR 10-2001-0058774 A (HYNIX SEMICONDUCTOR INC.) 06 July 2001 See the entire document.	1-14
A	KR 10-2004-0096365 A (HYNIX SEMICONDUCTOR INC.) 16 November 2004 See the entire document.	1-14

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 MARCH 2013 (21 .03.2013)	**21 MARCH 2013 (21.03.2013)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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