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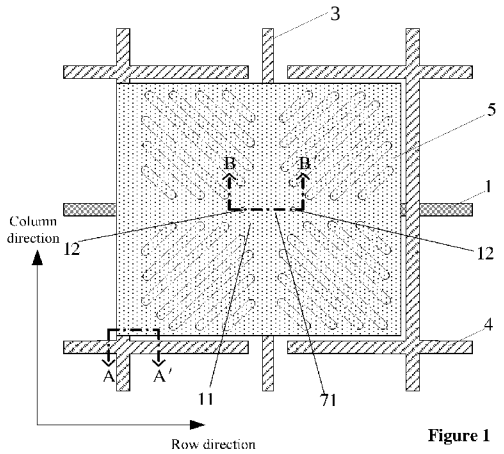

Figure 1

(57) Abstract: The present disclosure provides an array substrate. The array substrate includes a substrate (8) having a display region with a plurality of pixel regions, each pixel region having two or more first regions; a common electrode line (4) between two adjacent pixel regions; a gate line (1); a data line (3) intersecting with the gate line (1); at least one of the gate line (1) and the data line (3) being in a second region between two adjacent first regions; and a pixel electrode having a hollowed-out pattern within a corresponding first region, pixel electrodes corresponding to the two or more first regions being a pixel electrode unit (5).

WO 2017/059825 A1

ARRAY SUBSTRATE AND SEMICONDUCTOR DEVICE CONTAINING THE SAME, AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCES TO RELATED APPLICATIONS

[001] This PCT patent application claims priority of Chinese Patent Application No. 201510654443.7, filed on October 10, 2015, the entire content of which is incorporated by reference herein.

TECHNICAL FIELD

[002] The present invention generally relates to the display technologies and, more particularly, relates to an array substrate, a semiconductor device containing the array substrate, and a method for fabricating the array substrate.

BACKGROUND

[003] A transparent thin film transistor-liquid crystal display (TFT-LCD) panel is a display panel with high light transmission rate and is capable of displaying the objects behind the displayed images. Transparent TFT-LCD panels can be used as the TFT-LCD panels for many show windows, e.g., in buildings, bus stops, and shops. Besides the display functions, transparent TFT-LCD panels can also be used to provide desired information. Thus, transparent TFT-LCD panels have drawn much attention in the display market. The transparent TFT-LCD panels will likely occupy display markets in buildings, billboards, public places, etc. The development of transparent TFT-LCD panels can help the development of the entire market of TFT-LCD panels.

BRIEF SUMMARY

[004] The present disclosure provides an array substrate, a semiconductor device containing the array substrate, and a method for fabricating the array substrate. The transparent TFT-LCD panel containing the array substrate may have improved light transmission rate.

[005] One aspect of the present disclosure includes an array substrate, including: a substrate having a display region with a plurality of pixel regions, each pixel region having two or more first regions; a common electrode line between two adjacent pixel regions; a gate line; a

data line intersecting with the gate line; at least one of the gate line and the data line being in a second region between two adjacent first regions; and a pixel electrode having a hollowed-out pattern within a corresponding first region, pixel electrodes corresponding to the two or more first regions being a pixel electrode unit.

[006] Optionally, each pixel electrode corresponds to a first region, and an area of the pixel electrode corresponds to an area of the first region.

[007] Optionally, the array substrate further includes a first insulating layer being between the gate line and the data line; and a second insulating layer being between the data line and the pixel electrode unit.

[008] Optionally, a pixel region includes four first regions arranged in a two by two configuration; and the gate line and the data line are in the second region being perpendicular to each other.

[009] Optionally, hollowed-out patterns of two adjacent pixel electrodes are axisymmetric.

[0010] Optionally, the hollowed-out pattern includes one or more of slit shapes and stripe shapes.

[0011] Optionally, the array substrate further includes a thin-film transistor, the thin-film transistor including a gate electrode being integrated with the gate line; first electrodes being electrically connected to the pixel electrode; a second electrode being integrated with the data line; an active layer being electrically connected to the first electrodes and the second electrode. The data line, the common electrode line, and first electrodes are over the gate electrode, the data line, the common electrode line, and the first electrodes being separated from the gate electrode by a first insulating layer; the gate electrode and the gate line are on the substrate; the active layer is on the gate electrode and is separated from the gate electrode by the first insulating layer, the active layer being electrically connected with the first electrodes and the second electrode; the second electrode of and the data line are one piece; and the pixel electrode unit is over the data line, the pixel electrode unit being connected to the first electrodes through first via holes, the first via holes being through the second insulating layer.

[0012] Optionally, the array substrate further includes a third insulating layer being between the second insulating layer and the pixel electrode; a first via holes being through the second

insulating layer and the third insulating layer. The pixel electrode being connected to the first electrodes through the first via hole.

[0013] Optionally, the third insulating layer is made of an organic insulating material.

[0014] Optionally, the array substrate according further includes a storage electrode formed in areas corresponding to the common electrode line. The first insulating layer is between the storage electrode and the common electrode line; and the storage electrode is electrically connected to the pixel electrode and forms a storage capacitor structure with the common electrode line.

[0015] Optionally, the storage electrode is integrated with the gate line.

[0016] Optionally, at least one common electrode line substantially overlaps with the pixel electrode; and the second insulating layer is between the common electrode line and the pixel electrode.

[0017] Optionally, the pixel electrode is of a squared shape.

[0018] Another aspect of the present disclosure provides a semiconductor device, including a disclosed array substrate.

[0019] Optionally, the semiconductor device further includes a cover substrate with a clear region corresponding to the pixel electrode for improving light transmittance.

[0020] Another aspect of the present disclosure provides a method for fabricating an array substrate, including providing a substrate having a display region with a plurality of pixel regions, each pixel region having two or more first regions, and a second region between two adjacent first regions; forming a gate line and a gate electrode of a thin-film transistor on a substrate, the gate line and the gate electrode of the thin-film transistor being formed in a same fabrication step; and forming a first insulating layer; forming an active layer of the thin-film transistor, the active layer being located in an area where the gate line and a data line intersect. The method further includes forming a data line, common electrode lines between two adjacent pixel regions, first electrodes, and a second electrode, at least one of the gate line and the data line being formed in the second region; forming a second insulating layer and first via holes, the first via holes being through the second insulating layer; and forming a pixel electrode with a hollowed-out pattern in the pixel region being connected to the first electrodes through the first via holes, the hollowed-out pattern corresponding to the first region.

[0021] Optionally, the hollowed-out pattern having one or more of slit shapes and stripe shapes; each pixel region includes four first regions arranged in a two by two configuration; and the gate line and the data line being perpendicular to each other are fabricated in the second region.

[0022] Optionally, the method further includes forming a third insulating layer on the second insulating layer, the first via holes being through the third insulating layer and the second insulating layer.

[0023] Optionally, the method further includes forming storage electrodes in areas corresponding to the common electrode lines, the storage electrodes and the gate line being formed in a same fabrication step; and forming second via holes in areas corresponding to the storage electrodes, the second via holes and the second insulating layer being formed in a same fabrication step, the second via holes being through the first insulating layer and the second insulating layer, and the pixel electrode being connected to the storage electrodes through the second via holes.

[0024] Optionally, the pixel electrode unit overlaps with at least one common electrode line.

[0025] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present disclosure.

[0027] Figure 1 illustrates a top view of an exemplary array substrate according to various disclosed embodiments of the present disclosure;

[0028] Figure 2 illustrates cross-sectional views along the A-A' direction and the B-B' direction depicted in Figure 1;

[0029] Figure 3 illustrates a top view of another exemplary array substrate according to various disclosed embodiments of the present disclosure;

[0030] Figure 4 illustrates cross-sectional views along the A-A" direction and the B-B" direction depicted in Figure 3;

[0031] Figure 5 illustrates an exemplary process flow for fabricating an exemplary array substrate according to various disclosed embodiments of the present disclosure; and

[0032] Figures 6-11 illustrates top views of certain parts of an array substrate at certain stages of an exemplary fabrication step.

DETAILED DESCRIPTION

[0033] For those skilled in the art to better understand the technical solution of the invention, reference will now be made in detail to exemplary embodiments of the invention, which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0034] The most prominent feature of a transparent TFT-LCD device/panel is its transparency. However, transparency results from the perception that the human eyes provide to the brain, and the perception mainly comes from the brightness of the objects behind the transparent TFT-LCD devices. Thus, in conventional transparent TFT-LCD devices, high-power illuminating devices are often mounted behind the TFT-LCD devices as the backlight, which make the TFT-LCD devices power-consuming. Transparent TFT-LCD devices without backlight consume less power, but the light transmission rate in such a LCD panel may be undesirably low. As a result, without backlight, the transparency of a TFT-LCD device is impaired.

[0035] One method to improve the transparency of a TFT-LCD device is to remove the color filters (e.g., red, green, and blue, or RGB) and form black-and-white transparent display panels. Often, after the RGB color filters are removed, the light transmission rate of an LCD panel can be increased from about 5.9% to about 22%. The method of removing the color filters can greatly improve the transparent display of a transparent TFT-LCD device without using a backlight. However, the light transmission rate of a transparent TFT-LCD device needs to be further improved.

[0036] In embodiments of the present disclosure, in a pixel region of an array substrate, at least one of the gate line and the data line is formed in the dark region between the pixel-domain regions. As a result, the gate lines and the data lines may have less impact on the aperture ratio of the array substrate. Thus, the light transmission rate of the transparent TFT-LCD panel may be further improved.

[0037] One aspect of the present disclosure provides an array substrate.

[0038] To form the disclosed array substrate, gate lines, data lines, and common electrode lines may be formed on a substrate. The common electrode lines may divide the display region of the array substrate to a plurality of pixel regions. A common electrode line may be between two adjacent pixel regions. Each pixel region may be disposed with a pixel electrode unit. A pixel region may include at least two first regions. Each first region may correspond to a pixel electrode. The pixel electrodes corresponding to the at least two first regions may form a pixel electrode unit. A first region may be, e.g., a pixel-domain region. A pixel electrode may contain a hollowed-out pattern where the pixel electrode and a corresponding first regions overlap. A pixel electrode may have a hollowed-out pattern within the corresponding first regions. An area of the pixel electrode may correspond to an area of the first region. The hollowed-out pattern may be of suitable shapes, e.g., a plurality of hollowed-out stripes or slits. Gate lines and data lines may intersect, i.e., not being aligned in parallel. When displaying images, a second region may be formed between first regions in the described multiple-domain pixel electrode. A second region may be, e.g., a dark region. For example, a second region may be formed between two adjacent first regions in a multiple-domain pixel electrode. In one embodiment, to improve light transmission rate, at least one of a gate line and a data line in a pixel region may be arranged or formed in a second region between the first regions. A TFT may be formed at the intersection of a gate line and a data line. The TFT may be electrically connected to the gate line, the data line, and the pixel electrode. A first insulating layer may be formed between the gate line and the data line. A second insulating layer may be formed between the data line and the pixel electrode.

[0039] In the present disclosure, a pixel electrode unit refers to a continuous piece of pixel electrode material. It is merely for illustrative purposes to describe a pixel electrode unit as a plurality of pixel electrodes, each corresponding to a first region. It should also be noted that, an intersection between two lines, e.g., a gate line and a data line, merely indicates that the two lines are not parallel with each other. That is, the projections of the two lines on the substrate may intersect. The term "intersect" or "intersection" do no indicate any physical or electrical connection between the two lines. In addition, to "correspond" to an object or a location may be used to describe the correspondence relationship between the physical locations of two or more objects. For example, the two or more objects may have the same location or sufficiently close locations.

[0040] In the present disclosure, a plurality of pixel regions may be formed by the common electrode lines. Each pixel region may include at least two first regions. At least one of a gate line and a data line in a pixel region may be arranged in an obscure area or a second region between first regions. By this arrangement, the gate lines and the data lines would thus have less impact on the aperture ratio of the array substrate, and the light transmission rate of the transparent TFT-LCD panel may be improved.

[0041] In one embodiment, a pixel region may include two first regions. One second region may be formed between the two first regions. One of a gate line and a data line may be arranged in the second region. For example, the gate line may be arranged in the second region. The gate line may be arranged to be perpendicular to the data line, and the common electrode line may be arranged to be parallel to the data line. Also, the data line may be arranged in the second region. The data line may be arranged to be perpendicular to the gate line in the corresponding second region, and the common electrode line may be arranged to be parallel to the gate line.

[0042] In another embodiment, a pixel region may include four first regions. The pixel electrode unit in the pixel region may include four pixel electrodes, each corresponding to a first region. The configuration of the array substrate may be shown in Figures 1-4. Figure 1 is a top view of an exemplary array substrate. Figure 2 illustrates the cross-sectional views of the array substrate along the A-A' direction and the B-B' direction shown in Figure 1. Figure 3 is a top view of another exemplary array substrate. Figure 4 illustrates the cross-sectional views of the array substrate along the A-A" direction and the B-B" direction shown in Figure 3. For illustrate purposes, only one pixel region is shown in Figures 1-4.

[0043] The array substrate may include a substrate 8. A gate line 1, a data line 3, and common electrode lines 4 may be formed on the substrate 8. The common electrode lines 4 may divide the display region of the array substrate into a plurality of pixel regions. A pixel region may include four first regions arranged in two rows and two columns, i.e., two by two configuration, as shown in Figures 1 and 3. Two adjacent pixel electrodes in the pixel electrode unit may contain hollowed-out patterns of different directions. For example, the two adjacent pixel electrodes along the column direction or along the row direction may contain hollowed-out patterns of different directions.

[0044] The gate line 1 and the data line 3 may be arranged to be perpendicular to each other. In the multiple-domain pixel electrode unit, a second region may be formed between two

adjacent first regions. For example, for the two by two configuration depicted in Figures 1 and 3, two adjacent first regions may form a second region along the column direction, and two adjacent first regions may form a second region along the row direction. Thus, two second regions may be formed in the pixel region, one along the row direction and the other one along the column direction.

[0045] In some embodiments, to improve light transmission rate, the gate line 1 and the data line 3 may be formed or arranged in the second regions between first regions. For example, as shown in Figures 1 and 3, the gate line 1 may be formed in the second region along the row direction, and the data line 3 may be formed in the second region along the column direction. A TFT may be formed at the intersection of the gate line 1 and the data line 3, indicated by the dashed circles in Figures 2 and 4. The TFT may be connected to the gate line 1, the data line 3, and the pixel electrode unit 5. The first insulating layer 9 may be disposed between the gate line 1 and the data line 3. The second insulating layer 10 may be disposed between the data line 3 and the pixel electrode unit 5. For a TFT, as shown in Figures 2 and 4, any connection between a part and the pixel electrode unit 5 may be between the part and the pixel electrode corresponding to the TFT.

[0046] In the embodiments illustrated in Figures 1-4, the common electrode lines 4 may divide the display region of the array substrate to a plurality of pixel regions. Each pixel region may include four first regions arranged in two rows and two columns. The gate line 1 and the data line 3 may be formed in the second regions between adjacent first regions. Thus the gate line 1 and the data lien 3 may have less impact on the aperture ratio of the array substrate, and the light transmission rate of the transparent TFT-LCD may be improved.

[0047] Further, the hollowed-out patterns of a pixel electrode unit 5, as shown in Figures 1 and 3, may be symmetrical or axisymmetric with respect to the corresponding second region. For example, two hollow-patterns arranged along the column direction or row direction may be axisymmetric with respect to the second region in between. Thus, when displaying images, the electric field formed between each pixel electrode in a pixel electrode unit, i.e., corresponding to each first region, and the common electrodes may be uniform.

[0048] The array substrate provided by the present disclosure is now illustrated in detail using bottom-gated TFTs. For illustrative purposes, only one pixel is described in an embodiment. It should be noted that, for a top-gated TFT, the display region of the array substrate may also be divided into a plurality of pixel regions by the common electrode lines,

and the electrode structure described in relation to the bottom-gated TFTs may also be applied to the top-gated TFTs.

[0049] As shown in Figures 2 and 4, a gate line 1 may be formed on the substrate 8. A data line 3, a common electrode line 4, and first electrodes 72 of a TFT may be formed through a same fabrication process, located over the gate line 1, and separated from the gate line 1 by a first insulating layer 9. The gate electrode 11 (not shown in Figures 2 and 4) of the TFT may be integrated with the gate linel as one piece or be formed through a same fabrication step. The active layer 71 of the TFT may be formed on the gate electrode 11 of the TFT and may be separated from the gate electrode 11 by the first insulating layer 9, i.e., the gate insulating layer. The active layer 71 of the TFT may be electrically connected with the first electrodes 72 of the TFT and a second electrode of the TFT. The second electrode of the TFT (not shown in Figures 2 and 4) may be integrated with the data line 3 as one piece or be formed through a same fabrication step. The data line 3 may be formed on the active layer 71. The pixel electrode unit 5 may be formed over the data line 3. The pixel electrode unit 5 may be connected to the first electrodes 72 of the TFT through via holes 12. The first via holes 12 may be through a second insulating layer 10.

[0050] As shown in Figures 2 and 4, a third insulating layer 13 may be formed between the second insulating layer 10 and the pixel electrode unit 5. The pixel electrode unit 5 may be connected with the first electrodes 72 of the TFT through the via holes 12. The via holes 12 may be through the second insulating layer 10 and the third insulating layer 13. The third insulating layer 13 may increase the thickness of the insulating material between the pixel electrode unit 5 and the data line 3 to minimize parasitic capacitance. Crosstalk during display may be reduced. The third insulating layer 13 may be made of an organic insulating material. It can be easy to form the organic insulating material that is desirably thick, to increase the distance between the pixel electrode unit 5 and the data line 3.

[0051] A storage capacitor structure may also be formed in a pixel electrode. Figures 1 and 2 illustrate an exemplary storage capacitor structure. As shown in Figures 1 and 2, the pixel electrode unit 5 and the common electrode line 4 may share an overlapped area. In the overlapped area, the pixel electrode unit 5 and the common electrode line 4 may be separated by the second insulating layer 10 and the third insulating layer 13. Thus, a storage capacitor structure may be formed between the pixel electrode unit 5 and the common electrode line 4. It should be noted that, in the present disclosure, for illustrative purposes, the pixel electrode

unit 5 may overlap with one common electrode line 4. In certain other embodiments, the pixel electrode unit 5 may also overlap with more than one common electrode lines 4.

[0052] Figures 3 and 4 illustrate another exemplary storage capacitor structure. As shown in Figures 3 and 4, the array substrate may further include storage electrodes 2. A storage electrode 2 may be formed where a common electrode line 4 is formed. That is, a storage electrode 2 and a common electrode line 4 may substantially overlap. The first insulating layer 9 may be formed between the storage electrode 2 and the common electrode line 4. The storage electrode 2 may be electrically connected to the pixel electrode unit 5 through a second via hole 6. A second via hole 6 may be through the second insulating layer 10 and the third insulating layer 13. A storage capacitor structure may be formed between a storage electrode 2 and a common electrode line 4.

[0053] To reduce fabrication steps, the storage electrodes 2 may be integrated with the gate line 1, and the storage electrodes 2 and the gate line 1 may be formed through a same fabrication step.

[0054] For the disclosed array substrate, no color filters need to be formed. Thus, subpixel structures need not be formed. The pixel electrode unit 5 may have a squared shape. The pixel electrode unit 5 may contain hollowed-out patterns, which may have suitable shapes such as slits or stripes.

[0055] Another aspect of the present disclosure provides a semiconductor device.

[0056] The semiconductor device may include one or more of the disclosed array substrates, one or more of cover substrates to be aligned and bonded with the array substrates, and a liquid crystal layer between an array substrate and a cover substrate. An alignment layer may be formed on each of the array substrates and a corresponding cover substrate. The pattern of the alignment layer on the array substrate and the pattern of the alignment layer on the cover substrate may be perpendicular to each other. The perpendicular configuration of the patterns of the alignment layer may enable the second regions formed by the alignment layers to have an orthogonal configuration in the plane the alignment layers are located. The second regions formed by the alignment layers may overlap with the second regions formed by the first regions. That is, the pattern of the alignment layer on the array substrate and the pattern of the alignment layer on the cover substrate may overlap and form second regions, and the orthogonal configuration of the alignment layers may form second regions with an orthogonal configuration. Thus, the second regions formed by the alignment layers may have reduced

impact on the light transmission rate of the semiconductor device. In some embodiments, the semiconductor device may be a display apparatus.

[0057] The regions on a cover substrate that correspond to or face the pixel electrode units of an array substrate may be clear, colorless and transparent to improve light transmittance. Thus, light transmission rate may be further improved.

[0058] The semiconductor device may be operated under advanced super dimension switch (ADS) mode or under twisted nematic (TN) mode. When operated under the ADS mode, common electrodes may be formed on the array substrate and may be connected with the common electrode lines. When operated under the TN mode, common electrodes may be formed on the cover substrate. In this case, the common electrodes may be connected to the common electrode lines, which are formed on the array substrate, after the cover substrate is bonded with the array substrate.

[0059] Another aspect of the present disclosure provides a method for fabricating the array substrate. Figure 5 illustrates an exemplary process flow of the method. The method may include steps S510-S550. For illustrative purposes, steps S510-S550 only describe the formation of one pixel structure.

[0060] In step S510, a gate line may be formed on the substrate. The gate electrode of the subsequently-formed TFT may be formed together with the gate line as one pattern.

[0061] In step S520, a first insulating layer and an active layer of the subsequently-formed TFT may be formed sequentially. The active layer may be located in the area where the gate line and the subsequently-formed data line overlap or intersect.

[0062] In step S530, a data line, common electrode lines, first electrodes of the TFT, and a second electrode of the TFT may be formed. The common electrode lines in the array substrate may divide the display region of the array substrate into a plurality of pixel regions. A pixel region may include at least two first regions. In a pixel region, the data line and the gate line may intersect. At least one of the gate line and the data line may be formed in a second region formed between the first regions.

[0063] In step S540, a second insulating layer and first via holes through the second insulating layer may be formed.

[0064] In step S550, a pixel electrode unit may be formed in a pixel region. A pixel electrode unit may include a plurality of pixel electrodes, each corresponding to a first region.

Each pixel electrode may contain a hollowed-out pattern. The pixel electrode unit may be connected to the first electrodes of the TFT through the first via holes. The hollowed-out pattern may be of any suitable shapes such as stripes and slits.

[0065] Details of the fabrication step to form the array substrates shown in Figures 1-4 are further exemplified in Figures 6-11. Figure 6 illustrates an exemplary process to form the gate line and the gate electrode of the TFT. Figure 7 illustrates an exemplary process to form the first insulating layer and the active layer over the gate electrode depicted in Figure 6. Figure 8 illustrates an exemplary process to form the data line, the common electrode lines, and the first electrodes of the TFT on the active layer depicted in Figure 7. Figure 9 illustrates an exemplary process to form the gate line and the gate electrode of the TFT, and the storage electrodes shown in Figure 3. Figure 10 illustrates an exemplary process to form the first insulating layer and the active layer over the gate line depicted in Figure 9. Figure 11 illustrates an exemplary process to form the data line, the common electrode lines, and the first electrodes of the TFT over the active layer depicted in Figure 10.

[0066] Figures 6-8 illustrate the top views of certain parts at certain stages of an exemplary fabrication step to form the pixel structure shown in Figures 1 and 2.

[0067] For example, at the beginning of the fabrication step, as shown in Figure 6, a gate line 1 and a gate electrode 11 of the subsequently-formed TFT may be formed on the substrate 8. For viewing simplicity, the substrate 8 is not shown in Figure 6.

[0068] Further, as shown in Figure 7, the first insulating layer (not shown) and the active layer 71 may be formed. The active layer 71 may be formed at the area where the gate line 1 and the subsequently-formed data line 3 intersect.

[0069] Further, as shown in Figure 8, the data line 3, the common electrode lines 4, and the first electrodes 72 of the subsequently-formed TFT in a pixel region may be formed. The common electrode lines 4 of the array substrate may divide the display region into a plurality of pixel regions. In a pixel region, the gate line 1 and the data line 3 may be perpendicular to each other. The gate line 1 and the data line 3 may be formed in the second regions between the subsequently-formed first regions. The two by two first regions may each correspond to a pixel electrode of the subsequently-formed pixel electrode unit.

[0070] Further, a second insulating layer and first via holes may be formed. The first via holes may be through the second insulating layer.

[0071] Further, the pixel electrode unit with four pixel electrodes, arranged in a two by two configuration, may be formed. Each pixel electrode may correspond to a first region. The pixel electrode unit may be connected to the first electrodes 72 of the TFT through the first via holes. Thus, a pixel structure shown in Figures 1 and 2 may be formed.

[0072] To reduce the crosstalk between the pixel electrode unit and the data line 3, after forming the second insulating layer and before forming the pixel electrode unit, a third insulating layer may be formed on the second insulating layer. The first via holes may be through the third insulating layer and the second insulating layer. In some embodiments, the third insulating layer may be made of an organic insulating material.

[0073] In some embodiments, to form a storage capacitor structure, when forming the pixel electrode unit, the pixel electrode unit and the common electrode line may overlap. The second insulating layer and the third insulating layer may be formed between the pixel electrode unit and the common electrode line such that the storage capacitor structure may be formed.

[0074] Figures 9-11 illustrate the top views of certain parts at certain stages of an exemplary fabrication step to form the pixel structure shown in Figures 3 and 4.

[0075] As shown in Figure 9, at the beginning of the fabrication step, when forming the gate line 1 on the substrate, a storage electrode 2 may be formed in the area a common electrode line 4 is subsequently-formed. In one embodiment, two storage electrodes 2 may be formed, as shown in Figure 9.

[0076] Further, as shown in Figure 10, the first insulating layer and the active layer 71 may be formed. The active layer 71 may be located at the area the gate line 1 and the subsequently-formed data line 3 intersect.

[0077] Further, as shown in Figure 11, the data line 3, the common electrode lines 4, and the first electrodes 72 of the TFT may be formed. The common electrode lines 4 of the array substrate may divide the display region of the array substrate into a plurality of pixel regions. In a pixel region, the gate line 1 and the data line 3 may be perpendicular to each other. The gate line 1 and the data line 3 may be formed in the second regions between the subsequently-formed first regions. The two by two first regions may each correspond to a pixel electrode of the subsequently-formed pixel electrode unit.

[0078] Further, when forming the second insulating layer, first via holes may be formed in the areas the first electrodes 72 are located. The first via holes may be through the second insulating layer to be connected with the first electrodes 72. Second via holes may be formed in the areas where the storage electrodes 2 are located. The second via holes may be through the first insulating layer and the second insulating layer. The subsequently-formed pixel electrode unit may be connected with the storage electrodes 2 through the second via holes. A storage electrode 2 and a common electrode line 4 may form a storage capacitor structure.

[0079] Further, the pixel electrode unit may be formed. The pixel electrode unit may include four pixel electrodes arranged in a two by two configuration. Each pixel electrode may correspond to a first region. The pixel electrode unit may be connected to the first electrodes 72 of the TFT through the first via holes, and may be connected to the storage electrode 2 through a second via hole. Thus, the pixel structure shown in Figures 3 and 4 may be formed.

[0080] To reduce the crosstalk between the pixel electrode unit and the data line 3, after forming the second insulating layer and before forming the pixel electrode unit, a third insulating layer may be formed on the second insulating layer. The first via holes may be through the third insulating layer and the second insulating layer. The second via holes may be through the third insulating layer, the second insulating layer, and the first insulating layer. In some embodiments, the third insulating layer may be made of an organic insulating material.

[0081] The disclosed array substrate and the fabrication method have several advantages. By optimizing the design of the pixels, at least one of the gate line and the data line is formed in the second region between the first regions in a pixel region. The gate line and the data line may have less impact on the aperture ratio of the array substrate, and the aperture ratio may thus be less impaired. The light transmission rate of the transparent TFT-LCD panel may be improved.

[0082] It should be understood that the above embodiments disclosed herein are exemplary only and not limiting the scope of this disclosure. Without departing from the spirit and scope of this invention, other modifications, equivalents, or improvements to the disclosed embodiments are obvious to those skilled in the art and are intended to be encompassed within the scope of the present disclosure.

What is claimed is:

1. An array substrate, comprising:

a substrate having a display region with a plurality of pixel regions, each pixel region having two or more first regions;

a common electrode line between two adjacent pixel regions;

a gate line;

a data line intersecting with the gate line;

at least one of the gate line and the data line being in a second region between two adjacent first regions; and

a pixel electrode having a hollowed-out pattern within a corresponding first region, pixel electrodes corresponding to the two or more first regions being a pixel electrode unit.

2. The array substrate according to claim 1, wherein:

each pixel electrode corresponds to a first region, and an area of the pixel electrode corresponds to an area of the first region.

3. The array substrate according to claim 1, further comprising:

a first insulating layer being between the gate line and the data line; and

a second insulating layer being between the data line and the pixel electrode unit.

4. The array substrate according to claim 1, wherein:

a pixel region includes four first regions arranged in a two by two configuration; and

the gate line and the data line are in the second region being perpendicular to each other.

5. The array substrate according to claim 4, wherein:

hollowed-out patterns of two adjacent pixel electrodes are axisymmetric.

6. The array substrate according to claim 1 or claim 4, wherein:

the hollowed-out pattern includes one or more of slit shapes and stripe shapes.

7. The array substrate according to claim 2, further comprising a thin-film transistor, the thin-film transistor comprising:

a gate electrode being integrated with the gate line;

first electrodes being electrically connected to the pixel electrode;

a second electrode being integrated with the data line;

an active layer being electrically connected to the first electrodes and the second electrode, wherein:

the data line, the common electrode line, and first electrodes are over the gate electrode, the data line, the common electrode line, and the first electrodes being separated from the gate electrode by a first insulating layer;

the gate electrode and the gate line are on the substrate;

the active layer is on the gate electrode and is separated from the gate electrode by the first insulating layer, the active layer being electrically connected with the first electrodes and the second electrode;

the second electrode of and the data line are one piece; and

the pixel electrode unit is over the data line, the pixel electrode unit being connected to the first electrodes through first via holes, the first via holes being through the second insulating layer.

8. The array substrate according to claim 7, further comprising:

a third insulating layer being between the second insulating layer and the pixel electrode;

a first via holes being through the second insulating layer and the third insulating layer, wherein:

the pixel electrode being connected to the first electrodes through the first via hole.

9. The array substrate according to claim 8, wherein the third insulating layer is made of an organic insulating material.

10. The array substrate according to claim 1, further comprising a storage electrode formed in areas corresponding to the common electrode line, wherein:

the first insulating layer is between the storage electrode and the common electrode line; and

the storage electrode is electrically connected to the pixel electrode and forms a storage capacitor structure with the common electrode line.

11. The array substrate according to claim 10, wherein: the storage electrode is integrated with the gate line.

12. The array substrate according to claim 11, wherein:

at least one common electrode line substantially overlaps with the pixel electrode; and

the second insulating layer is between the common electrode line and the pixel electrode.

13. The array substrate according to claim 1, wherein the pixel electrode is of a squared shape.

14. A semiconductor device, comprising the array substrate according to any one of claims 1-13.

15. The semiconductor device according to claim 14, further comprising:

a cover substrate with a clear region corresponding to the pixel electrode for improving light transmittance.

16. A method for fabricating an array substrate, comprising:

providing a substrate having a display region with a plurality of pixel regions, each pixel region having two or more first regions, and a second region between two adjacent first regions;

forming a gate line and a gate electrode of a thin-film transistor on a substrate, the gate line and the gate electrode of the thin-film transistor being formed in a same fabrication step;

forming a first insulating layer;

forming an active layer of the thin-film transistor, the active layer being located in an area where the gate line and a data line intersect;

forming a data line, common electrode lines between two adjacent pixel regions, first electrodes, and a second electrode, at least one of the gate line and the data line being formed in the second region;

forming a second insulating layer and first via holes, the first via holes being through

the second insulating layer; and

forming a pixel electrode with a hollowed-out pattern in the pixel region being connected to the first electrodes through the first via holes, the hollowed-out pattern corresponding to the first region.

17. The method according to claim 16, wherein:

the hollowed-out pattern having one or more of slit shapes and stripe shapes;

each pixel region includes four first regions arranged in a two by two configuration; and

the gate line and the data line being perpendicular to each other are fabricated in the second region.

18. The method according to claim 16, further comprising:

forming a third insulating layer on the second insulating layer, the first via holes being through the third insulating layer and the second insulating layer.

19. The method according to claim 16, further comprising:

forming storage electrodes in areas corresponding to the common electrode lines, the storage electrodes and the gate line being formed in a same fabrication step; and

forming second via holes in areas corresponding to the storage electrodes, the second via holes and the second insulating layer being formed in a same fabrication step, the second via holes being through the first insulating layer and the second insulating layer, and the pixel electrode being connected to the storage electrodes through the second via holes.

20. The method according to claim 16, wherein the pixel electrode unit overlaps with at least one common electrode line.

DRAWINGS

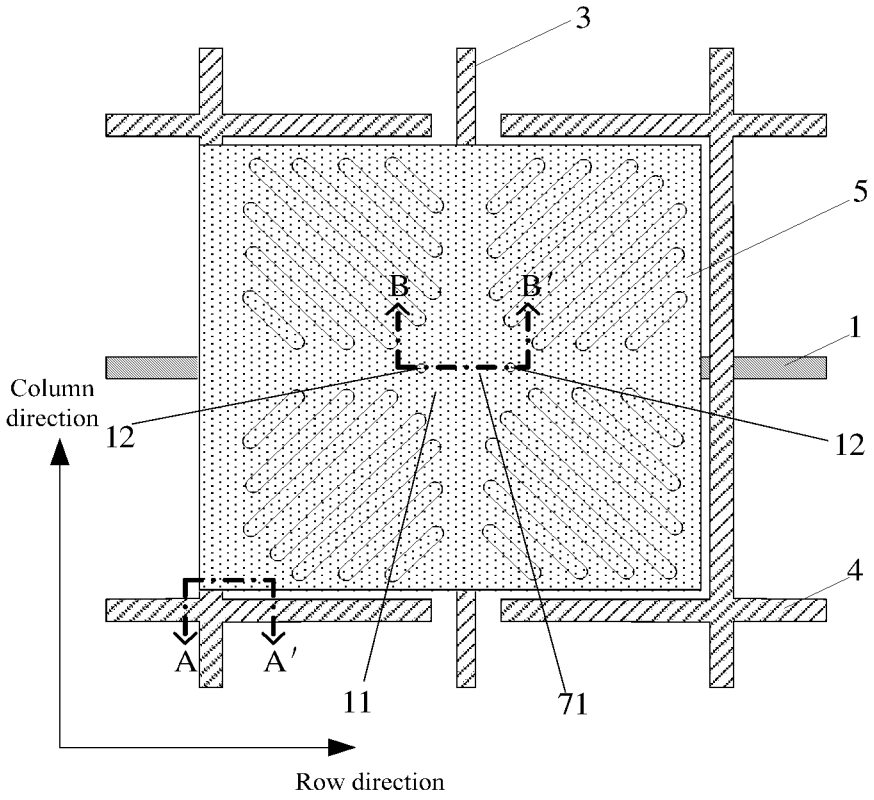

Figure 1

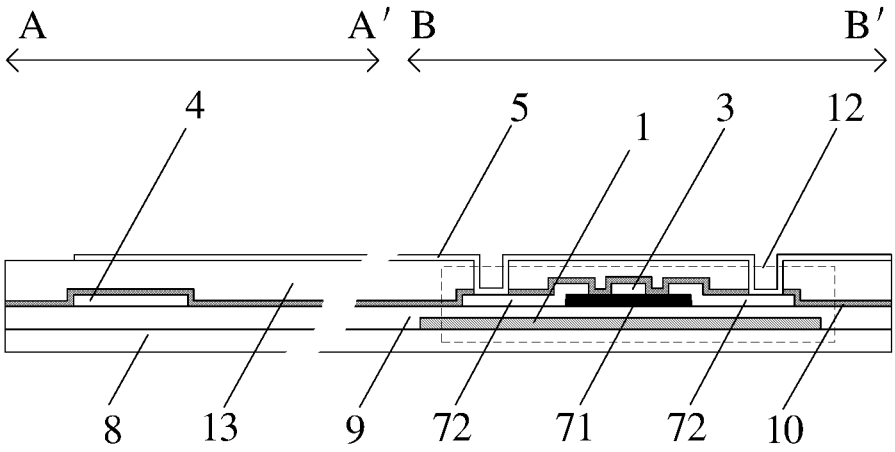

Figure 2

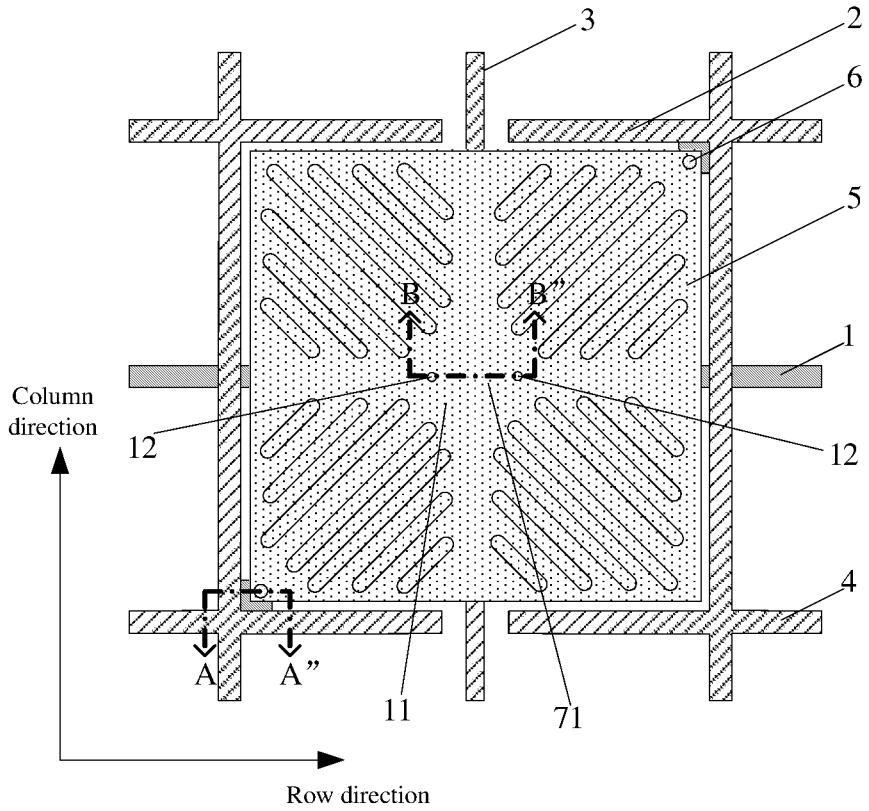

Figure 3

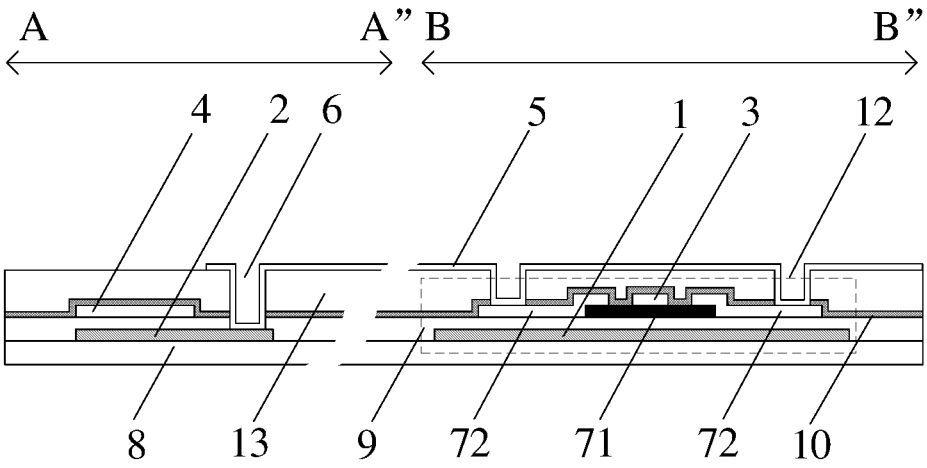

Figure 4

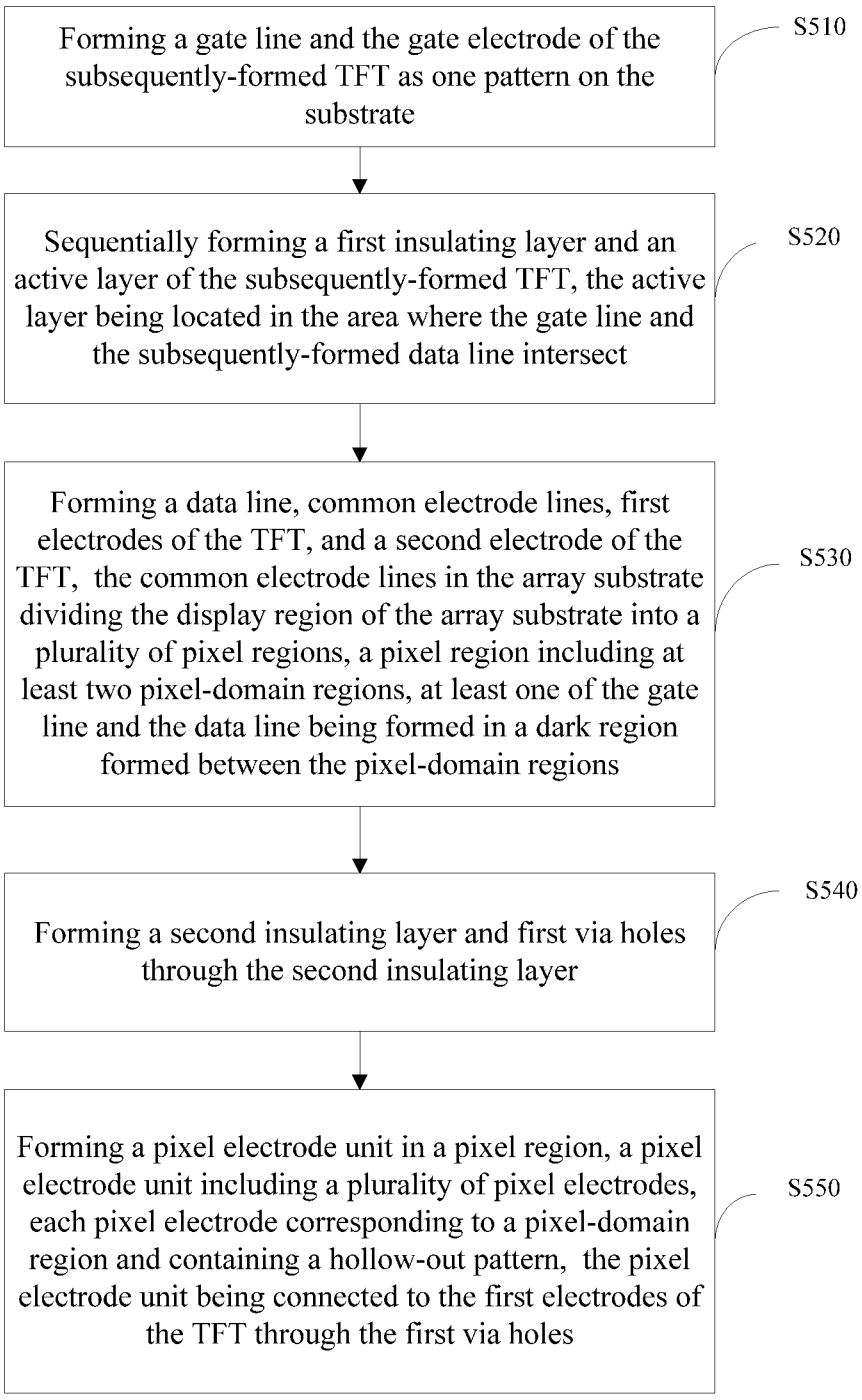
Forming a gate line and the gate electrode of the subsequently-formed TFT as one pattern on the substrate
S510
Sequentially forming a first insulating layer and an active layer of the subsequently-formed TFT, the active layer being located in the area where the gate line and the subsequently-formed data line intersect
S520
Forming a data line, common electrode lines, first electrodes of the TFT, and a second electrode of the TFT, the common electrode lines in the array substrate dividing the display region of the array substrate into a plurality of pixel regions, a pixel region including at least two pixel-domain regions, at least one of the gate line and the data line being formed in a dark region formed between the pixel-domain regions
S530
Forming a second insulating layer and first via holes through the second insulating layer
S540
Forming a pixel electrode unit in a pixel region, a pixel electrode unit including a plurality of pixel electrodes, each pixel electrode corresponding to a pixel-domain region and containing a hollow-out pattern, the pixel electrode unit being connected to the first electrodes of the TFT through the first via holes
S550

Figure 5

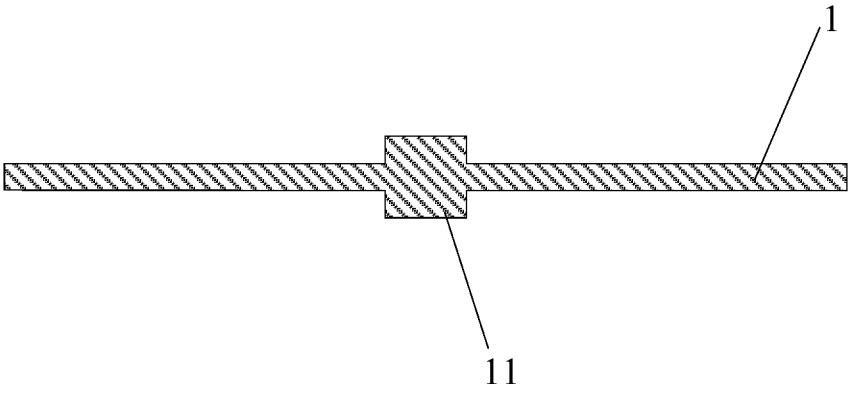

Figure 6

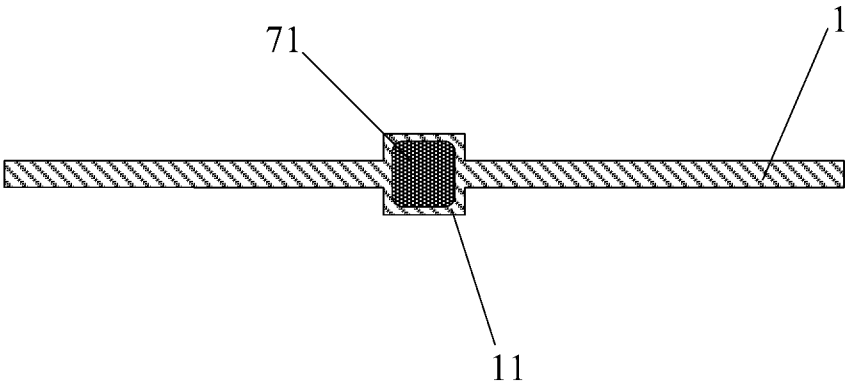

Figure 7

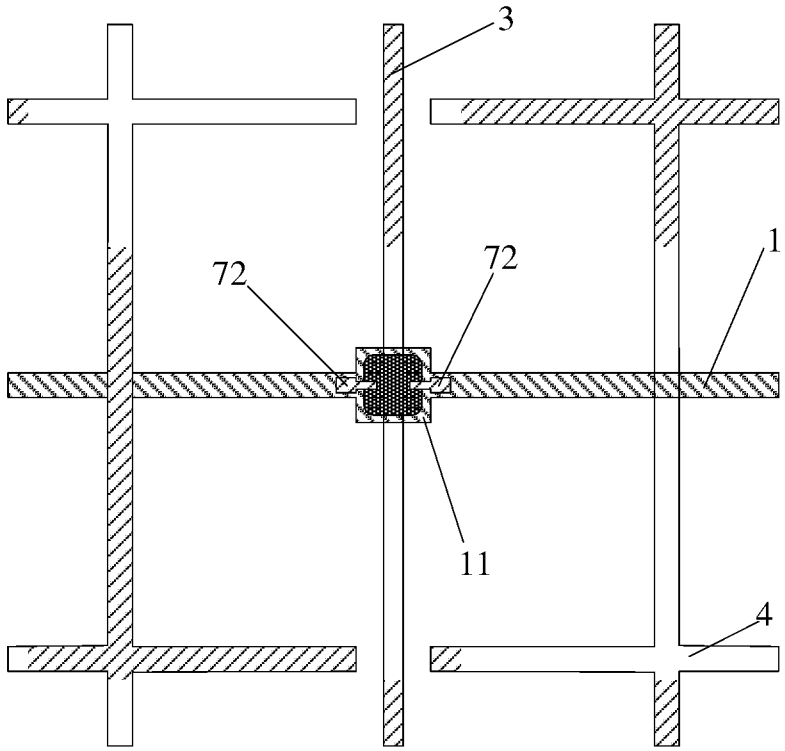

Figure 8

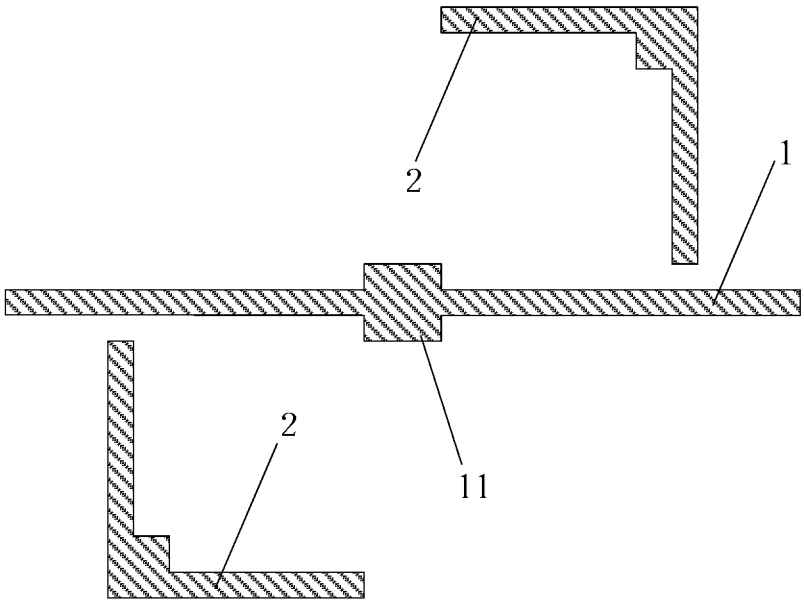

Figure 9

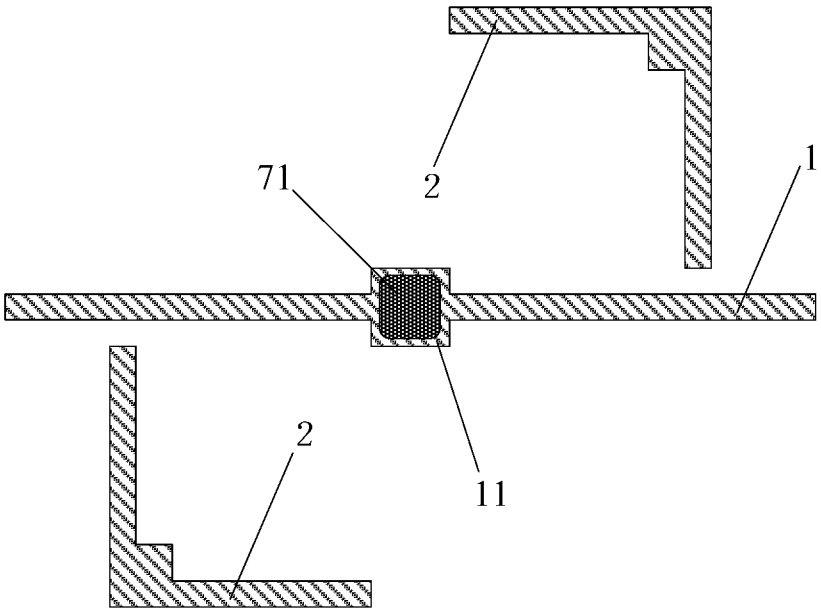

Figure 10

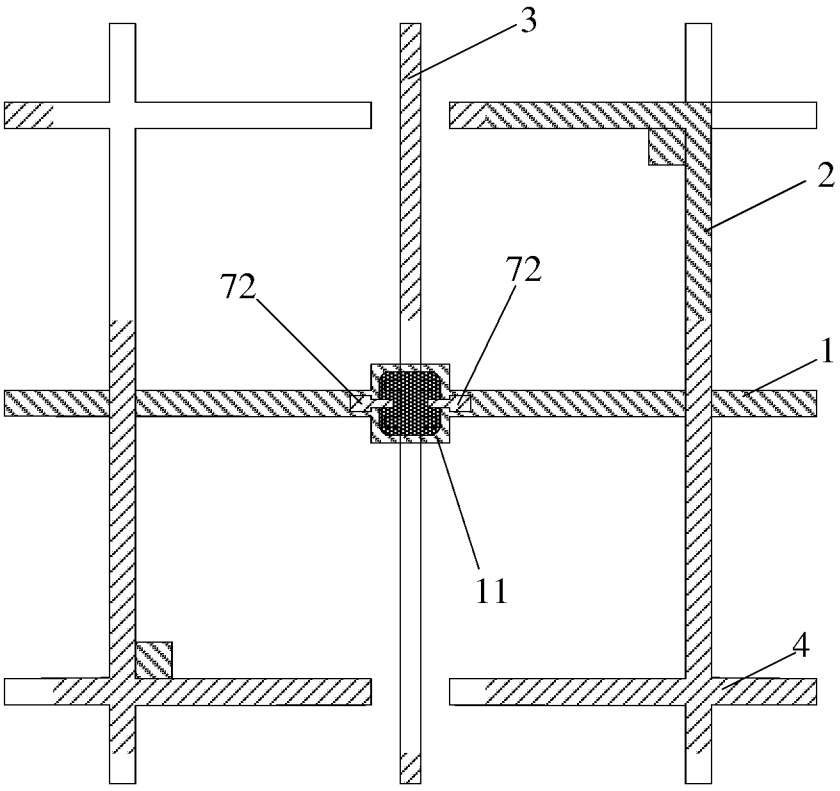

Figure 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/101692

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/1362(2006.01)i; G02F 1/1343(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,EPODOC,WPI,display+,liquid+,crys1al+,subs1rat+,region+,more,pixel+,electrod+,gate?,da1a?,line+,intersect+, cross+,perpendicul+,hollow+,TFT,thin?,film?,insulat+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CN 104049429 A (NANJING CEC-PANDA LCD TECHNOLOGY CO., LTD.) 17 September 2014 (2014-09-17) description, paragraphs [0046], [0048], [0058]-[0062] and figures 2-3, 5a-9b	1-20
Y	CN 103323988 A (BOE TECHNOLOGY GROUP CO., LTD. ET AL.) 25 September 2013 (2013-09-25) description, paragraphs [0020]-[0023] and figure 2	1-20
PX	CN 105223749 A (BOE TECHNOLOGY GROUP CO., LTD. ET AL.) 06 January 2016 (2016-01-06) description, paragraphs [0047]-[0082] and figures 1-11	1-20
PX	CN 205003420 U (BOE TECHNOLOGY GROUP CO., LTD. ET AL.) 27 January 2016 (2016-01-27) description, paragraphs [0037]-[0072] and figures 1-11	1-20
A	CN 104007591 A (NANJING CEC-PANDA LCD TECHNOLOGY CO., LTD.) 27 August 2014 (2014-08-27) the whole document	1-20

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2016	**30 December 2016**
Name and mailing address of the ISA/CN **STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer **SUN,Xin** Telephone No. **(86-10)61648461**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2016/101692

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002118330 A1 (LEE, YUN-BOK ET AL.) 29 August 2002 (2002-08-29) the whole document	1-20

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2016/101692

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
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