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(54) **Title:** LOW-POWER, HIGH-ACCURACY CURRENT REFERENCE FOR HIGHLY DISTRIBUTED CURRENT REFERENCES FOR CROSS POINT MEMORY

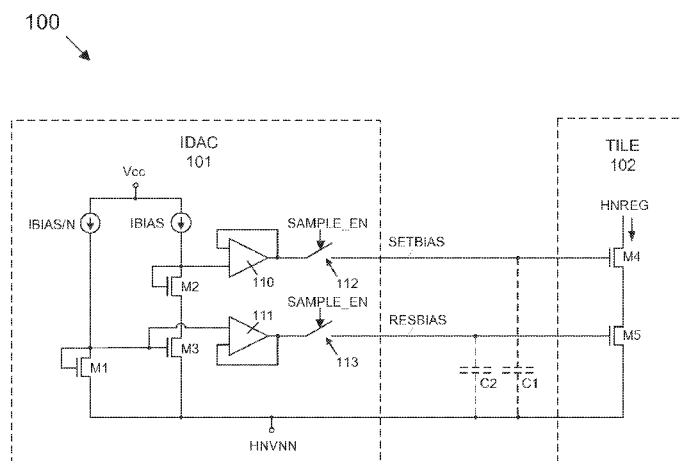


FIG. 1

(57) **Abstract:** A highly distributed current reference for a solid-state memory comprises a centrally located current digital-to-analog converter (IDAC) and a plurality of remotely located tile current references. The IDAC comprises a first active device that generates a reference current, and a device that forms a first source degeneration resistance for the first active device. The IDAC outputs a voltage signal that represents a magnitude of the reference current. A remotely located tile current reference comprises a second active device and a device that forms a second source degeneration resistance for the second active device. The source degeneration resistances and capacitance coupled to the voltage signal output from the IDAC compensate for current, temperature, supply and process variations.

LOW-POWER, HIGH-ACCURACY CURRENT REFERENCE FOR HIGHLY DISTRIBUTED CURRENT REFERENCES FOR CROSS POINT MEMORY

TECHNICAL FIELD

5 The subject matter disclosed herein relates to cross-point memories. More particularly, the subject matter disclosed herein relates to a low-power, high-accuracy current reference for highly distributed current reference for a solid-state memory, such as a cross-point memory.

BACKGROUND

10 A three-dimensional (3D) cross-point memory is a solid-state, non-volatile type of memory that for some memory operations requires delivery of accurate currents at many locations around a cross-point memory chip. For example, in one exemplary embodiment of a cross-point memory chip, over 8000 locations on the chip require an accurate low-power current
15 reference that can instantaneously deliver a reference current for a memory operation. Transferring a reference current from a central location to each of a plurality of current mirrors that are highly distributed across a chip has serious drawbacks in both power and chip-area use considerations. Another approach that has been used is to transfer a bias voltage that is remotely converted into a reference current at a plurality of locations. Such an approach presents
20 challenges because each separate current reference source must be calibrated to remove mismatches, such as random device offsets that can appear around a chip that are caused by process offsets. Additionally, the remotely generated reference current is sensitive to bias voltage noise, temperature variations, and supply voltage variations.

BRIEF DESCRIPTION OF THE DRAWINGS

25 Embodiments disclosed herein are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements and in which:

 Figure 1 depicts a schematic diagram of an exemplary embodiment of a highly
30 distributed current reference 100 according to the subject matter disclosed herein;

 Figure 2 depicts a schematic diagram of a second exemplary embodiment of a highly distributed current reference according to the subject matter disclosed herein;

 Figure 3 depicts a schematic diagram of a third exemplary embodiment of a highly distributed current reference according to the subject matter disclosed herein; and

Figure 4 depicts an exemplary embodiment of a process 400 for generating a reference current according to the subject matter disclosed herein.

It will be appreciated that for simplicity and/or clarity of illustration, elements depicted in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. The scaling of the figures does not represent precise dimensions and/or dimensional ratios of the various elements depicted herein. Further, if considered appropriate, reference numerals have been repeated among the figures to indicate corresponding and/or analogous elements.

DESCRIPTION OF THE EMBODIMENTS

The subject matter disclosed herein relates to cross-point memories. More particularly, the subject matter disclosed herein relates to a low-power, high-accuracy current reference for highly distributed current reference for a cross-point memory. In the following description, numerous specific details are set forth to provide a thorough understanding of embodiments disclosed herein. One skilled in the relevant art will recognize, however, that the embodiments disclosed herein can be practiced without one or more of the specific details, or with other methods, components, materials, and so forth. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the specification.

Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments. Additionally, the word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any embodiment described herein as “exemplary” is not to be construed as necessarily preferred or advantageous over other embodiments.

Various operations may be described as multiple discrete operations in turn and in a manner that is most helpful in understanding the claimed subject matter. The order of description, however, should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation. Operations described may be performed in a different order than the described

embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

The subject matter disclosed herein provides a low-power, high-accuracy current reference system that can be used for highly distributed current references of a solid-state

5 memory, such as, but not limited to, a cross-point memory. In one exemplary embodiment, the low-power, high-accuracy current reference system disclosed herein comprises part of a solid-state drive. Embodiments of the subject matter disclosed herein utilize a source degeneration technique to compensate for current, temperature, supply and process variations. That is, embodiment of the subject matter disclosed herein use an active Metal-Oxide Semiconductor (MOS) device as a source degeneration resistance with active biasing that significantly reduces adverse influences of bias voltage noise, supply voltage variations and device offsets.

Additionally, embodiments of the subject matter disclosed herein provide a particularly low-power current reference system that is instantly available even during an exit from a standby mode by remaining in a sample-and-hold mode for long periods of time. Moreover,

15 embodiments of the subject matter disclosed herein use a relatively small area in comparison to conventional techniques. Although the subject matter disclosed herein is described in relationship to a cross-point memory, a solid-state memory and/or a solid-state drive, it should be understood that the subject matter disclosed herein is not so limited and is applicable in a system that utilizes highly distributed current references, such as, but not limited to, imaging systems and other sensor systems.

Figure 1 depicts a schematic diagram of a first exemplary embodiment of a highly distributed current reference 100 according to the subject matter disclosed herein. Highly distributed current reference 100 comprises a centrally located current digital-to-analog converter (IDAC) 101 and a plurality of remotely located TILE current references 102, of which only one remotely located TILE current reference 102 is shown. IDAC 101 comprises a first current source IBIAS/N, a second current source IBIAS, three Complementary Metal Oxide Semiconductor (CMOS) active devices M1-M3, a first buffer amplifier 110, a second buffer amplifier 111, and first and second switches 112 and 113. One terminal of current source IBIAS/N is coupled to a power supply voltage Vcc and the other terminal of current source IBIAS/N is coupled to the drain and the gate of active device M1. The source of active device M1 is coupled to a supply voltage HNVNN. One terminal of current source IBIAS is coupled to power supply voltage Vcc and the other terminal of current source IBIAS is coupled to the drain and the gate of active device M2. The source of active device M2 is coupled to the drain of

active device M3. The gate of active device M3 is coupled to the drain and gate of active device M1. The source of active device M3 is coupled to supply voltage HNVNN.

The drain of active device M2 is coupled to the input to buffer amplifier 110, and the gate of active device M3 is coupled to the input of buffer amplifier 111. The output of buffer amplifier 110 is coupled to the input of switch 112, and the output of buffer amplifier 111 is coupled to the input of switch 113. The output of switch 112 is coupled to a signal line SETBIAS. The output of switch 113 is coupled to signal line RESBIAS. The voltages appearing on the SETBIAS and RESBIAS signal lines are respectively based on a magnitude of the current through current source IBIAS and a magnitude of the current through current source IBIAS/N. Buffer amplifiers 110 and 111 have sufficient drive capability to charge capacitances C1 and C2, which respectively represent the coupling capacitance between signal line SETBIAS and supply voltage HNVNN and between signal line RESBIAS and supply voltage HNVNN.

Switches 112 and 113 are each controlled to sample and hold the respective outputs of buffer amplifiers 110 and 111 by a SAMPLE_EN signal. In one exemplary embodiment, the circuitry of IDAC 101 is capable of being turned off (i.e., placed in a standby mode), and when the voltages on signal lines SETBIAS and RESBIAS are to be refreshed, the circuitry of IDAC 101 is powered up and allowed to stabilize to refresh the voltages on signal lines SETBIAS and RESBIAS. SAMPLE_EN is then controlled to be “true” so that switches 112 and 113 are actuated and signal lines SETBIAS and RESBIAS are refreshed. SAMPLE_EN is then controlled to be “not true,” thereby opening switches 112 and 113. The circuitry of IDAC 101 is then controlled to be turned off (i.e., the standby mode) so that the highly distributed current reference does not dissipate power during the time that signal lines SETBIAS and RESBIAS are not being refreshed.

Signals lines SETBIAS and RESBIAS are distributed around the integrated circuit to a plurality of TILE current references 102, of which only one is shown in Figure 1. In one exemplary embodiment, signal lines SETBIAS and RESBIAS are coupled to more than 8000 TILE current references 102. In one exemplary embodiment, each TILE current reference 102 comprises CMOS active devices M4 and M5. The drain of active device M4 is coupled to a supply voltage HNREG, and the source of active device M4 is coupled to the drain of active device M5. The source of active device M5 is coupled to supply voltage HNVNN. The gate of active device M4 is coupled to signal line SETBIAS, and the gate of active device M5 is coupled to signal line RESBIAS.

The current variation through the current mirror at the HNREG node with respect to the current at IDAC 101 is minimized because active devices M3 and M5 operate in a linear

region and are respectively used as a degenerative resistance for the current mirrors (active devices M2 and M4). The resistive values of active devices M3 and M5 are equal or about equal. In one exemplary embodiment, node HNVNN comprises a node through which current passing through active device M4 is controlled by IDAC 101. The voltage drop across the
5 degeneration resistance (e.g., about 500 mV) mitigates the current variation due to V_t mismatch or supply variation (HNVNN) by linearizing the relationship between the current and the gate voltage of bias device M4. The gate voltage of the degeneration resistance generated at the center of the chip tracks, that is follows, variable DAC currents and also process, voltage, temperature (PVT) variations, thereby maintaining a relatively constant voltage drop across the
10 degeneration device.

The SETBIAS and RESBIAS signal lines track sudden HNVNN voltage variations based on the capacitance between them (i.e., capacitors C1 and C2). In one exemplary embodiment, signal lines SETBIAS and RESBIAS and power supply HNVNN are physically arranged to remain in close proximity to each other as they are distributed around an integrated
15 circuit. That is, the capacitance C1 between the SETBIAS line and power supply HNVNN and the capacitance C2 between the RESBIAS line and power supply HNVNN reduce inaccuracies caused by power supply variations coupling through active devices M4 and M5, and holds the bias for long periods of time (allowing for a sample-to-hold ratio in excess of 1:1000), thereby significantly reducing power consumption. Because SETBIAS and RESBIAS are always ready,
20 even during a HOLD operation, the circuit can be instantly used upon wakeup from standby or entry into an operation that utilizes a highly accurate reference current. It should be understood that capacitors C1 and C2 are depicted in the Figures using dashed lines because both C1 and C2 are distributed capacitances instead of being lumped-value capacitances. It should also be understood that in an alternative exemplary embodiment, at least a portion of capacitor C1 and/or
25 C2 could comprise a lumped-value capacitance.

Figure 2 depicts a schematic diagram of a second exemplary embodiment of a highly distributed current reference 200 according to the subject matter disclosed herein. The circuit configuration of highly distributed current reference 200 is similar to highly distributed current reference 100 (Figure 1) except that active device M3 of IDAC 201 is coupled to a supply
30 voltage V1 and no RESBIAS signal line is used. Supply voltage V1 can be an available supply voltage. Another difference between IDAC 201 and IDAC 101 (Figure 1) is that IBIAS/N and active device M1 are not needed for IDAC 201. Signal line SETBIAS for distributed current reference 200 is distributed around an integrated circuit to a plurality of TILE current references

102, of which only one is shown in Figure 2. Tile current references 102 are configured similar to the tile current references depicted in Figure 1.

Figure 3 depicts a schematic diagram of a third exemplary embodiment of a highly distributed current reference 300 according to the subject matter disclosed herein. The circuit configuration of highly distributed current reference 300 is similar to highly distributed current reference 200 (Figure 2) except that device M3 of IDAC 301 is embodied as a resistance R1 instead of an active device. Additionally, a TILE current reference 302 is similar to TILE current reference 102 except active device M5 is embodied as a resistance R2 having a resistance value equal to or about equal to the resistance value of resistance R1.

As yet another alternative exemplary embodiment, active devices M3 and M5 in Figure 1 could each be replaced with a degenerative resistance. It should be understood that devices M3 and M5 for any of the exemplary embodiments disclosed herein could be metal oxide semiconductor (MOS) devices, resistances, or a combination thereof.

Figure 4 depicts an exemplary embodiment of a process 400 for generating a reference current according to the subject matter disclosed herein. At 401, a first current is generated, such as IBIAS in Figure 1. At 402, based on the first current, a first voltage signal is generated based with respect to a first power supply. For example, the first voltage signal in some exemplary embodiments may correspond to the voltage at the output from buffer 110 in Figure 1, which is generated with respect to power supply HNVNN. At 403, based on the first current, a second voltage is generated with respect to the first power supply. For example, the second voltage signal in some exemplary embodiments may correspond to the voltage at the output of buffer 111 in Figure 1, which is generated with respect to power supply HNVNN. At 404, the first and second voltages are respectively sampled and held. At 405, the held first and second voltages are output to a plurality of remotely located tile current device, such as a tile current 102 in Figure 1. In one exemplary embodiment of the subject matter disclosed herein, the first voltage signal and the second voltage signal are generated using a degeneration-resistance device, which could comprise a metal oxide semiconductor (MOS) device or a resistance.

These modifications can be made in light of the above detailed description. The terms used in the following claims should not be construed to limit the scope to the specific embodiments disclosed in the specification and the claims. Rather, the scope of the embodiments disclosed herein is to be determined by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS:

1. A current reference source, comprising:

a current source to generate a first current;

5 a converter to generate a first voltage signal based on the first current, the converter comprising:

a first active device to generate a second current based on the first current, the first active device comprising a first terminal, a second terminal and a third terminal, the first terminal being coupled to the second terminal,

10 a first degeneration-resistance device comprising a first terminal and a second terminal, the first terminal being coupled to the first active device, and the second terminal being coupled to a first power supply voltage, and

a first buffer comprising an input and an output, the input of the first buffer being coupled to the first active device,

15 the first voltage signal being formed between the output of the first buffer and the first terminal of the first power supply.

2. The current reference source according to claim 1, wherein the first degeneration-resistance device comprises a second active device or a resistance.

20 3. The current reference source according to claim 2, wherein the first and second active devices comprise metal oxide semiconductor (MOS) devices.

25 4. The current reference source according to claim 1, wherein the current reference source comprises part of a solid-state drive.

5. The current reference source according to claim 1, further comprising at least one tile reference current generator coupled to the first voltage, the at least one tile reference current generator being remotely located from the current reference source.

30 6. The current reference source according to claim 5, wherein the at least one tile reference current generator comprises:

a third active device comprising a first terminal, a second terminal and a third terminal, the first terminal being coupled to the first voltage signal, and the second terminal being coupled to a first node of the at least one tile reference current generator, and

5 a second degeneration-resistance device comprising a first terminal and a second terminal, the first terminal being coupled to the third active device, and the second terminal device being coupled to the first power supply voltage.

7. The current reference source according to claim 1, wherein the first degeneration resistance comprising a third terminal coupled to a second voltage signal,

10 the current reference source further comprising a second buffer comprising an input and an output, the input being coupled the first degeneration-resistance device.

8. The current reference source according to claim 7, further comprising:

15 a first switch comprising a signal input, a signal output and a control input, the signal input being coupled to the output of the first buffer; and

a second switch comprising a signal input, a signal output and a control input, the signal input being coupled to the output of the second buffer,

20 the control inputs of the first and second switch being coupled to a control signal, and the first and second switches being responsive to the control signal to respectively sample and hold the outputs of the first and second buffers.

9. The current reference source according to claim 8, further comprising at least one tile reference current generator coupled to the output of the first switch and the output of the second switch, the at least one tile reference current generator being remotely located from the reference current source.

10. A tile reference current generator, comprising:

30 a first active device comprising a first terminal, a second terminal and a third terminal, the first terminal being coupled to a first signal line, and the second terminal being coupled to a node of the tile reference current generator, and

a first degeneration-resistance device comprising a first terminal and a second terminal, the first terminal device being coupled to the first active device, and the second terminal being coupled to a second power supply voltage,

a current flowing between the second terminal and the third terminal of the first active device being based on a first voltage signal, and the first voltage being based on a magnitude of a reference current generated by a current reference source that is remotely located from the tile reference current generator.

5

11. The tile reference current generator according to claim 10, wherein the first degeneration-resistance device comprises a second active device or a resistance.

12. The tile reference current generator according to claim 11, wherein the first and
10 second active devices comprise metal oxide semiconductor (MOS) devices.

13. The tile reference current generator according to claim 10, further comprising the remotely located current reference source, the remotely located current reference source comprising:

15 a first current source to generate a first current;
a converter to generate the first voltage signal based on the first current, the converter comprising:

a third active device to generate a second current based on the first
current, the third active device comprising a first terminal, a second terminal and a third
20 terminal, the first terminal being coupled to the second terminal,

a second degeneration-resistance device comprising a first terminal and a
second terminal, the first terminal being coupled to the third active device, and the second
terminal being coupled to the second power supply voltage, and

a first buffer comprising an input and an output, the input of the first
25 buffer being coupled to the third active device,

the first voltage signal being formed between the output of the first buffer and
second power supply voltage.

14. The tile reference current generator according to claim 13, wherein the second
30 degeneration-resistance device comprises a fourth active device or a resistance.

15. The tile reference current generator according to claim 13, wherein the third and
fourth active devices comprise metal oxide semiconductor (MOS) devices.

16. The tile reference current generator according to claim 13, wherein the second degeneration resistance comprises a third terminal coupled to a second voltage signal, the current reference source further comprising a second buffer comprising an input and an output, the input being coupled to the second degeneration-resistance device.

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17. The tile reference current generator according to claim 13, further comprising: a first switch comprising a signal input, a signal output and a control input, the signal input being coupled to the output of the first buffer, and the output being coupled to the first signal line; and

10 a second switch comprising a signal input, a signal output and a control input, the signal input being coupled to the output of the second buffer, and the output being coupled to the second signal line,

the control inputs of the first and second switch being coupled to a control signal, and the first and second switches being responsive to the control signal to respectively sample and hold the outputs of the first and second buffers.

15

18. A method to generate a reference current, comprising:

generating a first current;

generating based on the first current a first voltage signal with respect to a first

20 power supply;

generating based on the first current a second voltage signal with respect to the first power supply;

sampling and holding the first voltage and the second voltage; and

outputting the held first voltage and the held second voltage to a remotely located

25 tile current device.

19. The method according to claim 18, wherein generating the first voltage signal and generating the second voltage signal comprises using a degeneration-resistance device.

30 20. The method according to claim 19, wherein the degeneration-resistance device comprises a metal oxide semiconductor (MOS) device or a resistance.

21. An apparatus to generate a reference current, comprising:

means for generating a first current;

means for generating based on the first current a first voltage signal with respect to a first power supply;

means for generating based on the first current a second voltage signal with respect to the first power supply;

5 means for sampling and holding the first voltage and the second voltage; and

means for outputting the held first voltage and the held second voltage to a remotely located tile current device.

22. The apparatus according to claim 21, wherein said means for generating the first
10 voltage signal and generating the second voltage signal comprises means for using a degeneration-resistance device.

23. The apparatus according to claim 22, wherein the degeneration-resistance device comprises a metal oxide semiconductor (MOS) device or a resistance.

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100

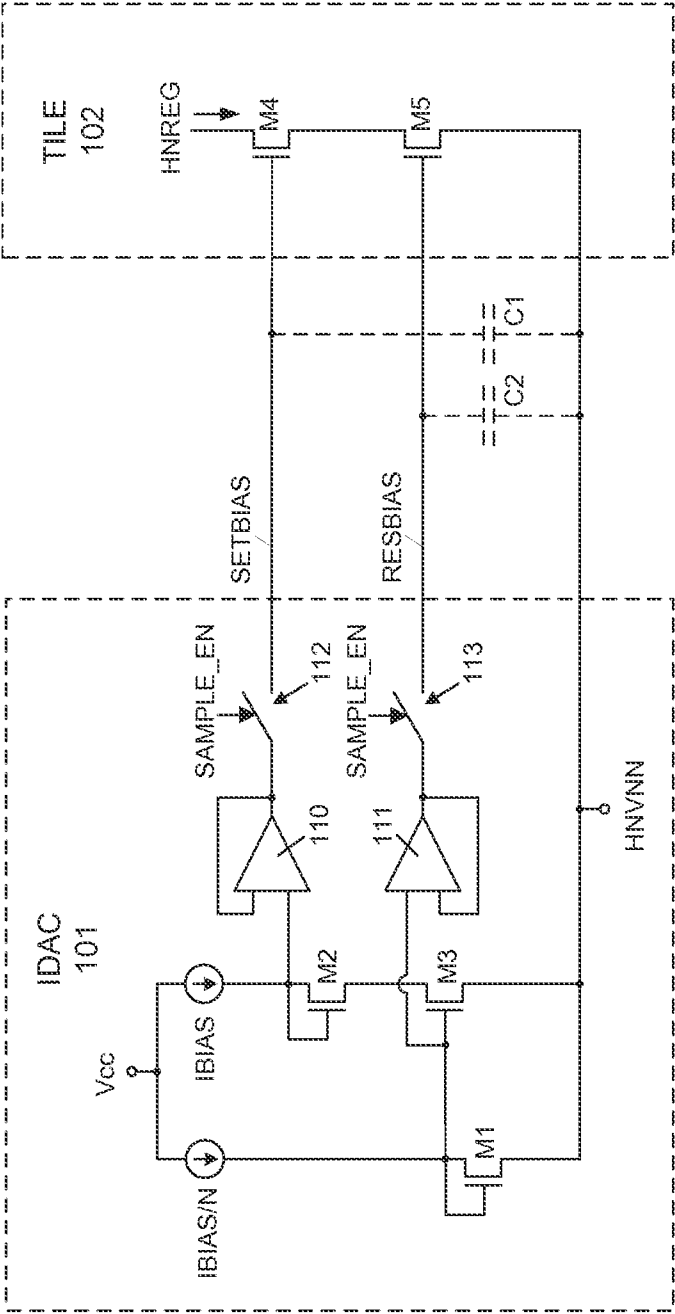


FIG. 1

200

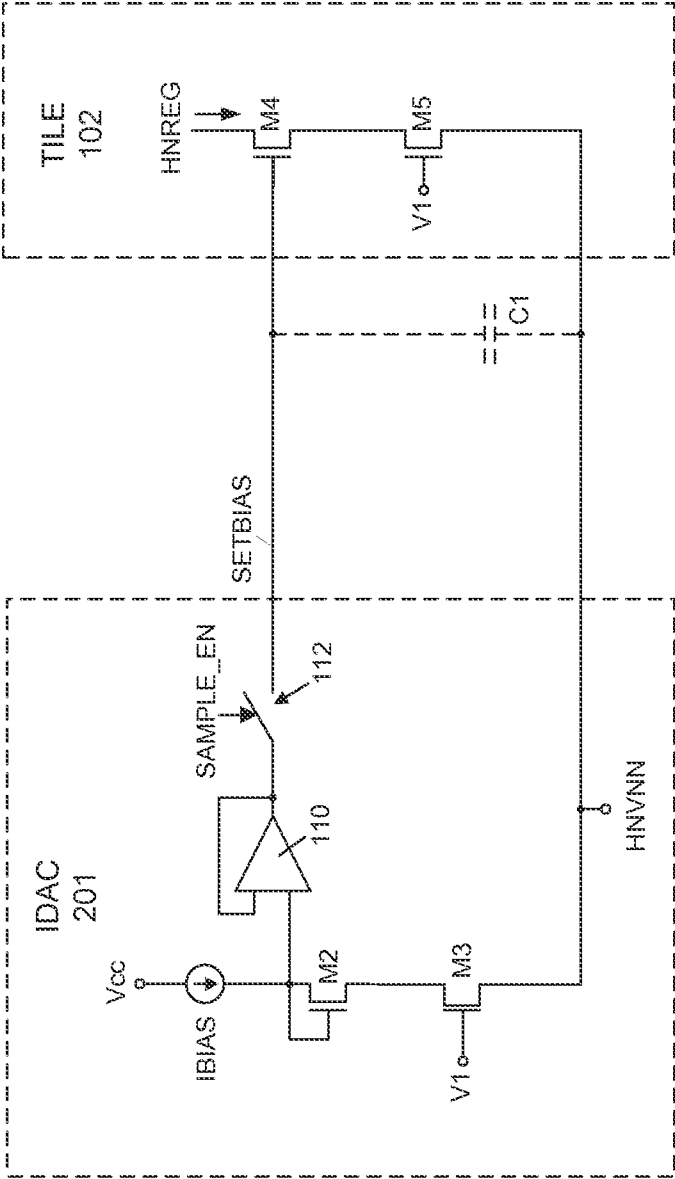


FIG. 2

300

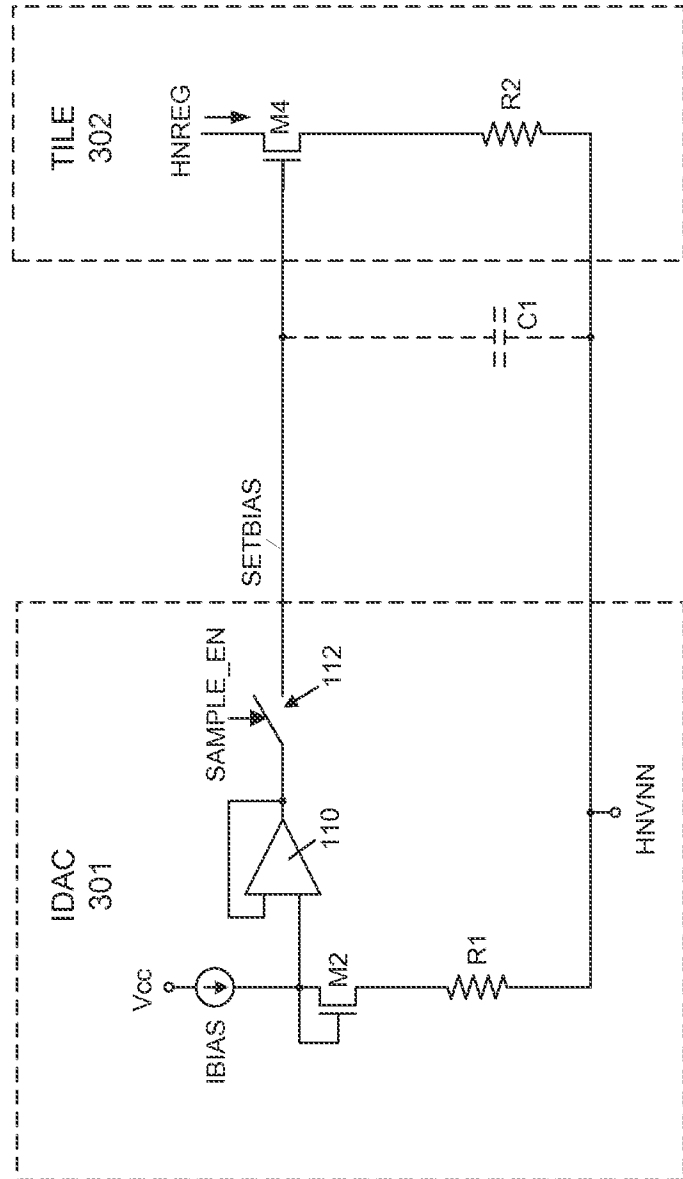


FIG. 3

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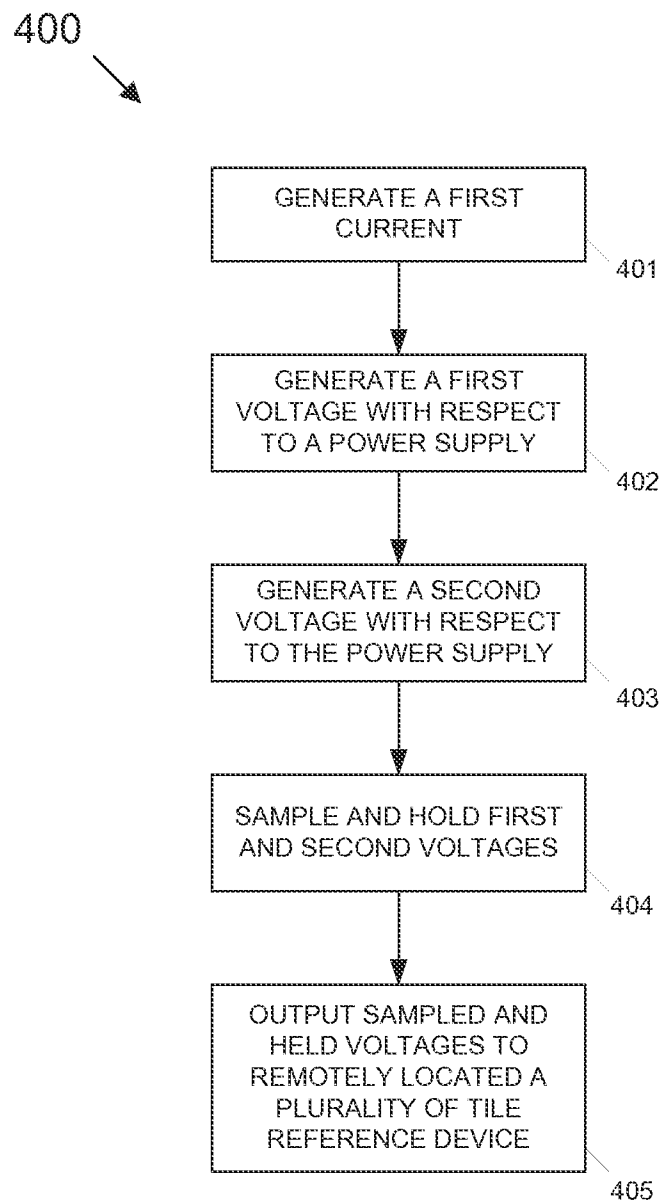


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/016288**A. CLASSIFICATION OF SUBJECT MATTER****G11C 5/14(2006.01)i, G11C 7/10(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 5/14; G11C 11/21; G11C 7/02; G05F 1/10; G05F 3/16; G11C 5/02; G11C 7/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: reference, current, source, memory, cross-point

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010-0148855 A1 (DA-GUANG YU et al.) 17 June 2010 See paragraphs [0020], [0024]; and figure 1.	1-23
A	US 2013-0002228 A1 (YANYI L. WONG et al.) 03 January 2013 See paragraphs [0024]-[0033]; and figure 2.	1-23
A	US 7227804 B1 (BADRINARAYANAN KOTHANDARAMAN et al.) 05 June 2007 See column 7, line 27 - column 8, line 9; and figure 3.	1-23
A	US 7023753 B2 (WAYNE THEEL) 04 April 2006 See column 15, line 52 - column 16, line 62; and figure 8.	1-23
A	US 2011-0188283 A1 (CHRISTOPHE J. CHEVALLIER et al.) 04 August 2011 See paragraphs [0044]-[0045]; and figure 4.	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0148855 A1	17/06/2010	JP 2010-152894 A US 07944281 B2	08/07/2010 17/05/2011
US 2013-0002228 A1	03/01/2013	None	
US 7227804 B1	05/06/2007	None	
US 7023753 B2	04/04/2006	US 2005-117408 A1	02/06/2005
US 2011-0188283 A1	04/08/2011	US 08363443 B2 US 08427868 B2 US 2011-188284 A1 US 2013-215667 A1 US 2013-229856 A1	29/01/2013 23/04/2013 04/08/2011 22/08/2013 05/09/2013