ABSTRACT

A gaming machine which is operated by a player when he manually actuates one of a plurality of switches each bearing a different symbol to activate the machine. The machine presents a display of various symbols, inclusive of those of the switches, which on each play of the machine changes the displayed symbols in a random manner to give a new display. Correspondence between the symbol of the manually activated switch and the same randomly displayed symbol results in a win signal in a win decoder with the win signal increasing depending upon the total number of correspondences therebetween. In addition, there is a different win signal if all the displayed symbols are the same, even though they do not correspond to the symbol of the pushed switch. Prize awarding means responsive to the win decoder awards numerical totals corresponding to the win signals. While normally only one switch is actuated and each switch controls its own triggering of a different stage of a shift register, a clock mechanism connected to the shift register will trigger all the stages thereof which is equivalent to pressing all of the switches if any one of the switches is manually pushed at the exact time as that corresponding to a predetermined stage of the counting state of the clock mechanism.
FIG. 2.

TO PAYOUT UNIT (FIG. 3)
GAMING MACHINE WITH COMPARISON OF RANDOMLY DETERMINED AND PLAYER PRESELECTED SYMBOLS

This invention relates to gaming machines of the kind commonly referred to as fruit machines in which a display of symbols is made to change in a random fashion so as to give any one of a plurality of possible final combinations of symbols during each play of the machine, a prize being awarded for certain final combinations (i.e., prize-winning combinations) of symbols resulting from each such play.

In most of the known gaming machines of the aforementioned kind the prize winning combinations and the corresponding prizes are all fixed and the player simply operates the machine to change the display.

According to the present invention we propose a gaming machine of the aforementioned kind comprising preselect means which allows the player before operating the machine, to increase the prize corresponding to at least one of the possible prize-winning combinations which can arise in the subsequent play of the machine.

Most simply, preselection involves choosing one of the symbols and registering this choice so that the machine is set to award appropriately increased prizes for a certain combination or certain combinations containing this symbol. Preferably, preselection also introduces prize-winning combinations which would otherwise exist and which contain the selected symbol.

This preselect feature according to the invention allows a player to increase his winnings by correctly predicting the subsequent occurrence of a combination of symbols and thereby makes the machine more interesting for the player.

According to a further feature of the invention we propose a gaming machine including reels which spin to produce an array of symbols and an electronic win decoder unit comprising sensing means associated with the reels which produces signals depending on the positions of the reels, and logical gating circuitry which receives the signals from the sensing means and which responds to those signals corresponding to a prize-winning combination of positions of the reels by producing an output signal indicative of the size of a corresponding prize. Preferably, the sensing means comprise a wiper contact fast with each reel which co-operates with relatively fixed contacts adjacent each reel, the wiper contacts engaging a different fixed contact for at least each of the prize-winning positions of the reels and producing a corresponding separate and distinct output signal from the fixed contact which it engages.

According to yet a further feature of the invention we propose a gaming machine having an electronic control unit comprising a binary counter which produces a predetermined sequence of control pulses to control a sequence of operations in the machine, each pulse corresponding to a predetermined counting state and each occurring at a random time after a start operation has been effected. Preferably, the counter counts continuously over a first part of its counting range prior to the start operation and the start operation frees the counter so that the count can proceed from whatever point has been reached in this first part of the range over the whole counting range, the control pulses being produced at counting states outside said first part of the range.

According to yet a further feature of the invention we propose a gaming machine including a payout unit comprising an electronic digital counter which is adapted to be set in a counting state corresponding to any prize, and which is adapted so that it controls the dispensing of tokens once at a time and counts up one in response to each dispensed token until it reaches the end of its counting range. The invention is now described by way of example with reference to the accompanying drawings in which:

FIG. 1 is a schematic diagram of the principal members and control circuitry of a fruit machine according to the invention,

FIG. 2 is a schematic diagram of part of the win decoder unit of the fruit machine of FIG. 1,

FIG. 3 is a schematic diagram of the payout unit of the fruit machine of FIG. 1.

The fruit machine comprises three reels R1, R2 and R3 which, as is conventional in fruit machines, are provided with symbols around their periphery and are mounted co-axially to be driven by a reel motor M. An electronic control unit comprises a clock pulse generator E, and a binary counter F which counts pulses from the generator E, and which in the counting states 28, 40, 52 and 60 produces control pulses from NAND gates G1, G2, G3 and G4 which act through bistable circuits H1, H2, H3, H4, H5, H6 through control solenoid-operated stops S1, S2, S3 and an electronic switch S4 associated with the reels R1, R2, R3 and the reel motor M. When the fruit machine is switched on but not being played pulse, inhibit signal derived from the output of the conducting portion H3 of the bistable circuit H3, H3 is applied to the conducting portions C and D of the bistable circuits C, C and D, D of the binary counter F which holds these bistable circuits in their zero state and thus limits the counting range of the counter to 16. The clock pulse generator E operates all the time that the fruit machine is switched on and while the fruit machine is not being played repeatedly causes the counter F to count up to 15 and to reset to zero on what would otherwise be the 16 count. During this time none of the NAND gates G1 to G4 pass a control pulse, as this can only occur on the counts of 28, 40, 52 and 60 which are outside the limited counting range up to 16.

The electronic control unit comprises a clock pulse generator E which delivers a pulse signal to the input of a binary counter F. The generator E comprises two Schmitt trigger circuits E1 and E2 with a common input each with an output connection to the input of a NAND gate E3 as shown in FIG. 1. The two circuits E1 and E2 oscillate at different frequencies and cause the NAND gate E3 to pass a pulse signal comprising a train of pulses at irregular intervals. The binary counter F comprises six bistable circuits P, P, Q, Q, A, A, B, B, C, C, and D, D interconnected as shown in FIG. 1 in which the two portions such as P, P of each bistable circuit represent the two alternately conducting portions or stable states thereof. The input connection from the generator E is connected to the first bistable circuit P, P, and output connections from the conducting portions A, A, B, B, C, C, and D, D are connected to the inputs of six four-input NAND gates G1, G2, G3, G4, G5 and G8. These connections are not shown fully in
FIG. 1 but those inputs of the NAND gates which are connected to the binary counter F are labelled with the reference letters of the conducting portions to which they are connected. These connections are such that the gates G1, G2, G3 and G4 each pass an output signal when the binary counter F is in the counting state 28, 40, 52 and 60 respectively, the highest counting state of the counter being 64. These outputs act through the bistable circuits H1, H1; H2, H2; H3, H3; and H4, H4 to control the stops S1, S2, S3 and the switch S4.

Playing of the fruit machine is initiated by the insertion of a token into a token insert mechanism (not shown) which action operates a switch T which in turn acts through the NAND gate G5 to set the bistable circuit H4, H4 in a state to start the reel motor M, and to reset a shift register J. This shift register J together with a series of selector switches K1 to K5 comprise preselection means (which will be more fully described below) which on operation of one of the switches K1 to K5 acts through a bistable circuit H5, H5 to set the bistable circuits H1, H1; H2, H2; H3, H3 in states to release all three reels R1, R2 and R3 and simultaneously remove the inhibit signal from the counter F so that all of the reels may rotate and the count progress from whatever count it has reached to include its whole counting range. On the count of 28 the NAND gate G1 passes a control pulse which sets the bistable H1, H1 to a state to cause the stop S1 to stop the reel R1, and similarly at later times on the counts of 40, 52 and 60 the NAND gates G2, G3 and G4 pass control pulses which act through the associated bistable circuits and stops to stop the reels R2, R3 and the reel motor M, the counter F finally resetting to zero automatically on the count of 64. Operation of the control unit to stop the reel motor M also triggers a win decoder unit through a connection Z4 and a payout unit through a connection Y2 whereupon the win decoder unit responds to a final position of the reels and passes information of any corresponding prizes to the payout unit which then pays out the corresponding prize in tokens.

The time for which each reel spins is equal to the time the counter takes in counting from its initial counting state when all of the reels start to spin to the counting state at which each reel is stopped. The initial counting state can be anywhere within the limited counting range 0 to 16, and for this reason alone the time for which each reel spins will generally vary from one play of the fruit machine to another. In the illustrated example assuming that the counter F counted at a regular rate, the uncertainty or randomness in the time for which the reels spin due to variation in the initial counting state is of the order of ±8/28 or ±30 percent of the time for which the reel R1 spins. However, the counter does not in fact count at a regular rate due to the irregularity in timing of the pulses from the generator E, and because of this the time taken by the counter to count over any counting range will vary and introduce an additional randomness in the time for which each reel spins.

The above description indicates the general sequence of operations in the control unit by which spinning of the reels and operation of the win decoder unit and payout unit are controlled.

The principal feature of the illustrated fruit machine as far as the present invention is concerned is the preselection means comprising the five stage shift register J and the five selector switches K1 to K5. Each of these selector switches K1 to K5 is connected in an individual input connection to a separate one of the stages J1 to J5, respectively, of the shift register and serves to make the corresponding stage conducting when operated, and each stage J1 to J5 of the shift register has an output connection through individual diodes L to the input of an INVERTER gate G7 and has an individual output connection X1 to X5, respectively, to the win decoder unit. As already described above, insertion of a token into the token insert mechanism by a player closes the switch T and causes the NAND gate G5 to pass a signal to the shift register J which resets all of the stages J1 to J5 to the non-conducting state. The player then has to select and operate just one of the selector switches K1 to K5, which action triggers the corresponding stage of the shift register and causes it to deliver a position output signal to the INVERTER gate G7. The gate G7 then passes a zero signal to the shift register which serves to prevent operation of another selector switch energising a stage of the register, and passes a similar signal to the bistable circuit H5, H5 which causes release of the three reels and freeing of the counter F.

Operation of a selector switch also produces an output signal to the win decoder unit through the corresponding connection X1 to X5, and unless an enriched condition exists as described below, this is the only such signal and it sets up corresponding prize-winning combinations in the win decoder unit. Preferably, each of the selector buttons K1 to K5 is labelled with a different symbol and the corresponding prize-winning combinations set up in the win decoder unit by operation of that selector button involve this symbol. For the purposes of the description hereinafter we shall consider that the selector switch K1 is labelled with a plum symbol and that operation of this switch sets up prize-winning combinations in the win decoder unit comprising a plum symbol displayed on reel R1 only, plum symbols displayed on the reels R1 and R2 only, and plum symbols displayed on all three reels.

The logical gating circuitry shown in FIG. 2 is that part of the win decoder unit which responds to prize-winning combinations involving a plum symbol, these combinations being set up in response to a signal on the input connection X1 in response to operation of the selector key K1. Position information of the reels is supplied through connections Z1, Z2 and Z3 from position sensing means comprising wiper contacts W1, W2 and W3 which are connected to rotate with the reels R1, R2 and R3, respectively, and which co-operate with electrical studs on stud boards V1, V2 and V3, respectively, each stud board being provided with a pair of studs for each position of the respective reel and these pairs of studs being arranged so that a corresponding pair is bridged by the respective wiper arm and produces a positive output signal in an associated output connection for each position of each reel. The connections Z1, Z2 and Z3 are associated with pairs of studs on the stud boards V1, V2 and V3, respectively, which are bridged and deliver positive output signals when the respective reels are in positions in which they display a plum symbol.

The input connection Z1, Z2, Z3 and X1 are all connected to the inputs of four NAND gates G11, G12, G13 and G14, as shown in FIG. 2, each of which is associated with a corresponding two-input NAND gate G21, G22, G23 and G24, having output connections 2, 4, 12 and 8, respectively, to the payout unit, and the
input connection Z4 is connected through an INVERTER gate G20 to one input of each of the NAND gates G21, G22, G23 and G24. The input connections X1 and Z4 supply control signals to the two groups of NAND gates G11, G12, G13 and G21, G22, G23, G24 respectively. The control signal on X1 is dependent on the selector switch K1 and comprises a zero input signal which inhibits the gates G11, G12 and G13 when the selector switch K1 has not been operated, and a positive input signal which allows operation of these gates when the selector switch K1 has been operated. The control signal on Z4 is dependent on the reel motor M and comprises a zero input signal which inhibits the gates G21, G22, G23 and G24 when the reel motor is operating, and a positive input signal which allows these gates to operate when the reel motor has stopped. We will now consider operation of the circuitry of FIG. 2 once the selector switch K1 has been operated and the reel motor stopped with the three reels displaying each of the three prize-winning combinations involving plum symbols.

If just the first reel R1 is in a position in which it displays a plum symbol, the connection Z1 applied a positive input signal to the NAND gate G11, which causes it to pass a zero output signal to one input of a two-input NOR gate G15. The other input of the NOR gate G15 has a zero input signal applied to it already through an INVERTER gate G16 from the output of the NAND gate G12 and thus the NOR gate G15 passes a positive input signal to one input of the two-input NAND gate G21 which causes it to pass a zero output signal through the connection 2 to the payout unit.

If just the first two reels R1 and R2 are in positions in which they display plum symbols the connections Z1 and Z2 apply positive input signals to the NAND gate G12 which causes it to pass a zero output signal to the input of the INVERTER gate G16 and one input of a two-input NOR gate G17. The INVERTER gate G16 responds by passing a positive output signal to one input of the NOR gate G15, which signal acts as an inhibit signal which prevents the zero input from passing a positive output signal to the NAND gate G21 to set the payout unit through the connection 2. The NOR gate G17 is similar to the NOR gate G15, its other input having a zero input signal applied to it through an INVERTER gate G18 from the output of the NAND gate G13 and thus it responds to the zero output signal from the NAND gate G12 by passing a positive output signal to one input of the two-input NAND gate G22 which causes it to pass a zero output signal to the payout unit through the connection 4.

If all three reels are in positions in which they display plum symbols, the connections Z1, Z2 and Z3 apply positive input signals to the NAND gate G13 which causes it to pass a zero output signal to the input of the INVERTER gate G18 which in turn passes a positive output signal. This positive output signal passes to the NOR gate G17 and acts as an inhibit signal which prevents this gate from passing a positive output signal to the NAND gate G22 to set the payout unit through the connection 4. A similar inhibit signal is also applied through the INVERTER gate G16 on the NOR gate G15, as already described above, which prevents setting of the payout unit through the connection 2. The positive output signal from the INVERTER gate G18 also passes to one input of a two-input NOR gate G19 which is connected between the NAND gate G14 and a NAND gate G24 and acts as an inhibit signal which stops the positive output signal from the NAND gate G14 passing to the NAND gate G24. Lastly, the same positive output signal from the INVERTER gate G18 also passes to one input of a two-input NAND gate G23 which causes it to pass a zero output signal to the payout unit through the connection 12.

If a selector switch other than K1 is operated and a combination of three plum symbols is displayed once the reels and reel motor stop, the inhibit signal applied to the NAND gate G13 by the input connection X1 prevents it from passing a zero output pulse to set the payout unit. However, this inhibit signal does not control the NAND gate G14 which also has inputs connected to the connections Z1, Z2 and Z3 and thus it passes a zero output signal which passes to the NOR gate G19. The other input of the gate G19 no longer has an inhibit signal applied to it by the gate G18 and thus it passes a positive output signal to the NAND gate G24 causing it to pass a zero output signal through the output connection 8 to the payout unit.

Thus, that portion of the win decoder unit shown in FIG. 2 is adapted to respond to prize-winning combinations comprising one, two and three plum symbols, it being controlled so that, if the selector key K1 is labelled with a plum has not been operated, it only responds to the three plum combination and passes a corresponding payout signal to the payout unit through the output connection 8, and if the selector key K1 has been operated it responds to the one, two and three plum combinations and passes corresponding payout signals to the payout unit through the output connections 2, 4 and 12, respectively. The labelling 2, 4, 12 and 8 used for output connections to the payout unit indicate the number of tokens which the payout unit delivers in response to an output signal on these connections. Operation of the selector key K1, therefore, serves to increase the prize corresponding to the three plum prize-winning combinations and also adds two new prize-winning combinations, each having a corresponding lower prize associated with it.

The complete win decoder unit comprises logical gating circuitry similar to that of FIG. 2 for each of the selector keys K1 to K5, each selector key being labelled with a different symbol and the input connections corresponding to Z1, Z2 and Z3 being appropriately connected to the reel position sensing means. The win decoder unit may also comprise other logical gating circuitry providing other prize-winning combinations which are always set up no matter which selector switch has been operated. Such prize-winning combinations may involve symbols not used to label the selector switches. The prizes corresponding to any combination is simply determined by the output connection to the payout unit and can be selected as required.

The payout unit itself may comprise any form of unit which can be selectively triggered to dispense any number of tokens. Preferably, however, the payout unit comprises a digital counter which is set in a corresponding state by each of the different output signals from the win decoder unit, and which thereafter counts up from this state to its maximum capacity, dispensing a token for each such count.

An example of a suitable payout unit of this kind is illustrated in FIG. 3. This payout unit comprises a token dispenser unit driven by a motor N which is controlled by a binary counter E' so as to dispense the
number of tokens corresponding to wins indicated by zero input signals through any of the connections 2, 4, 6, 8, 10 or 12 from the win decoder unit. The binary counter E' comprises four bistable circuits A, B, C, C and D, which are interconnected to form a counter with a counting capacity of 16. Each of the conducting portions A, B, C and D has an output connection with a positive bias voltage of 5 volts applied to it which normally holds the counter E' in its 0 or 16 counting state, and all of these output connections are connected through one or more of the diodes L' to the connections 2, 4, 6, 8, 10, 12 and 5, as shown in FIG. 3, so that application of a zero input signal to each of the latter connections in turn triggers the counter to the 14, 12, 10, 8, 6, 4 and 14 counting states respectively.

Each of the conducting portions A, B, C and D has an output connection to the input of a four input NAND gate G25, and these connections are such as to deliver positive output signals simultaneously only when the counter is in the 0 or 16 counting state, whereupon the NAND gate G25 passes a zero signal to the input of a two input NAND gate G26. Thus, if the counter has been set to a counting state other than 16 by a zero input signal on any of the connections 2, 4, 6, 8, 10, 12 and 5, then the NAND gate G25 delivers a positive output signal to the input of the NAND gate G26. The other input of the NAND gate G26 is connected to the connections Y2 from the control unit (FIG. 1) which delivers a positive output signal only when the reel motor M is not operating. Thus, if the counter E' is in any state other than 0 or 16 and the reel motor M is not operating the NAND gate G26 passes a zero output signal which is inverted by an INVERTER gate G27 and starts the motor N. While the motor N operates it causes the token dispenser unit to dispense tokens one at a time and operates a switch T' so as to generate an output pulse from a bistable circuit H7, H7 each time that a token is dispensed, these pulses being fed to the input of the binary counter E' and causing it to count up towards the 0 or 16 counting state. When the counter reaches the 0 or 16 counting state, four positive output signals are delivered to the NAND gate G25 which as a result passes a zero output signal to the NAND gate G26 thus stopping the motor N so that no more tokens are dispensed.

It should be clear from the above description that a zero signal applied to the connection 2 from the win decoder unit will set the counter to the 14 counting state, the motor N will be started, and the token dispenser unit will dispense two tokens before the corresponding pulses form the bistable circuits H7, H7 will cause the counter E' to count back up to the 0 or 16 counting state at which it stops the motor N. Similarly, a zero signal applied to the connection 4 will set the counter in the 12 counting state, and four tokens will be dispensed before the counter E' returns to the 0 or 16 counting state and the motor N is stopped. Zero signals applied to the 6, 8, 10 and 12 connections will similarly cause six, eight, 10 and 12 tokens to be dispensed. For the logical gating circuitry of the win decoder unit shown in FIG. 2 the connections 2, 4, 8 and 12 are used but it will be appreciated that these connections could be changed so that one, two and three plums paid out any other prizes.

The preselection means is also adapted so as to provide an enrich feature whereby under certain conditions all of the prize-winning combinations corresponding to the selector switches K1 to K5 are set-up simultaneously. This occurs if a selector switch is operated when the counter F of the control unit is in the fifteen counting state, this state being detected by coincidence of a pulse derived from a four input NAND gate G8 which is connected to the counter F and passes a zero output pulse on the count of 15, and a pulse derived from the INVERTER gate G7 which passes a zero output pulse when a selector switch is operated. The pulse from the NAND gate G8 is supplied through an INVERTER gate G9 to one input of a two input NAND gate G10, and the pulse from the INVERTER gate G7 is supplied through an a.c. coupled Schmitt trigger circuit E4 to the other input of the NAND gate G10. If the counter F is in its 15 counting state when a selector switch is operated positive input signals are applied to both inputs of the NAND gate G10 which responds by passing a zero output signal to a bistable circuit H6, H6 to set it so that it delivers a positive output signal to the serial input of the shift register J and to one input of a two input NAND gate G11. The other input of the gate G11 is connected to the output of the clock pulse generator E so that the positive input from the bistable circuit causes the gate G11 to pass pulses corresponding to the clock pulses from the generator E to the shift register J, which pulses serve to energise all of the stages J1 to J5 of the register. Thus output signals are delivered through all of the connections X1 to X5 to set-up the corresponding prize-winning combinations in the win decoder unit. The bistable circuit H6, H6 is subsequently reset by a signal from the output of the gate G1 on the count of 28 and the shift register itself is reset by a pulse from the NAND gate G5 when the next player inserts a token.

In the control unit as illustrated in FIG. 1, the counting range of the binary counter F is limited before insertion of a token by an inhibit voltage which is applied to the last two bistable circuits, C, C and D, D of the counter. In an alternative embodiment of the invention a logic gate might be connected between the bistable circuits B, B and C, C which is controlled by a signal corresponding to the inhibit signal so that no pulse could pass between these bistable circuits before a token is inserted.

In another alternative embodiment the control unit may comprise a clock pulse generator which produces pulses at irregular intervals, a digital counter which is fed these pulses from the clock pulse generator, and stop means which stops the supply of pulses to the counter when the fruit machine is not being played but which allows the supply of pulses to the counter when the fruit machine is played so that the counter counts up from zero at an irregular rate determined by the interval between successive pulses and produces successive output signals to control operations in the fruit machine at predetermined counts above zero.

It will be appreciated that the control unit is not restricted to use in fruit machines but is of general application in gaming machines which require a predetermined sequence of control pulses to control a sequence of operations at a random time after a start operation has been effected.

Further, although the invention consists primarily in the preselection feature, the control unit, the win decoder unit comprising logic gating circuitry which is fed electrical signals indicative of the positions of the reels
and which produces corresponding output signals indicative of prizes which have been won, and the payout unit comprising a counter which counts up to its maximum capacity and which dispenses a token for each such count, are each considered inventive per se.

I claim:

1. A gaming machine comprising display means which displays a combination of symbols to a player and which operates to change the displayed combination in a random manner and to produce a final randomly selected combination during each game; sensing means operatively associated with said display means; a plurality of signalling circuits through which the sensing means are connected to prize signalling circuits; pre-selection means comprising a plurality of manually operable devices each corresponding to a respective one of said symbols and operation of which activates said display means; circuit means associated with said manually operated devices and said prize signalling circuits so that correspondence between a manually operated device and displayed symbols creates win signals which increase dependent upon the number of correspondences therebetween, the win signal being further increased when all of the displayed symbols correspond to the manually operated device, and prize awarding means responsive to corresponding win signals.

2. The machine of claim 1 including one of said prize signalling circuits connected to said sensing means producing a different win signal when the final combination of symbols produced by said display means have correspondence to each other but not to said manually operated device.

3. A gaming machine as claimed in claim 1 in which said display means comprises reels which carry said symbols around their periphery and which are spun to change the display, and in which said sensing means comprises separate rotary switches which rotate with each reel and which have output switch contacts connected individually to said signalling circuits.

4. A gaming machine as claimed in claim 3 in which said prize-signalling circuits are logic gating circuits which include first logic gates with input connections from said signalling circuits.

5. A gaming machine as claimed in claim 4 in which each of said manually operable devices controls application of an output signal to one or more of the inputs of said first logic gates of corresponding prize-signalling circuits.

6. A gaming machine as claimed in claim 5 in which said preselection means includes a shift register and each of said manually operable devices controls operation of different stages of the shift register and when operated triggers this stage to produce said output signal therefrom to the first logic gates.

7. A gaming machine as claimed in claim 6 which further includes clock means which is connected to said shift register and which triggers all of the stages thereof to make all of the corresponding prize-signalling circuits operative if a manually operable device is operated at a preset time as determined by said clock means.

8. A gaming machine as claimed in claim 1 which includes an electronic control unit comprising a pulse generator and a digital counter which counts pulses from the pulse generator and which in predetermined counting states produces control pulses to control operation of said display means, said sensing means and said prize awarding means.

9. A gaming machine as claimed in claim 8 further comprising starter means which is operated by a player to begin a game on the machine and which controls said digital counter so that it is restricted to count over only a limited first part of its range when the starter means is in its inoperative state and does so in a cyclic manner by reverting to zero each time that it reaches the end of its limited range, and is free to count over the whole of its range when the starter means is operated by a player; and a number of output gates which are connected to the counter so that they each pass a control signal to said display means, said sensing means and said prize awarding means when the counter is in a respective counting state outside the said limited range.

10. A gaming machine as claimed in claim 9 in which the digital counter is a binary counter comprising a series of bistable circuits which are divided into first and second groups, the first group corresponding to the said limited range, and the second group being controlled by stop means which is in turn controlled by the starter means.

11. A gaming machine as claimed in claim 10 in which the stop means comprises means which serves to apply an inhibit voltage to the second group of bistable circuits so that they are held in their zero counting state.

12. A gaming machine comprising display means which displays a combination of symbols to a player and which operates to change the displayed combination in a random manner and to produce a final randomly selected combination during each game; sensing means including switch means which is operatively associated with said display means and a plurality of prize signalling circuits to which the switch means is connected so that when the display means displays each of a predetermined number of final combinations of symbols the switch means causes a corresponding prize signalling circuit to produce a corresponding signal; prize awarding means which responds to said signals and awards corresponding prizes; pre-selection means comprising a plurality of manually operable devices each corresponding to a respective one of said symbols and operable by a player before the display means operates to activate the same, two of said prize signalling circuits associated with each symbol being such as to produce a win signal in response to the same final winning combination of that symbol means responsive to the win signal of one of the two circuits for operating said prize awarding means to the exclusion of the win signal of the other of the two circuits to award a prize of one value when said same final combination includes the symbol of the device which has been operated; means responsive to the win signal of the other of the two circuits for operating said prize awarding means to the exclusion of the win signal of the first of the two circuits to award a prize of another value when said same final winning combination does not include the symbol of the device which has been operated, each of the other signalling circuits associated with each symbol producing a win signal in response to a final combination of symbols different from said winning combination but which includes the symbol of the device which has been operated; and means which allows only a set number of said manually operated devices to be operated.
13. A gaming machine comprising display means which displays a combination of symbols to a player and which operates to change the displayed combination in a random manner and to produce a final randomly selected combination during each game; sensing means including switch means which is operatively associated with said display means; a plurality of pairs of prize-signalling circuits each pair being associated with a respective symbol, to which the switch means is connected so that when the display means displays each of a predetermined number of final combinations of similar symbols the switch means causes the associated pair of prize signalling circuits to produce a pair of corresponding win signals pre-selection means comprising a plurality of manually operable devices each corresponding to a respective one of said symbols and operable by a player before said display means operates to activate the same and to render effective the win signal of one of the circuits of a pair while rendering ineffective the win signal of the other circuit of said pair when said win signals correspond to the symbol of the device which has been operated; means for rendering the win signal of said other circuit effective while rendering the win signal of said one circuit ineffective when the win signal does not correspond to the symbol of the device which has been operated; prize awarding means which responds to an effective win signal from said one prize signalling circuit of each pair by awarding a corresponding prize, and which responds to an effective win signal from the other prize signalling circuit of each pair by awarding a corresponding prize lower than the first mentioned prize; and means which allow only a set number of said manually operable devices to be operated before said display means operates.