METHOD AND APPARATUS FOR SOLDERING MODULES TO SUBSTRATES

Vacuum pick-up head of rework system/machine
QFN device

Bottom cover
METHOD AND APPARATUS FOR SOLDERING MODULES TO SUBSTRATES

Field of the Invention

The present invention relates to a method and apparatus for attaching a module such as a semiconductor device, to a substrate such as a printed circuit board.

Background of the Invention

Conventional processes for the assembly rework of surface mount technology (SMT) boards typically comprise removal of the components and cleaning of the sites. To fix the replacement components to the boards, one or more flat mini-metal stencils are applied to the boards to define the solder pattern to be applied. Solder paste is then applied to the solder pads on boards and is forced through the apertures in the stencil(s) using a squeegee. The one or more stencils are then removed. The semiconductor device is then positioned on the board and fixed thereto by reflow soldering of the solder paste.

The flat mini-metal stencil is custom-sized to fit into the reworked space within the confines of surrounding components. The mini-metal stencil may be formed with sides and other features that allow for manual mechanical fixturing for alignment to the printed circuit board (PCB) pattern. However, these mini-metal stencils lack the mechanical support of the rigid stencil frame, as well as the automated functions of alignment, contact pressure, squeegeeing and stencil lift off that make the use of metal stencils successful in the primary SMT printing function.

In such conventional processes, the flat mini-metal stencil is positioned by manual alignment and is taped along the stencil's edges to the PCB. Alternatively, the formed mini-metal stencil may be aligned with a mechanical arm, which is required to be set-up for each component location. Both of
these methods can result in insufficient mechanical retention between the stencil and PCB surface. Other problems with such conventional processes are that the stencil position may shift during squeegee passes, and the stencil may need to be removed and the board require cleaning and re-stencilling. Furthermore, alignment and positioning are typically difficult in such processes. Also, mini-metal stencils must be cleaned thoroughly between each use.

Further difficulties with the mini-metal stencil method include the possibility of not having enough solder paste deposited to form the contact pad or of having solder paste bleed under the stencil.

As the stencil is made of metal, it is not easy to tailor the stencil to fit the reworked site which is typically a confined spaced between other semiconductor devices. As a result, the use of the mini-metal stencils requires a high level of skill to ensure that the correct amount of solder paste is deposited with only a single pass of the squeegee.

An alternative conventional method is to use a mini-metal stencil to apply the paste to the semiconductor device contacts and the thermal pads on the semiconductor device, rather than to apply the stencil to the land of the printed circuit board as described above. Similar difficulties arise in this alternative method, as are mentioned above.

A number of the above-mentioned problems with prior art systems are addressed in US patent no. 6,253,675 of Mayer which describes a solder paste stencil printing apparatus and method. The stencil is a disposable, adhesive-backed, flexible, polymer membrane rather than being formed of metal. The stencil adheres to the PCB whilst the solder paste is applied thereto and squeegeed across the stencil surface. The stencil is then removed and the semiconductor device is located manually on the solder
paste. A reflow process is applied to melt the solder and fix the semiconductor device to the PCB.

Although the device and methods described in US patent no. 6,253,675 address some of disadvantages associated with conventional techniques using metal stencils, such as fixing the stencil to the PCB during the squeegee passes to prevent relative movement and inhibiting the solder paste from seeping under the stencil, the systems and devices described in this patent may still suffer from a number of disadvantages. For example, the alignment and positioning problems described above in connection with metal stencil techniques still exist, as well as the possibility of damage during stencil removal. Furthermore, a high level of skill is still required to ensure that the correct amount of solder paste is deposited with only a single pass of the squeegee.

US patent application no. 09/753,876 of Davis et al, published as US 2001/0000905 A1 describes a system for ball grid arrays in which the conventional stencil is replaced with a preformed alignment device having a pattern of holes therethrough which may be aligned with the pattern or footprint of the ball grid array. The holes are filled with either solder paste, a curable conductive adhesive, or solid solder.

In use, the preform described in US 2001/0000905 A1 is attached to a PCB and the semiconductor is then placed above the preform so that the preform is interposed between the semiconductor being placed on the PCB and the PCB, with the material in the filled holes being in contact with the solder balls on the semiconductor device and the contact pads on the PCB. Heat is applied to reflow the solder or cure the adhesive in the holes to join the semiconductor device to the PCB. The preform may be left in place on the PCB thereby eliminating the possibility of damage which may occur in other conventional systems where the stencil is removed. Alternatively, if it is
desired to remove the preform, a suitable material which can be dissolved away after the reflow process is used to form the preform. However, the alignment problems described above in connection with metal stencil techniques still remain.

In view of the foregoing problems with conventional processes and devices, a need exists for a quick and an easily applied method for replacing individual leadless semiconductor devices, such as QFN devices.

**Summary of the Invention**

In general, the invention relates to an apparatus and method for attaching a module having an array of contacts thereon arranged in a given pattern to a substrate having an array of contact pads, comprising applying an array of solder blocks to said module and attaching the module to the substrate.

According to a first aspect of the present invention there is provided a method for attaching a module having an array of contacts thereon arranged in a given pattern to a substrate having an array of contact pads, comprising the steps of:

- applying an array of solder blocks to the array of contacts on said module;
- positioning the module on said substrate so that said array of solder blocks contacts the array of contact pads on the substrate; and
- applying heat to reflow the solder blocks to provide mechanical and electrical connection of the module to said substrate.

According to a second aspect of the present invention there is provided a method of attaching a semiconductor device, such as a Quad Flatpack Nonlead (QFN) device, having an array of contacts thereon arranged in a
given pattern to a printed circuit board having an array of contact pads, comprising the method defined above.

According to a third aspect of the invention there is provided a device for attaching a module having an array of contacts thereon arranged in a given pattern to a substrate having an array of contact pads, the device comprising:

- a removable carrier; and

- an array of solder blocks arranged in an aperture in said carrier;

said aperture being arranged to receive and align said module to align said array of contacts thereon with said array of solder blocks; wherein said array of solder blocks are arranged to contact said array of contact pads on said substrate after removal of said removable carrier.

According to a fourth aspect of the present invention there is provided a sheet comprising an array of devices of the type defined above, each of said devices in said array being removable from said sheet.

The invention thereby proposes an alternative method to the conventional solder paste printing with mini-stencils.

The methods and devices of the present invention are particularly advantageous over the prior art systems and methods which tend to suffer from problems with paste thickness and volume consistency, and alignment problems. In the embodiments of the present invention, no stencil tooling is required and therefore less skill is required in implementing the process. Furthermore, the reworking of highly populated PCBs is easily achieved. Also, the solder deposition step takes less time than conventional stencil printing techniques, thereby improving rework efficiency.
Brief Description of the Drawings

The present invention will now be described by way of example and with reference to the accompanying drawings in which:

Figure 1 is a sectional elevation of a solder block array according to an embodiment of the present invention;

Figure 2 is a plan view of a carrier containing the solder block array of Figure 1;

Figure 3a is a plan view of the carrier of Figure 2 with the top cover removed to show the solder block array of Figure 1;

Figure 3b is a plan view of the carrier of Figure 2 with the top cover removed to show an alternative solder block array to that shown in Figure 3a;

Figure 4 is a partial sectional side elevation through the solder block of Figure 1 with the top cover partially removed;

Figure 5 is a side elevation of a solder block array according to an embodiment of the invention attached to a QFN device to be fitted to a board, with the bottom cover of the solder block array partially removed; and

Figure 6 is a plan view of a sheet containing a plurality of solder block arrays according to an embodiment of the present invention in their carriers.

Description of Preferred Embodiments

A solder block array 1 formed according to an embodiment of the invention is shown Figures 1, 2, 3a and 3b. The solder block array 1 is to be attached to a replacement device, for example a QFN device, which is to be fitted to a printed circuit board. The array 1 comprises a number of solder blocks 2 mounted in a carrier 4 and laterally spaced from one another to form an array
corresponding to the land pattern for the leads of the replacement device (not shown) and exposed thermal pads (not shown) on the replacement device. The top and bottom surfaces of the solder blocks 2 in the array 1 are each coated with a flux film layer 5, 6 which serves as an adhesive for the replacement device and the land of the printed circuit board.

The top surface of the carrier 4 is fitted with a detachable cover 8 which, as shown in Figure 2, extends over the aperture in the carrier containing the array 1 of solder blocks 2. The top cover 8 may be formed, for example, of paper. The bottom surface of the carrier 4 is also fitted with a detachable cover 10 which could be formed, for example of a plastic or plastics material.

Figures 3a and 3b show alternative layouts for an array 1 of solder blocks 2. The layout and shape of the individual solder blocks will depend on the device for which the array is intended, for example, a QFN device may have an array of solder blocks such as that shown in Figure 3a in which the solder blocks 2 are rectangular in cross-section. A ball grid array is shown in Figure 3b where the solder blocks have a circular cross-section.

As shown in Figure 4, the top cover 8 extending over the solder block array 1 mounted in the carrier 4, may be peeled back to reveal the array 1 of solder blocks 2, before applying the solder array 1 to the replacement device.

Figure 5 shows a QFN device 12 held in a vacuum pick-up head 14 of a re-work system/machine 16. The solder block array 1 is applied to the base of the QFN device 12 and is held therein by the adhesive flux layer 5 on the top surface of the solder blocks 2. The carrier 4 is designed so that the QFN device 12 drops into the aperture in the carrier in which the array 1 of solder blocks 2 is located and the QFN device 12 is thereby aligned over the solder blocks 2. The carrier 4 and bottom cover 10 may be peeled off, as shown in Figure 5, to allow the QFN device 12 with its solder blocks 2 to be positioned
on a PCB (not shown) where it will be held by the flux adhesive layer 6 on the under surface of the solder blocks 2, ready for reflow fixing.

A plurality of arrays 1 of solder blocks 2 in their carriers 4 may be arranged on a sheet of material 18, as shown in Figure 6, for convenient storage. The solder block arrays 1 may be detached from the sheet 18 for use, as required.

In practice, to replace or fix a device 12, such as a QFN device, onto a PCB, a suitable solder block array 1 in its carrier 4 is selected to match the land pattern on the (QFN) device 12. The top cover 8 of the carrier 4 is removed, as shown in Figure 4, and the (QFN) device 12 is then placed in the opening therein which is shaped to receive it, thereby aligning the array 1 of solder blocks 2 with the land pattern and thermal pad on the device 12, as shown in Figure 5. The adhesive flux layer 5 on the upper surface of the solder blocks 2 adheres to the contact lands on the device 12. The pick-up head 14 of the re-work system 16 picks up the device 12 together with the solder blocks 2 in the carrier 4, as shown in Figure 5. The carrier 4, together with the bottom cover 10, are then progressively peeled away from the solder block array 1. Using visual alignment equipment on the rework system 16, the device 12 is placed in the desired position in a PCB. The device 12 is retained in position by the adhesive flux layer 6 on the bottom surface of the solder blocks 2 in the solder block array 1.

A reflow process melts the solder blocks 2 and the flux film layers 5, 6 when heat is introduced, thereby fixing the device to the printed circuit board in a predefined reflow profile to suit the solder block composition. The profile depends on the composition of the solder blocks 2 which may be tin-lead (SnPb) or lead (Pb) free, although any type of solder may be used. The device is then inspected after the completion of the reflow process to ensure that the positioning of the device 12 is as desired and that the solder joints are sound.
As shown in Figure 6, a plurality of solder blocks 2 may be arranged on a sheet of material 18. The solder blocks 2 may be detached from the sheet 18 in a manner similar to that of removing an address label from a sheet of labels.

The systems and methods embodying the present invention may be applied to surface mount devices, such as QFN devices, particularly those that conform to the Jedec Standard of MO220.

In a preferred embodiment, the thickness of the flux film adhesive layers 5, 6 applied to the top and bottom surfaces of the solder blocks 2 is preferably between around 10 to 20 μm. Preferably, the solder blocks 2 have a thickness of between 80 to 100 μm.

Preferred embodiments of the present invention are particularly advantageous over prior art systems which use solder paste printing and mini-stencil techniques. In such prior art systems, it is not generally possible to print on a highly populated PCB land and the manual alignment of manual paste printing requires a high level of skill from the operator. Also, in conventional manual printing techniques, it is difficult to control the thickness consistency of the solder paste. Furthermore, tooling is required in the form of mini stencils and squeegee blades. Such conventional techniques are also time consuming.

One or more preferred embodiments of the invention aim to have better control of the paste thickness and volume than in such prior art techniques, and the alignment of the devices to the pads on the PCB is easier. Also, preferred embodiments of the present invention are much quicker than applying solder paste to a stencil and require much less skill on the part of the operator. Therefore, it is much easier to place the device onto a highly populated PCB as the device is placed in the aligned position using a rework head rather than manually positioning the device on the PCB.
Various modifications to the embodiments of the present invention described above may be made. Therefore, although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to the skilled reader, without departing from the spirit and scope of the invention. In particular, whilst a preferred embodiment of the invention has been described with reference to the placement of QFN devices on a PCB, other semiconductor devices may be used.
Claims

1. A method for attaching a module having an array of contacts thereon arranged in a given pattern to a substrate having an array of contact pads, comprising the steps of:

   applying an array of solder blocks to the array of contacts on said module;

   positioning the module on said substrate so that said array of solder blocks contacts the array of contact pads on the substrate; and

   applying heat to reflow the solder blocks to provide mechanical and electrical connection of the module to said substrate.

2. The method of claim 1, wherein the step of applying an array of solder blocks to the array of contacts on said module comprises applying an array of solder blocks located in an aperture in a carrier to said module.

3. The method of claim 2, wherein the step of applying an array further comprises locating said module in said aperture in said carrier to align said module relative to said array of solder blocks.

4. The method of claim 2, wherein the step of applying an array of solder blocks comprises bringing a first layer of adhesive flux on a first surface of said solder blocks into contact with said array of contacts on said module to adhere said array of solder blocks to said module.

5. The method of claim 4, further comprising the step of removing said carrier after applying said array of solder blocks and before the step of positioning said module on said substrate.

6. The method of claim 1, wherein the step of positioning the module on said substrate comprises bringing a second layer of adhesive flux on a
second surface of said solder blocks into contact with said array of contact pads on said substrate to adhere said array of solder blocks and said module to said substrate.

7. The method of claim 2, wherein the step of applying an array of solder blocks to the array of contacts on said module comprises applying an array of solder blocks located in an aperture in a carrier to said module after removing a cover from said aperture.

8. The method of claim 7, wherein the step of applying an array of solder blocks to the array of contacts on said module comprises applying an array of solder blocks located in an aperture in a carrier after removing said carrier from a sheet of carriers.

9. A method of attaching a semiconductor device having an array of contacts thereon arranged in a given pattern to a printed circuit board having an array of contact pads, comprising the method of claim 1.

10. A method of attaching a Quad Flatpack Nonlead (QFN) device having an array of contacts thereon arranged in a given pattern to a printed circuit board having an array of contact pads, comprising the method of claim 1.

11. A device for attaching a module having an array of contacts thereon arranged in a given pattern to a substrate having an array of contact pads, the device comprising:

   a removable carrier; and

   an array of solder blocks arranged in an aperture in said carrier;

   said aperture being arranged to receive and align said module to align said array of contacts thereon with said array of solder blocks; wherein said
array of solder blocks are arranged to contact said array of contact pads on said substrate after removal of said removable carrier.

12. The device of claim 11, further comprising a first layer of adhesive flux applied to a first surface of said solder blocks in said array of solder blocks for contacting said array of contacts on said module to adhere said array of solder blocks to said module.

13. The device of claim 11, further comprising a second layer of adhesive flux on a second surface of said solder blocks in said array of solder blocks for contacting said array of contact pads on said substrate to adhere said array of solder blocks and said module to said substrate.

14. The device of claim 11, further comprising a first removable cover locatable to cover said aperture in said carrier.

15. The device of claim 14, wherein said first cover is formed of paper.

16. A device according to claim 11 wherein said module comprises a semiconductor device.

17. A device according to claim 11 wherein said module comprises a Quad Flatpack Nonlead (QFN) device.

18. A device according to claim 11 wherein said substrate comprises a printed circuit board.

19. A sheet comprising an array of devices of the type according to claim 11, each of said devices in said array being removable from said sheet.
Figure 4

Opening to provide good alignment between solder block and the leads and pad

carrier

Top cover

Solder block

1 2 3 4 5 6 7 8 9 10
### A. CLASSIFICATION OF SUBJECT MATTER

**IPC 7** H05K3/34

According to International Patent Classification (IPC) or to both national classification and IPC.

### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

**IPC 7** H05K HO1L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched:

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

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**Date of the actual completion of the international search**

14 January 2005

**Date of mailing of the international search report**

21/01/2005

**Name and mailing address of the ISA**

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**Authorized officer**

Kirkwood, J
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