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(54) **Title:** BACK-ILLUMINATED SENSOR AND A METHOD OF MANUFACTURING A SENSOR USING A SILICON ON INSULATOR WAFER

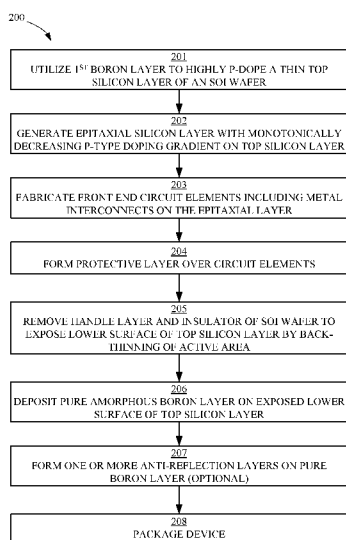


Figure 2

(57) **Abstract:** An image sensor is fabricated by first heavily p-type doping the thin top monocrystalline silicon substrate of an SOI wafer, then forming a relatively lightly p-doped epitaxial layer on a top surface of the top silicon substrate, where p-type doping levels during these two processes are controlled to produce a p-type dopant concentration gradient in the top silicon substrate. Sensing (circuit) elements and associated metal interconnects are fabricated on the epitaxial layer, then the handling substrate and oxide layer of the SOI wafer are at least partially removed to expose a lower surface of either the top silicon substrate or the epitaxial layer, and then a pure boron layer is formed on the exposed lower surface. The p-type dopant concentration gradient monotonically decreases from a maximum level near the top-silicon/epitaxial-layer interface to a minimum concentration level at the epitaxial layer's upper surface.

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BACK-ILLUMINATED SENSOR AND A METHOD OF MANUFACTURING A SENSOR
USING A SILICON ON INSULATOR WAFER

Related Applications/Patents

[0001] This application claims priority from U.S. Provisional Patent Application No. 63/006,724, entitled "BACK-ILLUMINATED SENSOR AND A METHOD OF MANUFACTURING A SENSOR USING A SILICON ON INSULATING WAFER", which was filed on April 8, 2020, and is incorporated by reference herein. This application also is related to U.S. Application Serial No. 16/562,396, entitled "BACK-ILLUMINATED SENSOR AND A METHOD OF MANUFACTURING A SENSOR" filed on September 5, 2019, and to US Patent Nos. 9,496,425, 9,818,887, 10,121,914, and 10,446,696, all to Chern et al., and all entitled "Back-illuminated sensor with boron layer". These patents and applications are incorporated herein by reference.

Field of the Disclosure

[0002] The present application relates to image sensors suitable for sensing radiation in deep UV (DUV) and vacuum UV (VUV) wavelengths, and to methods for making such image sensors. These sensors are suitable for use in photomask, reticle, or wafer inspection systems and for other applications.

Related Art

[0003] The integrated circuit industry requires inspection tools with increasingly higher resolution to resolve ever smaller features of integrated circuits, photomasks, reticles, solar cells, charge coupled devices etc., as well as detect defects whose sizes are of the order of, or smaller than, those feature sizes.

[0004] Inspection systems operating at short wavelengths, e.g. wavelengths shorter than about 250 nm, can provide such resolution in many cases. In particular for photomask or reticle inspection, it is desirable to inspect using a wavelength identical, or close, to the wavelength that will be used for lithography, i.e. close to 193.4 nm for current generation lithography and close to 13.5 nm for future EUV lithography, as the phase-shifts of the inspection light caused by the patterns will be identical or very similar to those caused during lithography. For inspecting semiconductor patterned wafers, inspection systems operating over a relatively broad range of wavelengths, such as a wavelength range that includes wavelengths in the near UV, DUV, and/or VUV ranges, can be advantageous because a broad range of wavelengths can reduce the sensitivity to small changes in layer thicknesses or pattern dimensions that can cause large changes in reflectivity at an individual wavelength.

[0005] In order to detect small defects or particles on photomasks, reticles, and semiconductor wafers, high signal-to-noise ratios are required. High photon flux densities are required to ensure high signal-to-noise ratios when inspecting at high speed because statistical fluctuations in the numbers of photons detected (Poisson noise) is a fundamental limit on the signal-to-noise ratio. In many cases, approximately 100,000 or more photons per pixel are needed. Because inspection systems are typically in use 24 hours per day with only short stoppages, the sensors are exposed to large doses of radiation after only a few months of operation.

[0006] A photon with a vacuum wavelength of 250 nm has energy of approximately 5 eV. The bandgap of silicon dioxide is about

10 eV. Although it may appear such wavelength photons cannot be absorbed by silicon dioxide, silicon dioxide as grown on a silicon surface must have some dangling bonds at the interface with the silicon because the silicon dioxide structure cannot perfectly match that of the silicon crystal. In addition, because the single dioxide is amorphous, there will be dangling bonds within the material. In practice, there will be a non-negligible density of defects and impurities within the oxide, as well as at the interface to underlying semiconductor, that can absorb photons with DUV wavelengths, particularly those shorter than about 250 nm in wavelength. Furthermore, under high radiation flux density, two high-energy photons may arrive near the same location within a very short time interval (nanoseconds or picoseconds), which can lead to electrons being excited to the conduction band of the silicon dioxide by two absorption events in rapid succession or by two-photon absorption.

[0007] A further requirement for sensors used for inspection, metrology and related applications is high sensitivity. As explained above, high signal-to-noise ratios are required. If the sensor does not convert a large fraction of the incident photons into signal, then a higher intensity light source would be required in order to maintain the same inspection or measurement speed compared with an inspection or metrology system with a more efficient sensor. A higher intensity light source would expose the instruments optics and the sample being inspected or measured to higher light intensities, possibly causing damage or degradation over time. A higher intensity light source would also be more expensive or, particularly at DUV and VUV wavelengths, may not be available. Silicon reflects a high percentage of DUV and VUV light incident on it. For example, near 193 nm in wavelength, silicon with a 2 nm oxide

layer on its surface (such as a native oxide layer) reflects approximately 65% of the light incident on it. Growing an oxide layer of about 21nm on the silicon surface reduces the reflectivity to close to 40% for wavelengths near 193 nm. A detector with 40% reflectivity is significantly more efficient than one with 65% reflectivity, but lower reflectivity, and hence higher efficiency, is desirable.

[0008] DUV and VUV wavelengths are strongly absorbed by silicon. Such wavelengths may be mostly absorbed within about 10 nm or a few tens of nm of the surface of the silicon. The efficiency of a sensor operating at DUV or VUV wavelengths depends on how large a fraction of the electrons created by the absorbed photons can be collected before the electrons recombine. Silicon dioxide can form a high-quality interface with silicon with a low density of defects. Most other materials including many of those commonly used for anti-reflection coatings, if deposited directly on silicon, result in a very high density of electrical defects at the surface of silicon. A high density of electrical defects on the surface of silicon may not be an issue for a sensor intended to operate at visible wavelengths, as such wavelengths may typically travel about 100 nm or more into the silicon before being absorbed and may, therefore, be little affected by electrical defects on the silicon surface. However, DUV and VUV wavelengths are absorbed so close to the silicon surface that electrical defects on the surface and/or trapped charges within the layer(s) on the surface can result in a significant fraction of the electrons created recombining at, or near, the silicon surface and being lost, resulting in a low efficiency sensor.

[0009] U.S Patents 9,496,425, 9,818,887 and 10,121,914, all to Chern et al., describe image sensor structures and methods of

making image sensors that include a boron layer deposited on, at least, an exposed back surface of the image sensor. Different ranges of temperature for deposition of the boron are disclosed, including a range of about 400-450°C and a range of about 700-800°C. The inventors have discovered that one advantage of a higher deposition temperature for the boron, such as a deposition temperature between about 600°C and about 900°C, is that at such temperatures boron diffuses into the silicon providing a very thin, heavily p-type doped silicon layer on the light-sensitive back surface. This p-type doped silicon layer is important for ensuring a high quantum efficiency to DUV and VUV radiation because it creates a static electric field near the surface that accelerates electrons away from the surface into the silicon layer. The p-type silicon also increases the conductivity of the back surface of the silicon, which is important for high-speed operation of an image sensor, since a return path is needed for ground currents induced by the switching of signals on electrodes on the front surface of the sensor.

[0010] However, processing temperatures higher than 450°C cannot be used on semiconductor wafers that include conventional CMOS circuits because 450°C is close to the melting point metals such as aluminum and copper commonly used in fabricating CMOS devices. At high temperatures, such as those greater than 450°C, these metals expand, become soft and can delaminate. Furthermore, at high temperatures copper can easily diffuse through silicon which will modify the electrical properties of the CMOS circuits. Thinning a wafer before any metals are deposited on it allows a boron layer to be deposited on the back surface as described in the aforementioned patents at a temperature between 600 and 900°C enabling boron to diffuse into the surface during, or subsequent to, the deposition of the boron

layer. Subsequently metal interconnects can be formed on the front surface. After the image sensor regions of the wafer have been thinned, for example to a thickness of about 25 μm or thinner, the thinned region can be significantly warped and may have peak-to-valley non-flatness of many tens of microns or more. So, it is necessary to use relatively wide metal interconnect lines and vias, such as multiple microns wide or more, to ensure that the lines and vias connect in spite of any misalignment caused by the non-flatness. Such wide metal interconnects and vias increase the capacitance per unit area associated with those lines and vias. Furthermore, wide interconnects and vias can make it difficult, or impossible, to interconnect all the signals on a large area sensor with about one million or more pixels. In some cases, polysilicon jumpers may be needed to connect metal interconnects, but polysilicon has much higher resistivity than any metal, so the use of such jumpers can limit the maximum operating speed of a sensor.

[0011] Therefore, a need arises for an image sensor capable of efficiently detecting high-energy photons without degrading yet overcoming some, or all, of the above disadvantages. In particular, a method of fabricating a back-thinned image sensor with a boron layer and boron doping on its backside surface while allowing formation of metal interconnects on a relatively flat wafer (i.e. with a flatness of about 10 μm or less) would allow the use of finer design rules (such as the design rules corresponding to a 0.35 μm process or finer). Such a method would allow narrower metal lines connecting to critical features such as the floating diffusion, enabling smaller floating-diffusion capacitance and higher charge to voltage conversion efficiencies. Finer design rules also allow more interconnect

lines per unit area of the sensor and allow more flexibility in connecting the circuits on the image sensor.

SUMMARY OF THE DISCLOSURE

[0012] Image sensors and methods of fabricating image sensors with high-quantum-efficiency (high QE) for imaging DUV, VUV, EUV, X-rays and/or charged particles (such as electrons) on SOI wafers are described. These image sensors are capable of long-life operation under high fluxes of radiation. These methods include process steps to form light sensitive active and/or passive circuit elements in a layer of semiconductor material (preferably silicon), as well as forming metal interconnections between the electrical elements of the sensor. These image sensors can include fine metal interconnects and vias (such as those conforming to about 0.35 μm , or finer, design rules), while having a backside surface coated with an amorphous boron layer and having a highly doped p-type silicon layer immediately adjacent to the boron layer. The metal interconnections may comprise tungsten, aluminum, copper or other metals used in fabricating interconnects in known CMOS processes.

[0013] An exemplary method of fabricating an image sensor begins by utilizing a boron layer to highly p-dope the thin top silicon substrate of a silicon on insulator (SOI) wafer, and then generating an epitaxial layer on the top silicon substrate in a manner that generates a monotonically decreasing p-type dopant concentration gradient (doping profile) having a maximum concentration level of p-type dopant (e.g., boron) atoms in the top silicon substrate (i.e., near the bottom of the epitaxial layer) and a minimum concentration level of p-type dopant atoms near the top surface of the epitaxial layer. Doping the thin top silicon substrate is performed, for example, by forming an

amorphous boron layer on the top silicon substrate, performing a boron drive-in anneal at a high temperature (i.e., 800°C or higher), and then removing the boron layer during or after the drive-in anneal (i.e., before forming the epitaxial layer). Generating the epitaxial layer with the desired doping gradient involves growing intrinsic or lightly p-doped epitaxial silicon on the top silicon substrate at the high temperature (i.e., at least 800°C) such that boron diffusion from the highly p-doped thin top silicon into the epitaxial silicon produces the desired p-type dopant concentration gradient in the epitaxial silicon. Circuit elements are then formed on the upper (relatively low p-doped) surface of the epitaxial layer using, for example, standard CMOS fabrication processes, and then metal interconnects (lines and vias) are formed to connect together those circuit elements. Then the thick handling substrate and intermediate insulator layer of the SOI wafer are thinned (i.e., at least partially removed) to expose a backside (lower) surface of either the top silicon substrate or the epitaxial layer to increase the sensitivity of the image sensor to light impinging the active sensor backside surface regions. In some embodiments some or all of the top silicon substrate is removed during the thinning process to maximize the p-type doping level of the exposed backside surface regions. In one embodiment the removal of the handling substrate, insulator/oxide and top silicon substrate is performed using known dry etching, wet etching, and/or mechanical polishing techniques. A permanent (second) amorphous pure boron layer is then formed directly on the exposed backside surface region, and one or more optional anti-reflection layers are formed on the surface of the second amorphous boron layer. In an alternative embodiment, a thin metal coating may be deposited on the boron layer to facilitate the detection of charged particles (e.g., electrons), EUV or X-rays. Such a thin metal coating may

also reduce to sensitivity of the sensor to stray light, may protect the surface of the sensor, and may facilitate in-situ cleaning of contaminants, such as carbon and organic molecules from the sensor surface.

[0014] Another method of fabricating an image sensor involves producing an epitaxial layer having the monotonically decreasing doping concentration gradient described above and then forming circuit elements and interconnects on the epitaxial layer using the processes described above. An optional protective layer is then formed on/over the circuit elements, and then a second handling wafer is bonded over the circuit elements and interconnects. At least a portion of the SOI wafer (i.e., the entire handling substrate, the insulator/oxide layer and some or all the top silicon substrate) are then removed to expose a backside sensor surface formed by either the remaining top silicon substrate or epitaxial layer material, where the exposed backside sensor surface defines a maximum boron doping concentration level of the monotonically decreasing doping concentration gradient (i.e., the boron doping concentration level monotonically decreases from the exposed backside sensor surface and the upper surface of the epitaxial layer on which the circuit elements are formed). The subsequently formed pure boron layer is then deposited at a temperature at or below 450°C by chemical vapor deposition (CVD) or molecular beam epitaxy (MBE), an optional protective layer is then formed, and then one or more anti-reflection coating layers are formed by an atomic-layer deposition (ALD) or other process that can be performed below 450°C in order to prevent heat-related damage to the circuit elements and interconnects.

[0015] The image sensors described herein may be fabricated using CCD (charge coupled device) or CMOS (complementary metal

oxide semiconductor) technology. The image sensors may be two-dimensional (2D) area sensors, or one-dimensional (1D) line sensors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figure 1 is a cross-sectional view showing an exemplary image sensor produced in accordance with the present invention.

[0017] Figure 2 is a flow diagram illustrating an exemplary method for fabricating an image sensor according to an embodiment.

[0018] Figures 3A, 3B, 3C, 3D, 3E, and 3F are cross-sectional side views illustrating exemplary processes utilized to fabricate an image sensor according to the method of Fig. 2.

[0019] Figure 4 is a flow diagram illustrating an exemplary method for fabricating an image sensor according to another embodiment.

[0020] Figures 5A, 5B, 5C, 5D and 5E are cross-sectional side views illustrating exemplary processes utilized to fabricate an image sensor according to the method of Fig. 4.

[0021] Figures 6A, 6B and 6C are cross-sectional side views illustrating exemplary processes utilized to fabricate an image sensor according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0022] Although claimed subject matter will be described in terms of certain embodiments, other embodiments, including embodiments that do not provide all of the benefits and features set forth herein, are also within the scope of this disclosure. Various structural, logical, process step, and electronic changes may be made without departing from the scope of the disclosure. Accordingly, the scope of the disclosure is defined only by reference to the appended claims.

[0023] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure as provided in the context of a particular application and its requirements. As used herein, directional terms such as "top," "bottom," "front," "frontside," "backside," "over," "under," "upper," "upward," and "lower" are intended to provide relative positions for purposes of description and are not intended to designate an absolute frame of reference. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present disclosure is not intended to be limited to the embodiments shown and described but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0024] Fig. 1 is a cross-sectional side view depicting a portion of an image sensor 100 configured to sense deep ultraviolet (DUV) radiation, vacuum ultraviolet (VUV) radiation, extreme ultraviolet (EUV) radiation or charged particles according to an exemplary embodiment of the present invention. Image sensor 100 generally includes a silicon substrate 103, an epitaxial layer 104 disposed on an upper surface 103U of silicon substrate 103, at least one circuit element 110 and associated interconnects 120 disposed on an upper surface 104U of epitaxial layer 104, a pure boron layer 106 disposed on a lower surface 103L of silicon substrate 103, and an optional anti-reflection coating 108 disposed on a lower (backside or outward-facing) surface 106L of pure boron layer 106.

[0025] Silicon substrate 103 is a relatively heavily p-doped monocrystalline silicon layer having an upper surface 103U that forms a silicon-substrate/epitaxial-layer interface with a lower

surface 104L of epitaxial layer 104, and a lower surface 103L of silicon substrate 103 forms a silicon/boron interface with an upper surface 106U of pure boron layer 106. In one embodiment a thickness T1 of silicon substrate 103 is in a range of 5 nm to 100 nm.

[0026] Epitaxial layer 104 is a layer of monocrystalline silicon that is homoepitaxially grown other otherwise formed on upper surface 103U using fabrication techniques described below. In one embodiment, epitaxial layer 104 has a thickness T2 in the range of 10 μm to 40 μm .

[0027] Circuit element 110 and interconnects 120 are formed on (i.e., into and/or over) an upper surface 104U of epitaxial layer 104 using known semiconductor fabrication techniques, and include a sensor device (e.g., a light sensitive device such as a photodiode) and associated control transistors. As used herein, the phrase "circuit element" refers to light sensitive devices such as charge-coupled devices and photodiodes, other semiconductor devices such as transistors, diodes, resistors and capacitors, and the term "interconnects" refers to electrical interconnections (often called metal lines and vias) that pass signals between semiconductor devices. The circuit elements mentioned herein are formed using standard semiconductor manufacturing processes including, but not limited to, photolithography, deposition, etching, diffusion, ion implantation, and annealing. In the exemplary embodiment depicted in Fig. 1, circuit element 110 includes spaced-apart n⁺ doped diffusion regions 111-11, 111-12 and 111-12 that extend from upper surface 104U into corresponding portions of epitaxial layer 104, and polycrystalline silicon (polysilicon) gate structures 113-21 and 113-22 that are respectively separated from

upper surface 104U by intervening gate oxide layers. Interconnects 120 include first metal lines 121 formed in/on a first dielectric region 122, second metal lines 123 formed in a second dielectric layer 124, first metal vias 125 and second metal vias 127, all of which being formed over circuit element 110 and are operably electrically connected to associated regions of circuit element 110 using known techniques. First metal lines 111 are formed in or on one or more dielectric layers 112 deposited over circuit element 110, and first metal vias 115 extend through dielectric layers 112 using known via formation techniques. Second metal lines 123 are formed in one or more second dielectric layers 124 that are disposed over first metal lines 111, and second metal vias 127 extend through one or both dielectric layers 112 and 122. In one embodiment, a protection layer (not shown in Fig. 1) is formed between first metal lines 121 and second metal lines 123, and all second metal vias 127 comprise at least one of tungsten, aluminum and copper and extend through this protection layer. The exemplary diffusion regions and gate structures forming circuit element 110 depicted in Fig. 1, along with the exemplary metal interconnects 120, are arbitrarily configured for illustrative purposes and provided solely to for purposes of describing exemplary circuit element structures and is not intended to represent a functional sensor device or to limit the appended claims.

[0028] Pure boron layer 106 and optional anti-reflection coating 108 are formed using techniques described below during backside processing performed after the formation of circuit elements 110 and interconnects 120. Pure boron layer 106 comprises a boron concentration of 80% or higher with inter-diffused silicon atoms and oxygen atoms predominantly making up the remaining 20% or less. In one embodiment pure boron layer

106 has a thickness T3 in the range of 2 nm to 20 nm. In one specific embodiment, thickness T3 of pure boron layer 106 is in the range of 3 nm to 10 nm, and an optional protective layer (e.g., a thin metal layer, not shown) and one or more anti-reflection coating (e.g., silicon dioxide) layers 108 are deposited on a lower (outward-facing) surface 106L of pure boron layer 106. Additional structures and details regarding image sensors produced in accordance with the present invention are provided in the following exemplary production method descriptions.

[0029] Referring to right side of Fig. 1, according to an aspect of the invention, silicon substrate 103 and epitaxial layer 104 are processed using methods described below to exhibit a p-type (e.g., boron) dopant concentration gradient d_{np} having a maximum concentration level n_{p-max} that occurs at a backside sensor surface, which in the depicted embodiment coincides with lower surface 103L of silicon substrate 103, and monotonically decreases in the Y-axis direction from maximum concentration level n_{p-max} to a minimum doping concentration level n_{p-min} occurring at upper surface 104U of epitaxial layer 104. In one embodiment, maximum concentration level n_{p-max} is in a range of about 10^{18} cm^{-3} (i.e., 10^{18} boron atoms per cubic centimeter) to 10^{21} cm^{-3} , and minimum doping concentration level n_{p-min} is in a range of about 10^{13} cm^{-3} to 10^{14} cm^{-3} . In one embodiment, the portion of dopant concentration gradient d_{np} generated within silicon substrate 103 is substantially flat (i.e., such that an intermediate dopant level n_{p-int} occurring at the silicon-substrate/epitaxial-layer interface defined by lower surface 104L and upper surface 103U is substantially equal to maximum concentration level n_{p-max} at lower surface 103L.

[0030] FIG. 2 illustrates an exemplary method 200 for fabricating an image sensor using a silicon on insulator (SOI) wafer, and Figs. 3A to 3F depict an exemplary SOI wafer at various process stages during the execution of method 200. Referring to Fig. 3A, at the beginning of the fabrication process SOI wafer 300 includes a relatively thin top (frontside) silicon substrate 303 having an exposed upper (first) surface 303U and an opposing lower (second) surface 303L that is attached to a relatively thick handling substrate 301 by way of an intervening insulator (oxide) layer 302. SOI wafer 300 is fabricated or procured prior to the beginning of the fabrication process, with handling wafer 301 and oxide layer 302 having standard compositions and thicknesses. In preferred embodiments SOI wafer 300 is characterized such that top silicon substrate 303 has a thickness in the range of 5 to 100 nm and consists of either intrinsic or lightly p-type doped monocrystalline silicon.

[0031] Referring to block 201 (Fig. 2), a boron layer is utilized to generate a high boron doping concentration level (i.e., 10^{18} cm⁻³ or greater) in the top silicon substrate of an SOI wafer by way of a boron diffusion process. In an embodiment depicted in Figs. 3A and 3B, utilization of a boron layer 310 to produce the desired high boron doping concentration level in the top silicon substrate of SOI wafer 300 includes forming first boron layer 310 (shown and described with reference to Fig. 3A) and then processing SOI wafer 300 (shown and described with reference to Fig. 3B) to perform both boron drive-in and boron removal either sequentially or simultaneously.

[0032] Referring to Fig. 3A, boron layer 310 is formed on upper surface 303U and comprises pure amorphous boron (as defined herein) having a thickness T4 in the range of 2 nm to 10 nm. In a preferred embodiment, boron layer 310 is formed using a

chemical vapor deposition (CVD) process while SOI wafer 300 is disposed in a CVD chamber and heated to a high temperature in a range of 600°C to 800°C. In other embodiments, other processes may be utilized to generate boron layer 310 (e.g., sputtering or a molecular beam epitaxy (MBE)), provided the resulting boron deposition is pure and clean.

[0033] Fig. 3B depicts SOI wafer 300 during or after the processing used to both generate the desired high boron doping concentration level and to completely remove boron layer 310 from upper surface 303U. Note that the top silicon substrate is identified using reference number 303A in Fig. 3B, where the suffix "A" is utilized to distinguish the highly p-doped silicon resulting from the boron diffusion process from the initially lightly doped top silicon substrate 303 of Fig. 3A. In a preferred embodiment, the boron diffusion is performed in situ (e.g., using the same CVD chamber utilized to form boron layer 310) using a CVD boron drive-in anneal process performed at a temperature in the range of 800°C to 900°C. In other embodiments the boron may be driven in at high temperature using any clean chamber in an H₂ or N₂ atmosphere. In a preferred embodiment, boron removal is also performed in situ immediately after boron deposition (i.e., simultaneously with the boron drive-in) in a hydrogen environment at a temperature in a range of 800°C to 900°C, whereby boron diffuses through upper surface 303U into top silicon substrate 303A while the exposed portion of boron layer 310 reacts with the hydrogen and leaves the boron layer's surface. Under these conditions, a typical removal rate of boron layer 310 is 3 nm to 5 nm in a period of 30 to 60 minutes (i.e., thinner boron layers require less than 30 minutes and thicker layers require more than one hour). After boron layer 310 has completely disappeared, top silicon substrate 303A is highly

doped (e.g., with a boron concentration level in the range of 10^{18} to 10^{21} cm^{-3} and the dopant profile will be relatively uniform. A benefit provided by performing both boron layer formation and processing (i.e., drive-in and removal) in situ is that epitaxial growth (described below with reference to Fig. 3C) can be performed immediately after completing boron layer removal (i.e., without requiring an additional cleaning process). In an alternative embodiment, SOI wafer 310 is removed from the deposition/diffusion chamber and boron layer 310 is removed using nitric acid dip (or other oxidizing dip), then epitaxial growth is performed after carrying out after cleaning oxides from upper surface 303U.

[0034] Referring to block 202 (Fig. 2), an epitaxial silicon layer is then generated on/over the top silicon substrate in a manner that provides the epitaxial layer with a monotonically decreasing boron concentration gradient (e.g., gradient d_{np} shown and described above with reference to Fig. 1). In one embodiment, intrinsic or lightly p-doped epitaxial silicon is grown on the upper surface of the heavily doped top silicon substrate under conditions that enhance boron diffusion from the top silicon substrate into the epitaxial layer material at a rate that produces the desired monotonically decreasing boron concentration gradient. FIG. 3C illustrates the SOI wafer after epitaxial layer 304 is formed on/over upper surface 303U during which a secondary boron diffusion generates the desired doping gradient (e.g., gradient d_{np} , described with reference to Fig. 1). Note that the suffix "B" is used to indicate the difference between top silicon substrate 303B after the secondary boron diffusion and heavily p-doped top silicon substrate 303A (Fig. 3B). In one preferred embodiment epitaxial layer 304 is grown in situ immediately after removal of the boron layer using the

decomposition of at least one of a silane or a chlorosilane gas (e.g. SiH_4 , SiCl_4 , SiHCl_3 , SiH_2Cl_2 or SiH_3Cl) with hydrogen at a temperatures in a range of 800°C to 1250°C in a CVD process. Diborane may be added to the gas mixture for low p-type doping in the epitaxial layer during the CVD process. In some embodiments the silicon epitaxy may be performed using molecular beam epitaxy (MBE). In some embodiments a drive-in anneal at a temperature greater than 800°C may be performed after the epitaxial silicon growth to cause p-type dopant (e.g., boron) atoms to migrate (diffuse) from the heavily p-doped top silicon substrate into epitaxial layer 304 to create the desired monotonically decreasing doping concentration gradient from top silicon substrate 303B into epitaxial layer 304.

[0035] Referring to block 203 (Fig. 2) and Fig. 3D, frontside circuit structures (elements) 110 and associated interconnects 120 are then fabricated on/over the epitaxial layer 304 using standard semiconductor fabrication processes, such as lithography, deposition, etching, ion-implantation, and annealing. The purpose and additional details related to these elements and interconnects are provided above with reference to Fig. 1, so details are omitted here for brevity. Charge-coupled device (CCD) and/or CMOS sensor elements and devices may also be created during the fabrication process of block 203. The frontside elements and devices are created in epitaxial layer 304 on the front side of the SOI wafer, and therefore are referred to as frontside circuit elements. During frontside processing the formation of poly-Si interconnects and metal interconnects may also be performed along with other high temperature processes. Because interconnects 120 are formed on the wafer prior to the back-thinning process (described below), these interconnects can be formed using normal sub-micron CMOS processing techniques and

may include multiple layers of high-density metal interconnects. The interconnects may be formed by Al, Cu, or another metal.

[0036] Referring to block 204 (Fig. 2), an optional protective layer is formed over the circuit elements to protect them during subsequent processing (described below). Referring to the upper portion of Fig. 3E, protective layer 310 is indicated as being formed over interconnects 120. In some embodiments protective layer 320 may comprise a silicon nitride layer deposited using plasma enhanced chemical vapor deposition (PECVD), among many other materials.

[0037] Referring to block 205 (Fig. 2) and Fig. 3E, a backside thinning process is then performed to remove (thin) at least a portion of the handling silicon substrate and at least a portion of oxide layer to expose lower surface 303L of top silicon substrate 303B in a photoactive area of the image sensor. In the depicted embodiment this removal (thinning) process is performed by grinding and/or etching handling and oxide material to expose a portion of lower surface 303L, which represents the backside sensor surface (i.e., the light sensitive area of the back illuminated image sensor), while retaining residual handling wafer portions 301A and residual oxide layer portions 302A around exposed lower surface 303L of top silicon substrate 303B. The etching can be performed by wet etching methods using alkaline solutions such as KOH or TMAH among others. The silicon substrate-oxide interface between the handling substrate and the oxide layer acts a natural etch stop for wet etching. The oxide layer can be removed using hydrofluoric acid and/or buffered oxide etch. The top silicon-oxide interface between the top silicon substrate and the oxide layer acts as a natural etch stop for the oxide etch. Alternatively, the silicon and oxide layers can also be removed using dry etching methods such as reactive

ion etching (RIE) and/or inductively coupled plasma reactive ion etching (ICPRIE) with etching gases such as SF₆, O₂, and C₄F₈ etc. among others. As described below with reference to Figs. 6A to 6C, some or all of the top silicon substrate may also be removed during the thinning process, whereby the backside sensor surface would be formed by epitaxial layer 304.

[0038] Referring to block 206 (Fig. 2) and Fig. 3F, a pure boron layer 306 and an optional antireflection layer (not shown) are then deposited over the exposed lower surface 303L of top silicon substrate 303B (or, alternatively, the exposed lower surface of epitaxial layer 304 where top silicon substrate 303B has been removed). In preferred embodiments lower surface 303L is cleaned and prepared before performing the boron deposition. In one embodiment this cleaning can be performed using standard RCA 1 and 2 cleaning processes with dilute HF or buffered oxide etch to remove the surface oxide after RCA 1 and 2 cleans. In preferred embodiments the high purity boron deposition is performed using a combination of diborane and hydrogen at a low temperature (i.e., less than 450°C, such as a temperature in a range of 300°C to 450°C) to avoid any damage to the frontside metal interconnects in a CVD process. The thickness of boron layer 306 is determined based on the target wavelength range of operation of the completed image sensor and the minimum thickness needed to avoid pin holes. Typical thicknesses may range between 2-20 nm. The time for which the wafer is kept at elevated temperatures must be kept to a minimum to avoid damage of the frontside metal interconnects.

[0039] As indicated in block 208 (bottom of Fig. 2), the completed image sensor is then packaged in some embodiments. The package may include flip-chip bonding or wire bonding of a chip to a substrate. The package may include a window that transmits

wavelengths of interest or may comprise a flange or seal for interface to a vacuum seal. In electron-bombarded image sensor embodiments, the package may include other components such as a photocathode as well as a sealed, evacuated tube.

[0040] FIG. 4 illustrates an alternative exemplary method 400 for fabricating an image sensor starting with a silicon on insulator (SOI) wafer, and Figs. 5A to 5E depict an exemplary SOI wafer at various process stages during the execution of method 400. For brevity, processes and structures generated by method 400 that are substantially identical to those described above with reference to process 200 (Figs. 2 and 3A-3C) are incorporated into Figs. 5A to 5E. For example, Fig. 5A depicts the processed layers of SOI wafer 300 after the completion of processes associated with blocks 301 and 302 (Fig. 3) and blocks 401 and 402 (Fig. 4), where top Si layer 303B is connected to Si handling substrate 301 by way of intervening oxide (insulator) layer 302, epitaxial layer 304 is formed on top silicon substrate 303B in a manner that generates the monotonically changing doping concentration gradient described above. The description provided above with reference to Figs. 3A and 3B is understood as describing similar exemplary processes performed in association with blocks 401 and 402, and therefore will not be repeated here. Similarly, Fig. 5A depicts circuit elements 110 and interconnects 120 that are formed on upper surface 304U of epitaxial layer 304 according to block 303 (Fig. 3) and block 403 (Fig. 4).

[0041] Referring to block 404 (Fig. 4) and Fig. 5A, a frontside protection material (e.g., silicon nitride) is deposited or otherwise formed using known fabrication processes (e.g., PECVD) on upper surface 120U over interconnects 120, which were previously fabricated on epitaxial layer 304 in the manner described above with reference to Fig. 3C.

[0042] Referring to block 405 (Fig. 4) and Fig. 5B, a handling wafer (second handling substrate) 501 is then attached to the frontside (e.g., to upper surface 510U of protective layer 510) using known techniques, whereby handling wafer 501 functions to further protect the elements and interconnects formed on epitaxial layer 304 and to serve as a base wafer for the backside processing stages described below. In exemplary embodiments, handling wafer 501 comprises a silicon wafer, a quartz wafer, or a wafer made of another suitable material. In some embodiments handling wafer 501 may be attached directly to upper surface 120U (i.e., by omitting intervening protection layer 510). In an alternative embodiment (not shown), protective layer 510 can be used instead of, or in addition to, handling wafer 501 (i.e., a second handling substrate may be omitted). In one embodiment, additional via structures (not shown) are formed through handling wafer 501 to facilitate frontside connection to circuit elements 110.

[0043] Referring to block 406 (Fig. 4) and Fig. 5C, backside processing is then performed to (at least partially) remove the handling substrate and oxide layer of the starting SOI wafer such that a backside sensor surface (e.g., lower surface 303L of top silicon substrate 303B) is exposed. In one embodiment the removal process is performed using a combination of grinding and/or etching processes described above with reference to Fig. 3E, including cleaning and processing of lower surface 303L in preparation for the subsequent boron layer formation. In this step, some or all of the top silicon substrate 303B may be removed by, for example, etching or polishing.

[0044] Referring to block 407 (Fig. 4) and Fig. 5D, a pure boron layer 506 is then formed on lower surface 303L of top

silicon substrate 303B, for example, using the processes described above with reference to Fig. 3F.

[0045] Referring to Fig. 408 (Fig. 4) and Fig. 5E, an anti-reflective material is deposited or otherwise formed on lower surface 506L of pure boron layer 506 to produce one or more anti-reflective layers 508. At least one of the layers may be deposited using an ALD process or other process that require temperatures below 450°C. In an alternative embodiment, a thin metal coating may be deposited on boron layer 506 (i.e., in place of or in addition to anti-reflective layer 508). The thin metal coating may be particularly useful when the sensor is used to detect charged particles (such as electrons), EUV or X-rays. Such a thin metal coating may reduce to sensitivity of the sensor to stray light, may protect the surface of the sensor, and may facilitate in-situ cleaning of contaminants, such as carbon and organic molecules from the sensor surface.

[0046] As indicated in block 409 (Fig. 4), the completed image sensor shown in Fig. 5E can then be packaged using any of the packaging techniques described above.

[0047] Figs. 6A to 6C illustrate exemplary conditions under which a doping profile generated in the top silicon substrate requires the removal of some or all of the top silicon substrate (i.e., along with the handling substrate and oxide layer of the original SOI wafer) during the backside thinning processes described above with reference to Figs. 3E and 5C. That is, referring briefly to Fig. 1, an exemplary ideal top silicon doping profile is depicted by the portion of gradient dn_p extending between maximum boron concentration level n_{p-max} and intermediate doping concentration n_{p-int} , where maximum boron

concentration level n_{p-max} occurs at lower surface 103U and the doping concentration monotonically decreases (or remains flat) between lower surface 103U and the top-silicon/epitaxial layer interface. When this ideal top silicon doping profile is generated, the backside thinning process may be terminated after the handling substrate and oxide layer of the SOI wafer are removed (i.e., without having to remove any of the top silicon substrate). However, in reality, the maximum boron concentration level occurs somewhere between the upper and lower surfaces of the top silicon substrate, which requires the removal of at least some of the top silicon substrate, as described below with reference to Figs. 6B and 6C.

[0048] Fig. 6A depicts a partially completed sensor 600A formed on an SOI wafer having a top silicon substrate 603 that is attached to a handling substrate 601 by way of an intervening insulator (oxide) layer 602 after a boron layer (not shown) has been utilized to a high boron doping concentration level in top silicon substrate 603, and after epitaxial layer 604 has been formed on top silicon substrate 603 such that boron diffusion from said top silicon substrate 603 generates a boron doping concentration gradient d_{np1} that monotonically decreases in the epitaxial layer 604 from an original maximum boron concentration level $n_{p-max10}$ disposed adjacent to upper surface 603U of top silicon substrate 603 to a minimum boron doping concentration level n_{p-min1} disposed adjacent to upper surface 604U of epitaxial layer 604. Note however, that maximum boron concentration level $n_{p-max10}$ occurs at a level located between upper surface 603U and original lower surface 603L0 of top silicon substrate 603, which means that boron doping concentration gradient d_{np1} fails to monotonically decrease between original lower surface 603L0 of top silicon substrate 603 and upper surface 604U of epitaxial

layer 604, as is required for optimal sensor performance in some cases. Specifically, a first intermediate boron concentration level $n_{p-int11}$ occurring at upper surface 603U and a second boron concentration level $n_{p-int12}$ occurring at original lower surface 603L0 are less than maximum boron concentration level $n_{p-max10}$. The "dip" (i.e., the small decreased in concentration gradient levels between maximum boron concentration level $n_{p-max10}$ and second boron concentration level $n_{p-int12}$) occurs, for example, due to downward boron diffusion from top silicon substrate 603 into oxide layer 602 during epitaxial silicon growth, and the Y-axis location in which this dip occurs depends on, for example, the peak boron concentration level and the temperature during epitaxial silicon growth.

[0049] Referring to Fig. 6B, in order to "fix" doping concentration gradient d_{np1} , it is necessary to perform backside processing such that the thinning process includes the removal of at least the portion of top silicon layer 603 located between maximum boron concentration level $n_{p-max10}$ and original lower surface 603L0 (i.e., along with the entirety of handle substrate 601 and oxide layer 602), whereby maximum boron concentration level $n_{p-max10}$ coincides with revised lower surface 603L1. That is, removing the depicted lower portion of top silicon layer 603 effectively adjusts doping concentration gradient d_{np1} such that maximum boron concentration level $n_{p-max10}$ occurs the backside sensor surface (i.e., revised lower surface 603L1) and monotonically decreases in the Y-axis direction to upper surface 604U. As described above, backside processing is immediately followed by the deposition of boron on revised lower surface 603L1 and the additional processes described above with reference to blocks 206 to 208 of Fig. 2 and blocks 407 to 409 of Fig. 4.

[0050] Fig. 6C depicts and alternative approach to fixing doping concentration gradient d_{np1} , where backside processing is performed such that the thinning process includes the removal of the entirety of top silicon layer 603 (i.e., along with the entirety of handle substrate 601 and oxide layer 602), whereby the new backside sensor surface is defined by exposing lower surface 604L of epitaxial layer 604. Doping concentration gradient d_{np1} is thus "fixed" in that it has a new maximum boron concentration level $n_{p-max11}$, which is equal to boron concentration level $n_{p-int11}$, and monotonically decreases in the Y-axis direction from the new backside sensor surface (i.e., lower surface 604L) to upper surface 604U. Once top silicon layer 603 has been entirely removed, boron is deposited on exposed lower surface 604L, and the additional processes described above with reference to blocks 206 to 208 of Fig. 2 and blocks 407 to 409 of Fig. 4 are performed.

[0051] The above examples are not meant to limit the scope of the invention disclosed herein. They are meant merely as illustrations of how the top silicon substrate of an SOI wafer may be processed to include both the desired p-type dopant concentration gradient and then coated with a boron layer on its photo-sensitive surface. Because the top silicon substrate includes a concentration gradient of the p-type dopant which has its maximum value adjacent to the boron, the image sensor has high efficiency even for short-wavelength light, or low-energy charged particles, which may penetrate only a few nm, or a few tens of nm into the top silicon and epitaxial layers.

[0052] The various embodiments of the structures and methods of this invention that are described above are illustrative only of the principles of this invention and are not intended to limit the scope of the invention to the particular embodiments

described. For example, additional steps may be added to the flow chart depicted in Figures 2 and 4, or some of the steps shown may be done in a different sequence than shown. Thus, the invention is limited only by the following claims and their equivalents.

CLAIMS

1. A method of fabricating an image sensor on a silicon-on-insulator (SOI) wafer including a top silicon substrate having an exposed first surface and an opposing second surface that is attached to a handling substrate by way of an intervening insulator layer, the method comprising:

utilizing a first boron layer to generate a first boron doping concentration level in the top silicon substrate;

generating an epitaxial layer on a first surface of the top silicon substrate;

forming circuit elements on a first surface of the epitaxial layer;

removing the handling substrate and the intervening insulator layer such that the second surface of the top silicon substrate is exposed; and

forming a pure boron layer on the exposed second surface of the top silicon substrate,

wherein utilizing the boron layer and generating said epitaxial layer are collectively performed such that boron diffusion from said top silicon substrate into the epitaxial layer generates a boron doping concentration gradient that monotonically decreases from a maximum boron concentration level disposed within the top silicon substrate to a minimum boron doping concentration level adjacent to the first surface of the epitaxial layer.

2. The method of claim 1, wherein utilizing the amorphous boron layer to generate said first boron concentration level comprises:

forming a first boron layer on the first surface top silicon substrate;

processing the SOI wafer such that boron diffusion from the first boron layer generates an initial boron doping concentration level in the top silicon substrate, and such that the first boron layer is entirely removed from the first surface of the top silicon substrate.

3. The method of claim 2, wherein forming said first boron layer comprises depositing boron using a CVD process at a temperature in a range of 600°C to 800°C.

4. The method of claim 2, wherein processing to generate said initial boron doping concentration level comprises performing a drive-in anneal at a temperature in a range of 800°C to 900°C.

5. The method of claim 2, wherein processing to remove said first boron layer comprises maintaining the SOI wafer in a hydrogen atmosphere at a temperature in a range of 800°C to 900°C.

6. The method of claim 5, wherein said processing comprises simultaneously generating said initial boron doping concentration level and removing said first boron layer.

7. The method of claim 2, wherein each of forming said first boron layer, performing said drive-in anneal, removing said first boron layer, and generating said epitaxial layer is performed while said SOI wafer is maintained within a CVD chamber.

8. The method of claim 1, wherein the method further comprises depositing an anti-reflection layer on a surface of the pure boron layer.

9. The method of claim 1, wherein the method further comprises forming a protective layer on the epitaxial layer over the circuit elements prior to removing said handling substrate and said intervening insulator layer.

10. The method of claim 1, wherein the method further comprises attaching a second handling substrate to the epitaxial layer over the circuit elements prior to removing said handling substrate and the intervening insulator layer.

11. The method of claim 1, wherein removing the handling substrate and the intervening insulator layer further comprises removing a portion of the top silicon substrate.

12. A method of fabricating an image sensor on a silicon-on-insulator (SOI) wafer including a top silicon substrate having an exposed first surface and an opposing second surface that is attached to a handling substrate by way of an intervening insulator layer, the method comprising:

utilizing a first boron layer to generate a first boron doping concentration level in the top silicon substrate;

generating an epitaxial layer on a first surface of the top silicon substrate such that boron diffusion from said top silicon substrate generates a boron doping concentration gradient that monotonically decreases in the epitaxial layer from a maximum boron concentration level disposed adjacent to the first surface of the top silicon substrate to a minimum boron doping

concentration level disposed adjacent to a second surface of the epitaxial layer;

forming circuit elements on the second surface of the epitaxial layer;

removing the handling substrate, the intervening insulator layer and the top silicon substrate such that a third surface of the epitaxial layer is exposed; and

forming a pure boron layer on the exposed third surface of the epitaxial layer.

13. The method of claim 12, wherein utilizing the amorphous boron layer to generate said first boron concentration level comprises:

forming a first boron layer on the first surface top silicon substrate;

processing the SOI wafer such that boron diffusion from the first boron layer generates an initial boron doping concentration level in the top silicon substrate, and such that the first boron layer is entirely removed from the first surface of the top silicon substrate.

14. The method of claim 13, wherein forming said first boron layer comprises depositing boron using a CVD process at a temperature in a range of 600°C to 800°C.

15. The method of claim 13, wherein processing to generate said initial boron doping concentration level comprises performing a drive-in anneal at a temperature in a range of 800°C to 900°C.

16. The method of claim 13, wherein processing to remove said first boron layer comprises maintaining the SOI wafer in a

hydrogen atmosphere at a temperature in a range of 800°C to 900°C.

17. The method of claim 13, wherein said processing comprises simultaneously generating said initial boron doping concentration level and removing said first boron layer.

18. The method of claim 13, wherein each of forming said first boron layer, performing said drive-in anneal, removing said first boron layer, and generating said epitaxial layer is performed while said SOI wafer is maintained within a CVD chamber.

19. The method of claim 12, wherein the method further comprises depositing one of an anti-reflection layer on a surface of the pure boron layer.

20. An image sensor for sensing at least one of deep ultraviolet (DUV) radiation, vacuum ultraviolet (VUV) radiation, extreme ultraviolet (EUV) radiation, and charged particles, the image sensor comprising:

a monocrystalline silicon substrate having a first surface and an opposing second surface;

an epitaxial layer having a third surface forming an interface with the first surface of the monocrystalline silicon substrate 103, said epitaxial layer having a fourth surface disposed opposite to the third surface;

circuit elements and metal interconnects formed on the fourth surface of the epitaxial layer; and

a pure boron layer formed on the second surface of the monocrystalline silicon substrate 103,

wherein said monocrystalline silicon substrate and said epitaxial layer collectively includes a boron concentration gradient configured such that a concentration of boron atoms monotonically decreases from a highest boron concentration level occurring at the second surface of the monocrystalline silicon substrate to a lowest boron concentration level at the fourth surface of the epitaxial layer.

21. The image sensor of claim 20,

wherein a thickness of the monocrystalline silicon substrate measured between the first and second surfaces is in the range of 5 nm to 100 nm,

wherein a thickness of the epitaxial layer measured between the third and fourth surfaces is in the range of 10 μm to 40 μm , and

wherein the pure boron layer has a thickness in the range of 2 nm to 20 nm.

22. The image sensor of claim 20, further comprising a handling wafer attached to the epitaxial layer over the circuit elements.

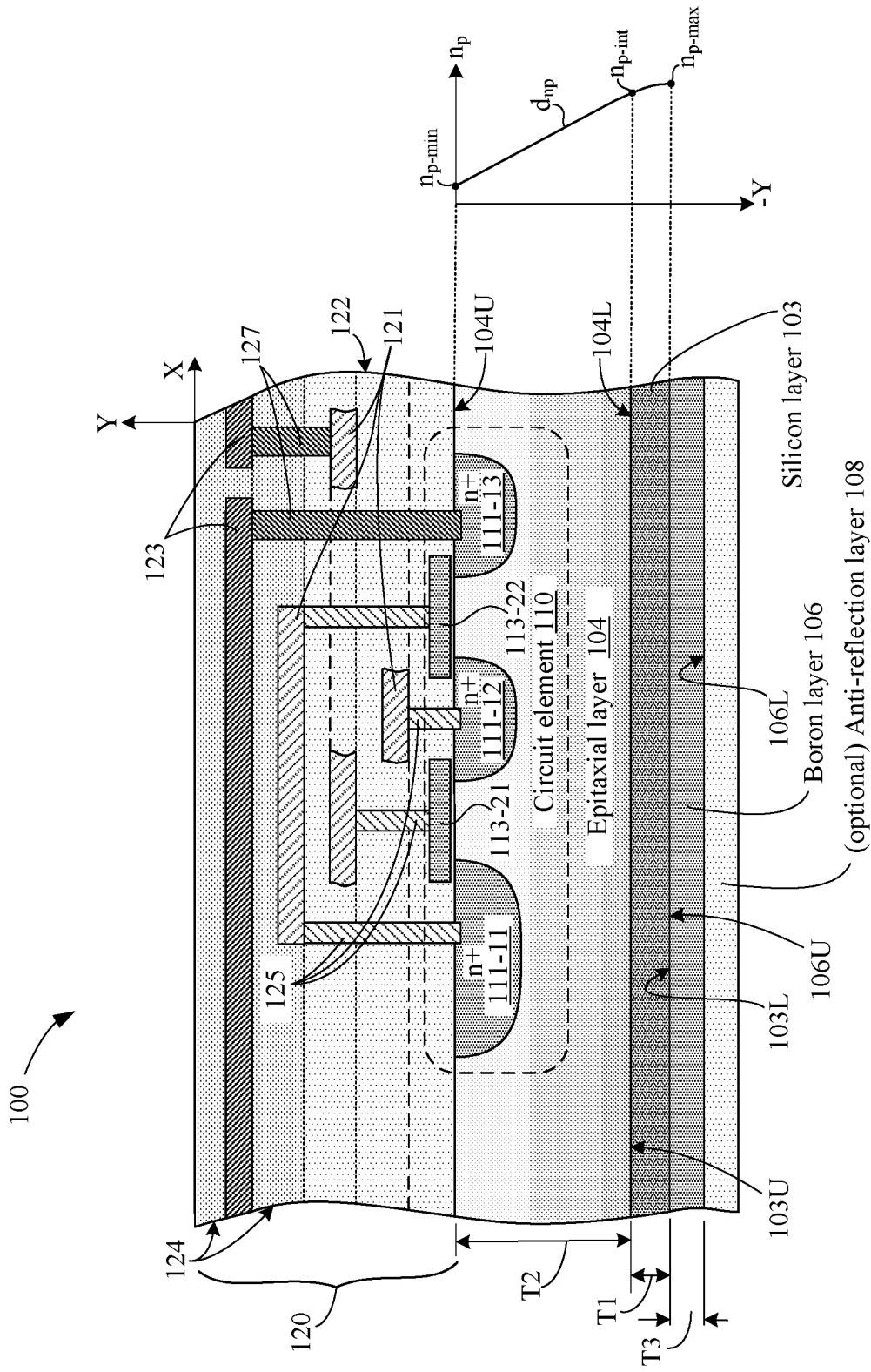


Figure 1

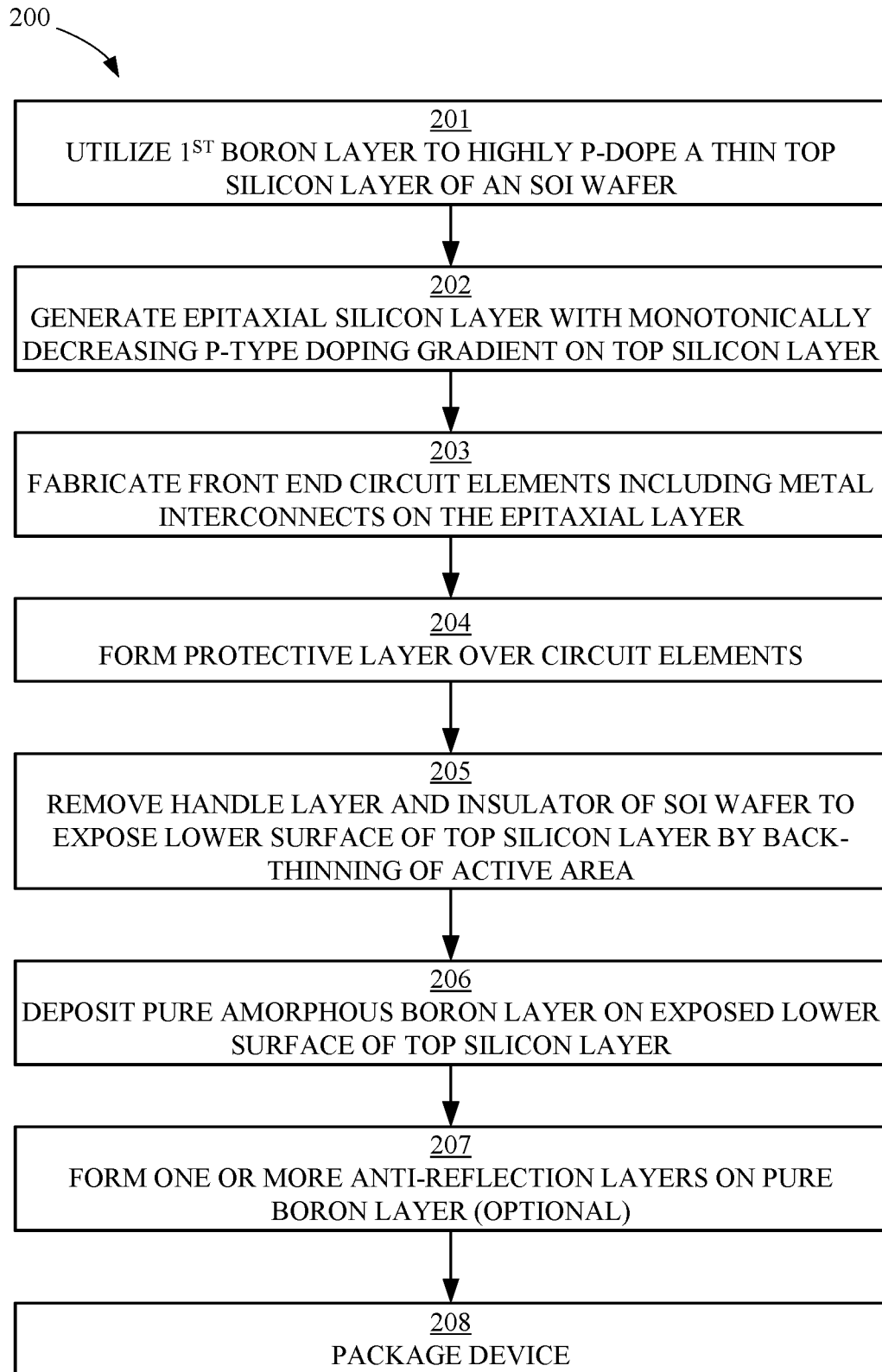


Figure 2

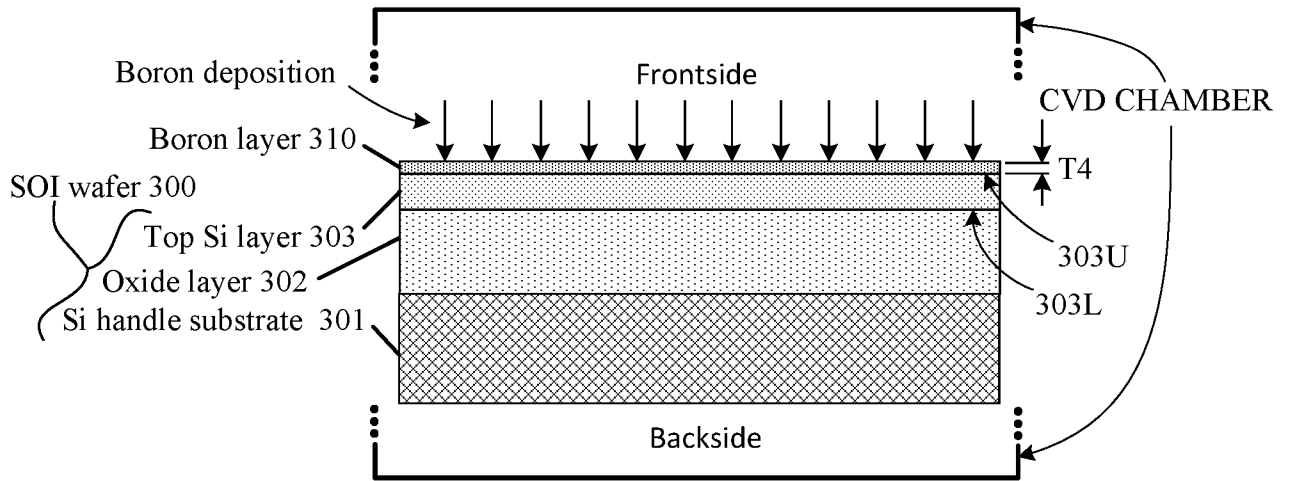


Figure 3A

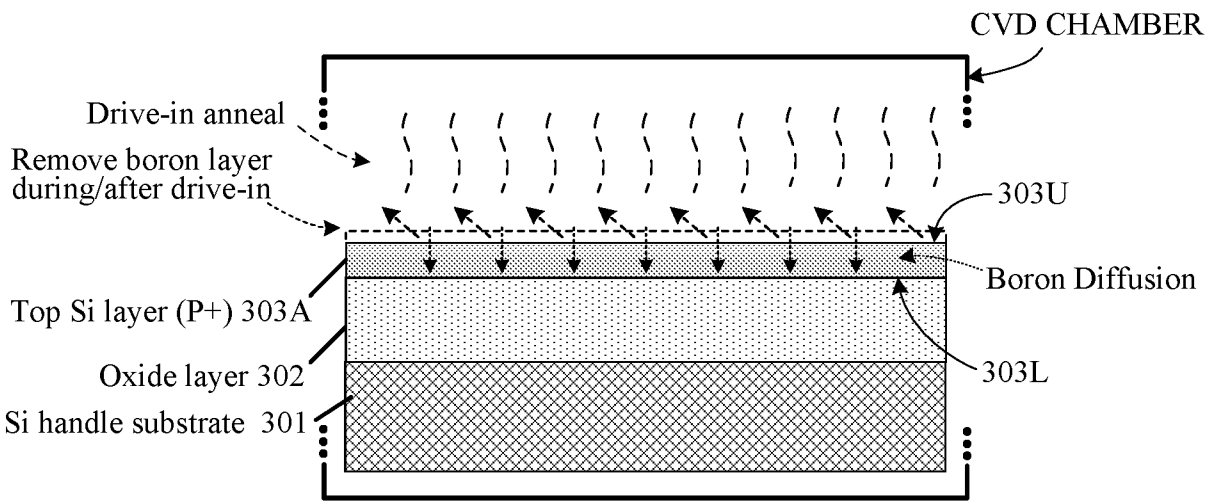


Figure 3B

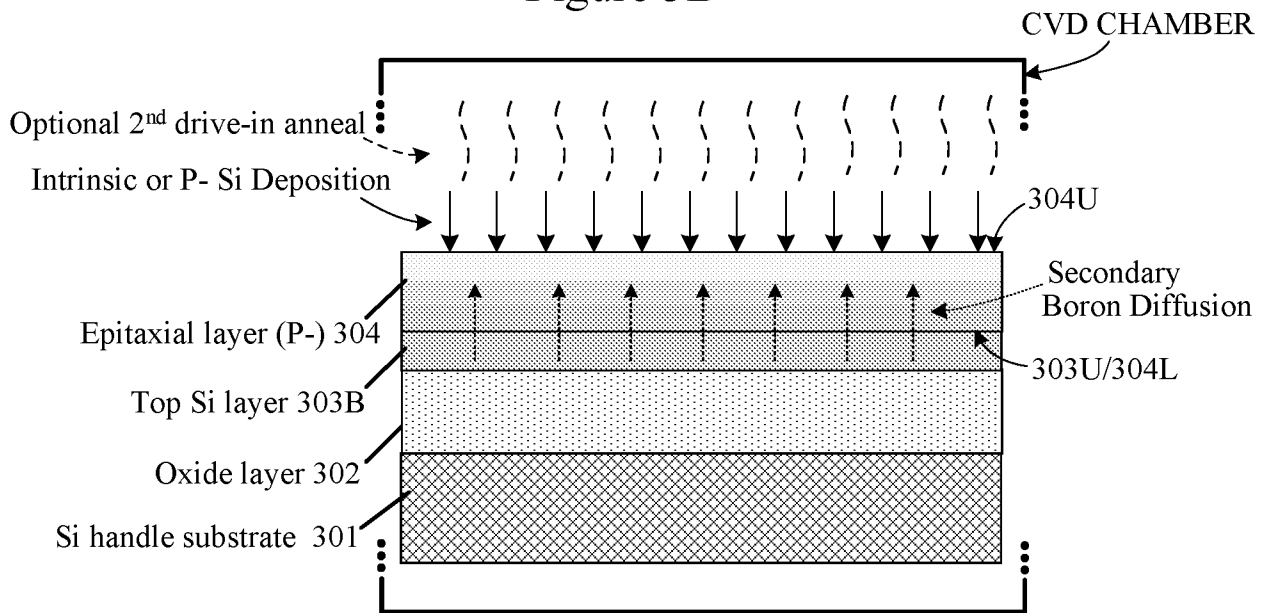


Figure 3C

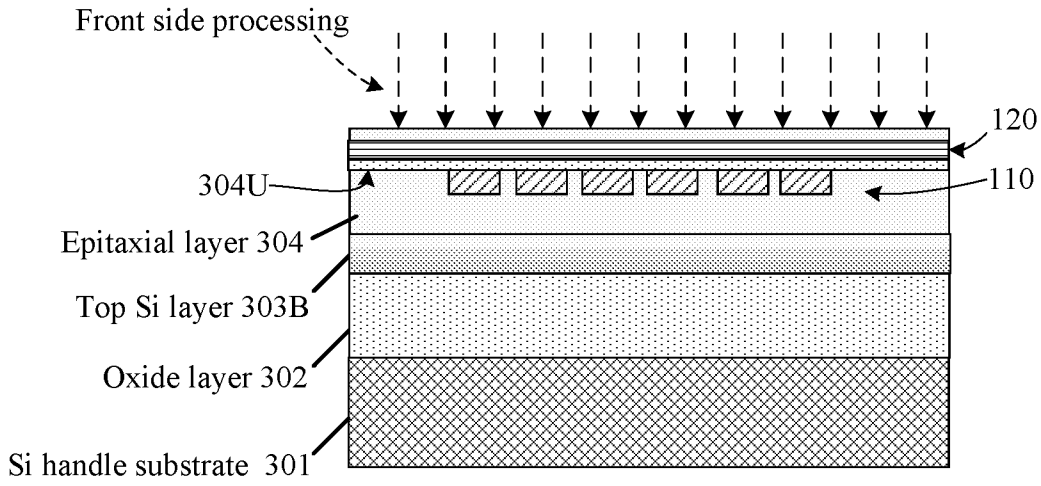


Figure 3D

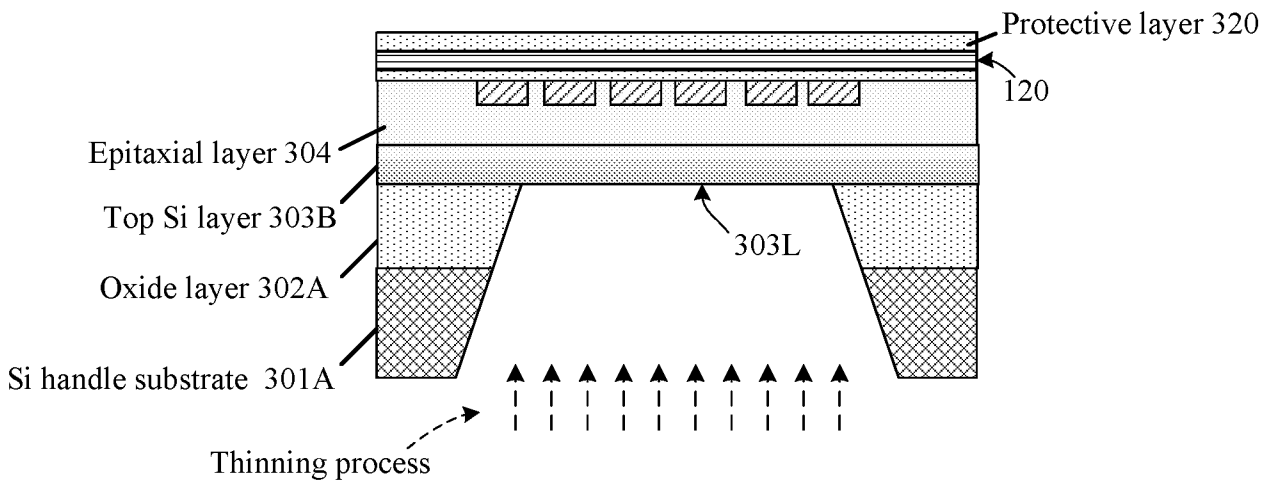


Figure 3E

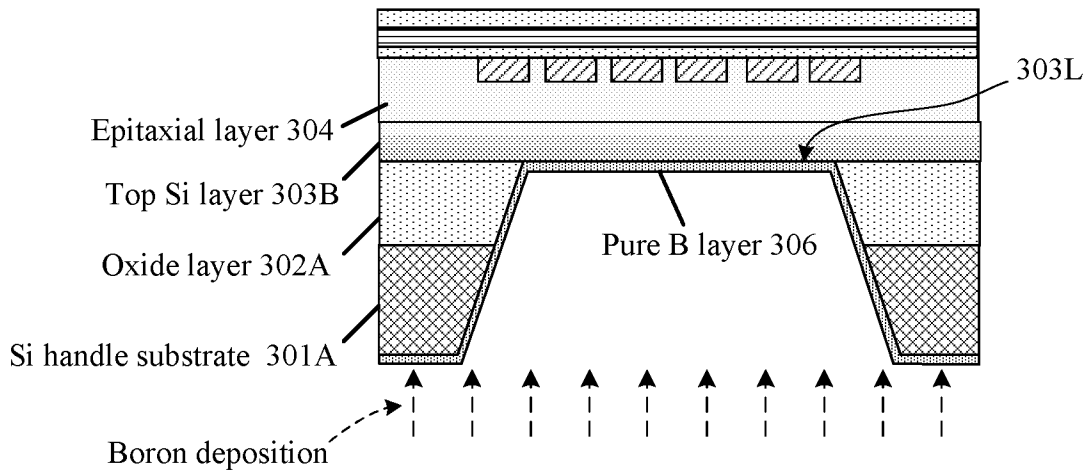


Figure 3F

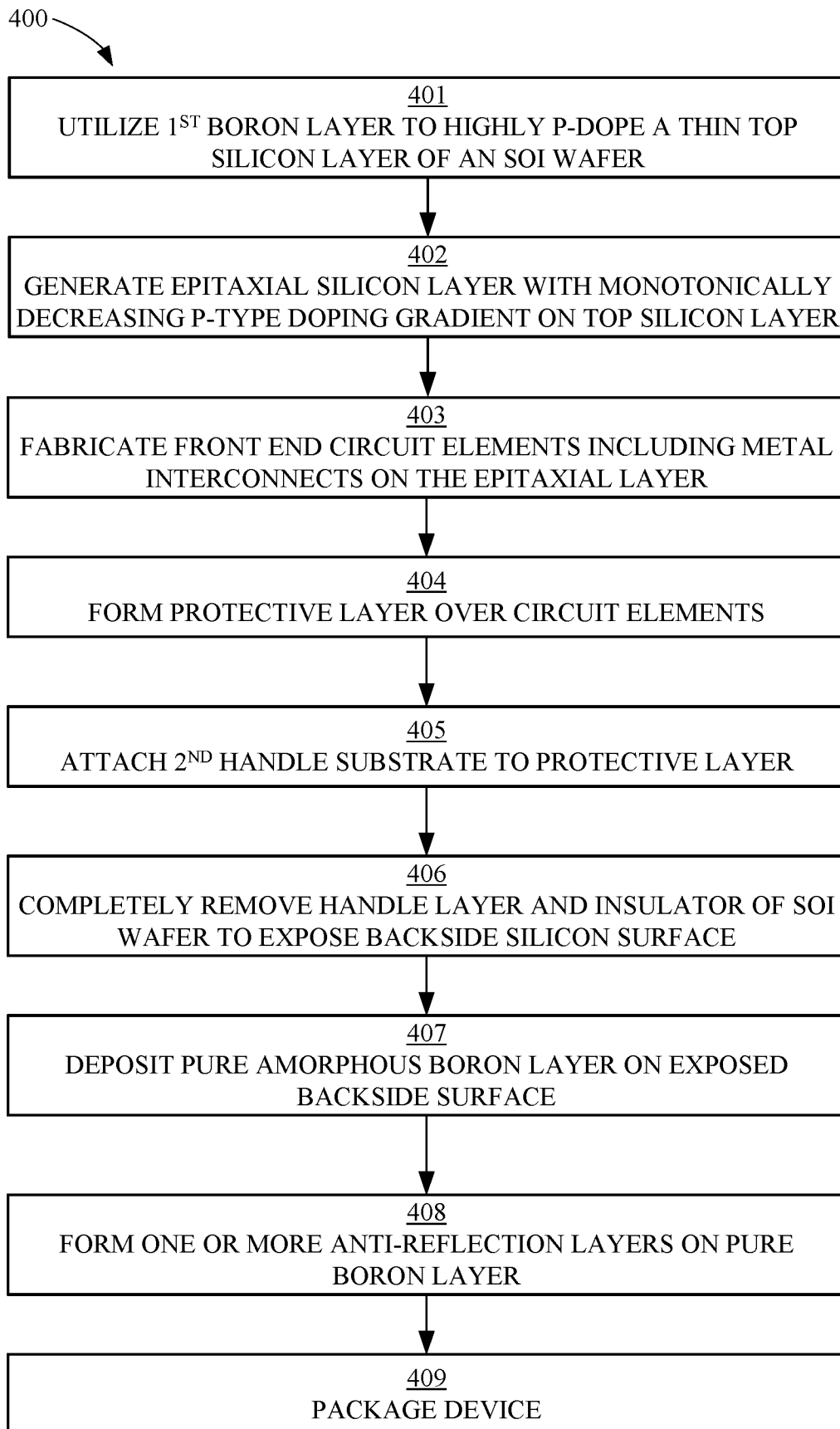


Figure 4

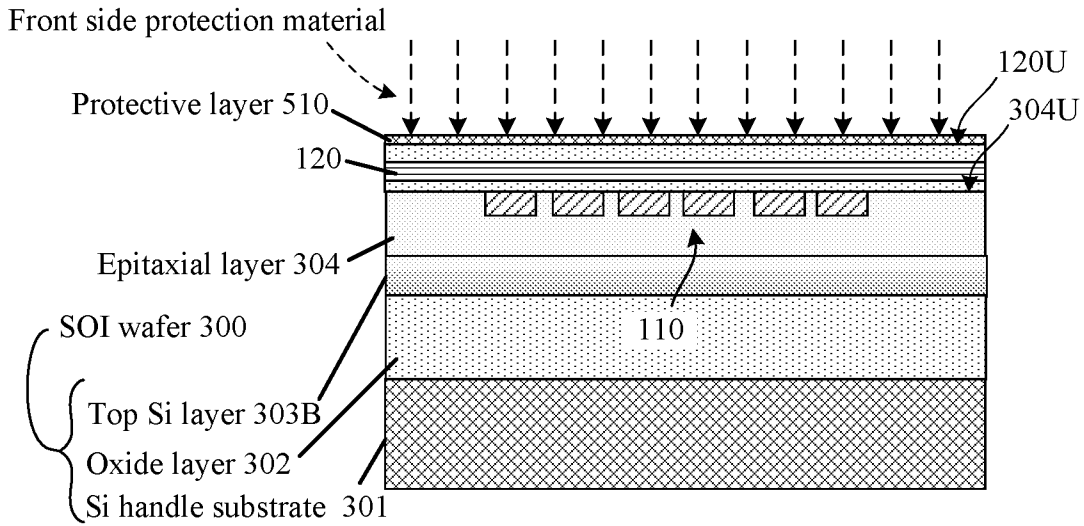


Figure 5A

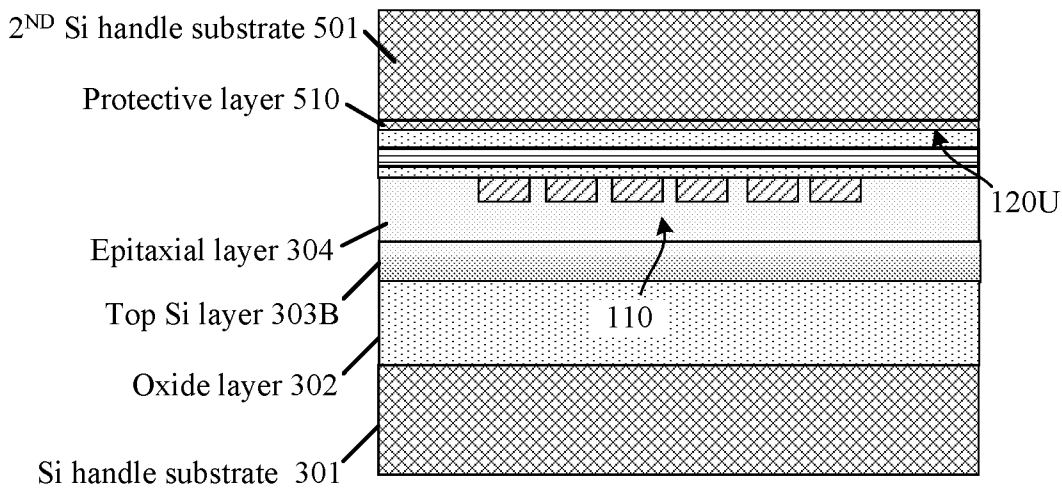


Figure 5B

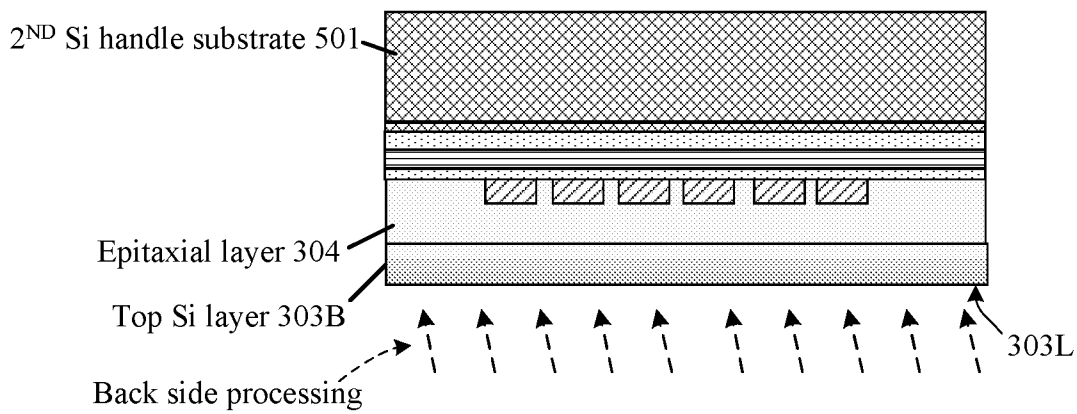


Figure 5C

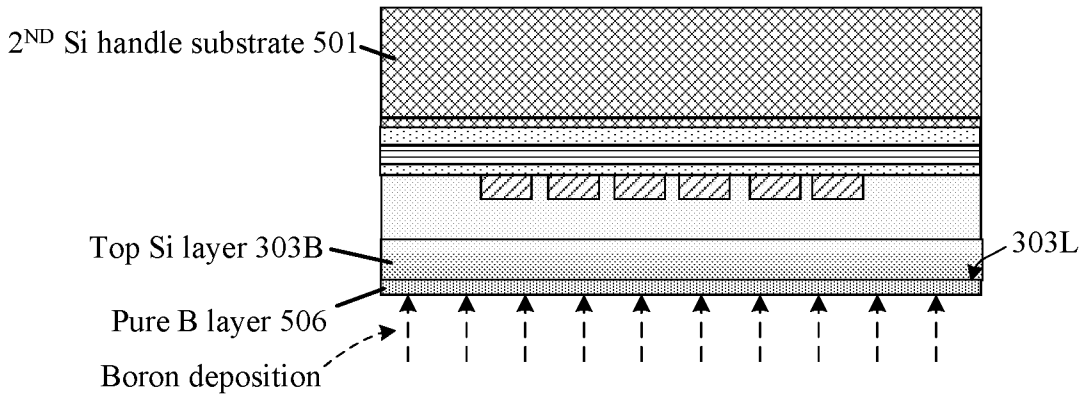


Figure 5D

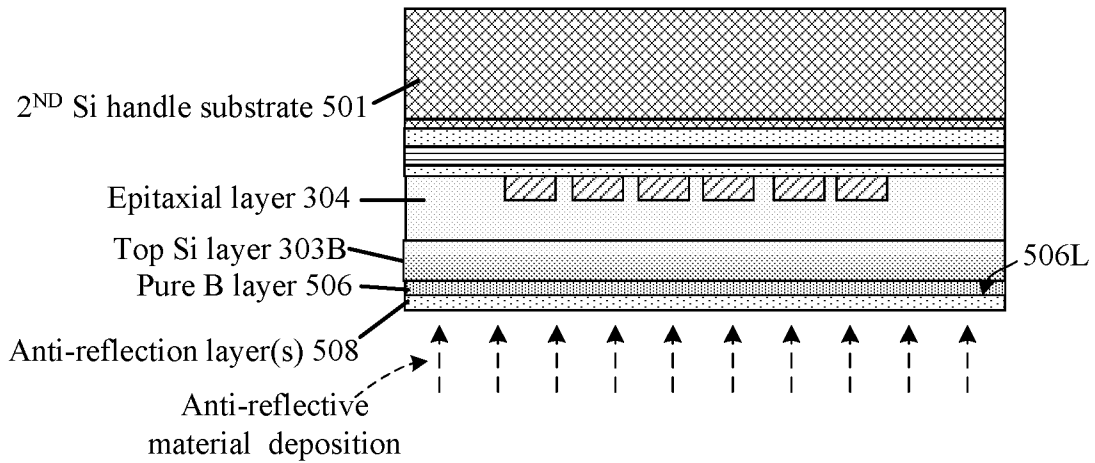


Figure 5E

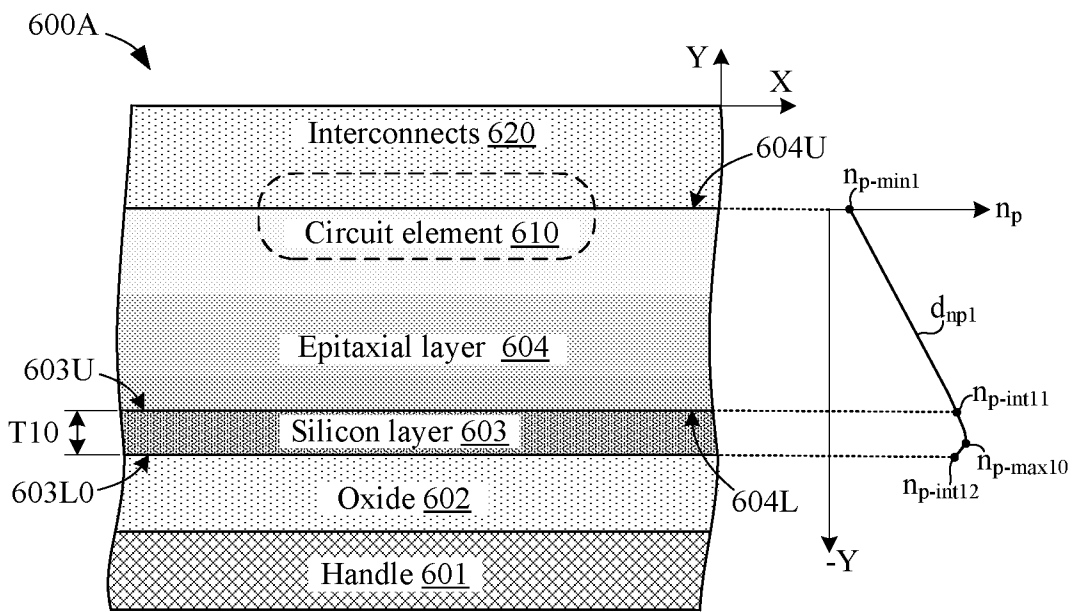


Figure 6A

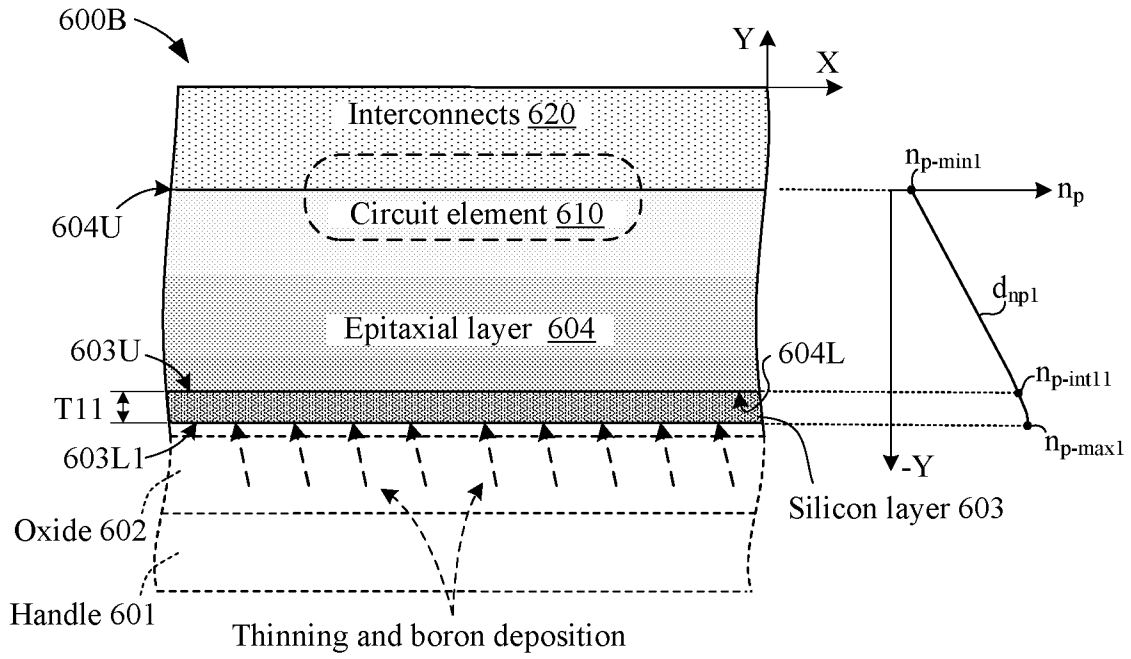


Figure 6B

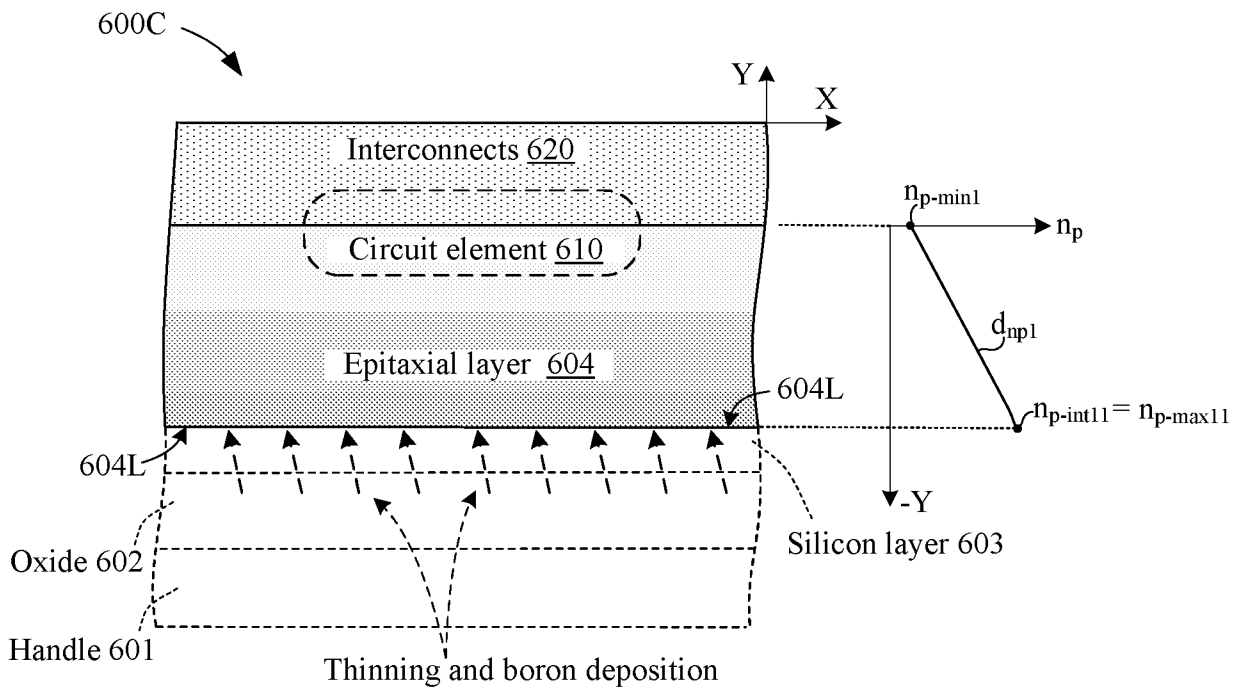


Figure 6C

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2021/026293

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 27/146(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) H01L 27/146(2006.01); G01N 21/88(2006.01); G02B 21/12(2006.01); H01J 31/50(2006.01); H01L 21/20(2006.01); H01L 21/30(2006.01); H01L 31/12(2006.01)		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: image sensor, epitaxial layer, pure boron layer, doping concentration, diffusion		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0020893 A1 (TETSUJI UENO et al.) 25 January 2007 (2007-01-25) paragraphs [0003], [0022], [0027], [0036]-[0037], [0047], [0049]-[0050]; and figures 1-2, 6-10.	1-22
Y	US 2016-0290932 A1 (KLA-TENCOR CORPORATION) 06 October 2016 (2016-10-06) paragraphs [0018], [0037]-[0039], [0053], [0057]-[0058]; and figures 3A-3F.	1-22
A	KR 10-2018-0000735 A (KLA-TENCOR CORPORATION) 03 January 2018 (2018-01-03) claim 1; and figure 1.	1-22
A	US 2010-0140675 A1 (HOWARD E. RHODES) 10 June 2010 (2010-06-10) paragraphs [0024]-[0025]; and figure 4.	1-22
A	JP 2007-013177 A (MAGNACHIP SEMICONDUCTOR LTD.) 18 January 2007 (2007-01-18) claims 1, 4-5; and figure 3F.	1-22
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 27 July 2021		Date of mailing of the international search report 27 July 2021
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer JANG, Gi Jeong Telephone No. +82-42-481-8364

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/US2021/026293

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