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(19)

(54) METHOD OF PHASE GATING CONTROL

(71) We, LICENTIA PATENT VERWALTUNGS G.m.b.H., of 1 Theodor-Stern-Kai, 6 Frankfurt/Main 70, Federal Republic of Germany, a German body corporate, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to a method of phase gating control.Such a control may be carried out by means of a monolithically integrated circuit in which the point in time when the firing pulse to be emitted by it takes place is determined by the fact that a ramp voltage which is mains synchronous and is produced by means of a capacitor charged by a constant current source achieves a threshold value which may be variable and predetermined in its level and which is adjacent a comparator.

Monolithically integrated phase gating control is known to be suitable particularly for controlling triacs and thyristors. (The journal "Elektronik" 1975, Volume 7, pp. 72 to 74). With the aid of phase gating control, the output capacity of a load on alternating mains current may be continuously changed by shifting the firing pulses between 0° and 180° phase angle for the load of prior-connected triacs or thyristors.

The firing pulses have until now been produced in monolithically integrated phase gating controls such that a saw-tooth generator at constant frequency (preferably from 100 Hz with a 50 Hz network) makes a voltage available which increases in linear manner in terms of time and the point in time of using the trigger signal may then be shifted along this ramp with a threshold value switch of variable response threshold. The threshold value switch activates an output stage which contains a pulse generator for producing the trigger pulse or the trigger pulse chain, if the voltage supplied by the saw-tooth generator exceeds the desired threshold of response. The known embodiment of phase gating control thus requires two timing elements i.e. one for the phase shifter for setting the firing time and one for producing the pulse in the output stage.

The invention seeks to provide an improved method of phase gating control.

According to the invention, there is provided a method of phase gating control comprising producing a mains synchronous ramp voltage by means of a capacitor charged by a constant current source, producing a firing pulse when the ramp voltage reaches a variably predetermined threshold value, further charging the capacitor until it reaches a further predetermined reference voltage and maintaining the firing pulse until this time. Preferably a monolithically integrated circuit issued and the reaching of the threshold value os determined by a computer.

An advantageous refinement of the method according to the invention provides for the capacitor to be discharged via the comparator when the threshold value is reached and at the same time for a storage trigger circuit supplying the ignition pulse to be set as a result of which a second constant current source is connected to the capacitor in addition and on the other hand the internally predetermined reference voltage is given to the comparator so that the capacitor is then charged by the two constant current sources and that when the reference voltage has been reached, the capacitor is discharged again via the comparator whereby the store trigger circuit is reset and the second constant current source is switched off while the reference voltage at the comparator remains until the zero axis crossing of the mains voltage and/or the mains current.

In further embodiment of the method, the circuit output, particularly the output amplifier of the monolithically integrated circuit is released only by setting of the storage trig-

ger circuit.

The stated method requires only one time defining capacitor for the ramp voltage and the firing pulse width. Moreover, the consumption of current is reduced quite substantially with regard to the known method. Thus in an advantageous manner both the total number of components and the loss of power is reduced to a minimum.

The invention will now be described in greater detail, by way of example, with reference to the drawings in which:-

Figure 1 shows a block circuit diagram of one embodiment of the invention

Figures 2*a* to *e* shows a function diagram for individual circuit elements.

A monolithically integrated circuit for a phase gating control is shown in the block circuit diagram of Figure 1 outlined in chain lines. At its output, to which the output amplifier A is connected, the circuit passes firing pulses to a triac TR through which a load Z is connected into a load circuit with the desired phase gating.

The supply of current to the integrated circuit takes place through the integrated element V, which also serves to rectify and limit the current supplied from an alternating voltage network. A normal smoothing capacitor C_G is assigned to the element V.

The circuit is connected up with a capacitor C. In contrast to conventional circuits,which required two separate RC elements for phase shifting of the firing pulse and its pulse width, here both functions are derived in an advantageous manner from only one capacitor.

Initially the phase state of the firing time is determined in the known way by comparison between a mains synchronous ramp voltage and a predetermined desired value. The capacitor C is discharged at the zero axis crossing of the mains voltage via a zero voltage detector U_O, a gate G2 and a switch S2. After expiry of the zero axis crossing pulse, the capacitor C is charged from a constant current source K1, the value of which may be set externally via a resistor R because of the unavoidable tolerance of the capacitor C. A control voltage U_{ST} of the difference between a desired voltage U_S and an actual value of the voltage U_I, which is passed into the circuit, determines the threshold value which must be achieved by the ramp voltage produced by charging the capacitor C, in order to fix the firing time. If the ramp voltage supplied by the capacitor C achieves the predetermined threshold value, then a thyrister T, taking over the function of the comparator, fires and sets a following storage trigger circuit F1 in turn. The Q output of the storage trigger circuit F1 releases the output amplifier A, switches a second constant current source K2 to the capacitor C in addition to the constant current source K1 and changes a switch S1 over to an internally predetermined reference voltage U_R via an RS trigger circuit F2 and an OR-gate G1.

The capacitor C is now charged by the constant current sources K1 and K2 until its voltage (U_C) reaches the reference voltage U_R. The duration of this charging corresponds to the pulse width (t_p) of the output pulse and thus of the firing pulse. If the capacitor voltage reaches the value U_R then the thyristor T again fires and sets the storage trigger circuit F1 back into its initial condition. The firing pulse is terminated thereby and the constant current source K2 is switched off. The RS trigger circuit F2 keeps the switch S1 however as before so that the internal reference voltage U_R remains at the thyristor T, The value of U_R is larger than the maximum control voltage U_{ST} so that it is possible to reliably prevent more than one firing pulse per half-period of the mains voltage from being emitted. This is particularly important because the energy content of the output pulse is greater than the natural requirement of the circuit per half-wave. In the succeeding zero axis crossing of the mains voltage, the zero axis crossing detector U_O resets the RS trigger circuit F2, discharges the capacitor C again via the gate G2 and the switch S2 and ensures the basic condition of the storage trigger circuit F1 in addition via the gate G3.

Furthermore, yet another current detector I_O is provided. When controlling inductive load Z, the load current of the mains voltage lags this means that, without taking the current into account, the circuit could deliver a firing pulse even during the time in which current is still flowing at a polarity which is opposite to the mains voltage. This in turn would lead to so-called "gaps" in the load current as the next firing pulse would only then be produced in the succeding half-wave. The statement as to whether the load current flows or not, is supplied by the triac itself. If the triac is fired then the voltage present at the electrode H2 moves to the value of the forward voltage of the triac from the instantaneous value of the mains voltage. If the load current falls below the retaining current of the triac towards the end of the half-wave then the voltage jumps back to the instantaneous value of the mains voltage which was present previously. The current detector interrogates this triac voltage by means of a resistor R_S and blocks off the pulse produced via gate G1 and switch S1 by raising the reference voltage as long as the triac is fired.

As in some circumstances the triac is quenched shortly before the zero axis crossing of the mains voltage when there is a resistant load Z- when the current drops below the retaining current - then the RS flip flop F2 must prevent a possible second firing pulse from being generated.

An integrated additional element is designated Ü and may intervene in the circuit via the gates G2 and G3, the operating voltage of the circuit via the gates G2 and G3, the operating voltage of the circuit being supervised thereby.

In Figure 2 the time curves of the voltages of individual circuit elements are shown in relation to the mains voltage U_N, in agreement with the method described above.

The path of the output voltage of the zero detector is designated U_O (Fig. 2b). This emits a pulse of the duration t_{pO} with each zero axis crossing of the mains voltage U_N (Fig. 2a). When this pulse is emitted, the capacitor C is discharged to a value U_{S2} and then is charged up by the constant current source K1 so that its voltage U_C rises as a ramp until it reaches the value of the control voltage U_{ST}(Fig. 2c). Discharge of the capacitor takes place via the thyristor T to a minimum value U_{MIN} of the ramp voltage and a renewed rapid charging (through the constant current sources K1 and K2) until the capacitor voltage U_C reaches the value U_R of the internally predetermined reference voltage and is again lowered to the value U_{MIN} by renewed firing of the thyristor T. The value of U_R is always selected such that it is greater than the maximum control voltage U_{ST} which may be input. Between the first and second discharge of the capacitor C described, the desired firing pulse is passed to the control electrode of the triac by the circuit as a voltage pulse U_A of the duration t_p (Fig 2d). In order to clarify the voltage curves the control voltage U_T of the thyristor T has been plotted over time t (Fig. 2e).

WHAT WE CLAIM IS:-

1. A method of phase gating control comprising producing a mains synchronous ramp voltage by means of a capacitor charged by a constant current source, producing a firing pulse when the ramp voltage reaches a variably predetermined threshold value, further charging the capacitor until it reaches a further predetermined reference voltage and maintaining the firing pulse until this time.

2. A method according to claim 1 wherein a monolithically integrated circuit is used.

3. A method according to claim 1 or 2, wherein the reading of the threshold value is determined by a comparator,

4. A method according to Claim 3, wherein when the threshold value is achieved, the capacitor is discharged by the comparator and at the same time a storage trigger circuit delivering the firing pulse is set by means of which a second constant current source is additionally switched to the capacitor and on the other hand the internally predetermined reference voltage is passed to the comparator; that the capacitor is then charged up by the two constant current sources; and that when the reference voltage is reached the capacitor is re-discharged via the comparator, by which the storage trigger circuit is reset and the second constant current source is switched off while the reference voltage at the comparator remains present until the zero axis crossing of the mains voltage and/or of the mains current.

5. A method according to Claim 4, wherein the circuit output is released only be setting of the storage trigger circuit.

6. A method of phase gating control substantially as described herein with reference to the drawings.

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2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

FIG. 1

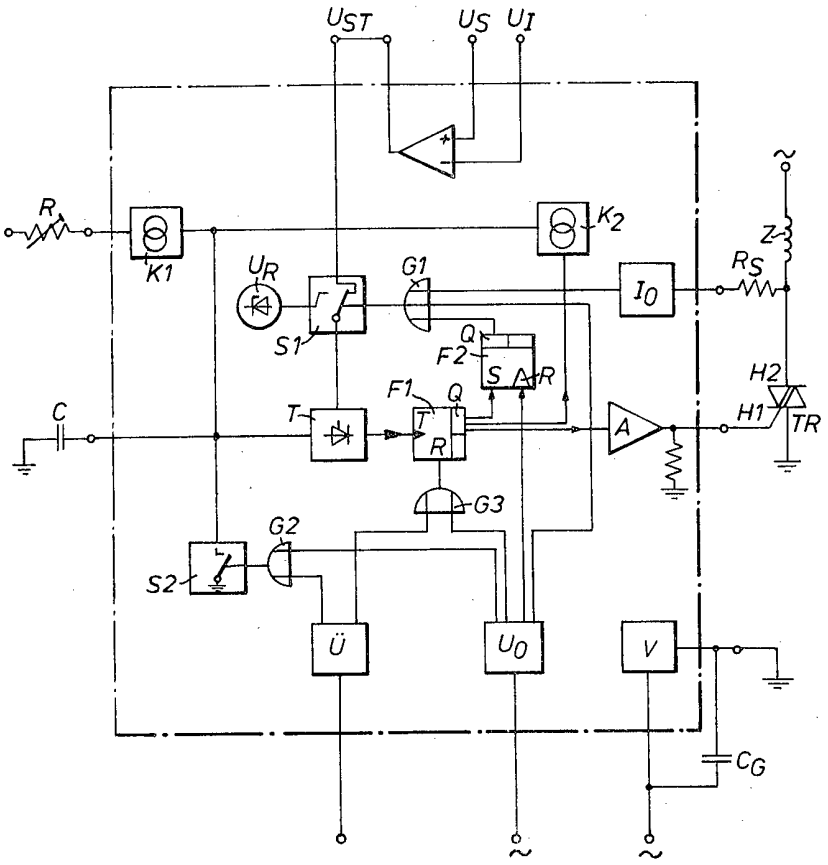

FIG.2a

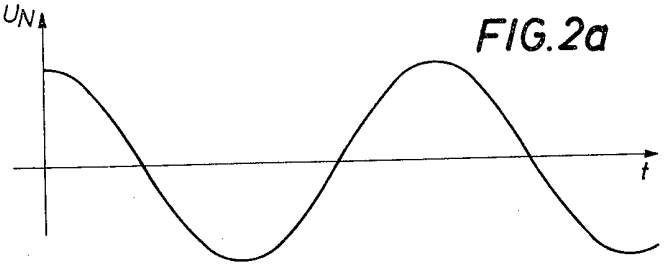

FIG.2b

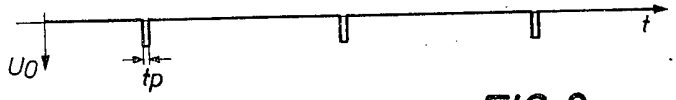

FIG.2c

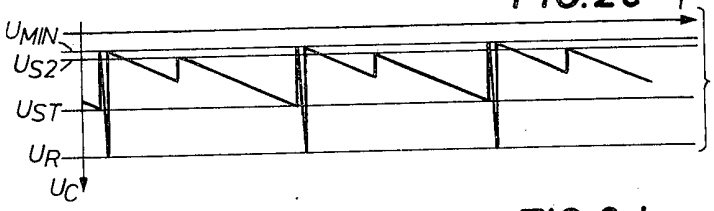

FIG.2d

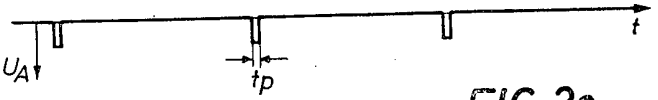

FIG.2e