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(54) IMPROVEMENTS IN OR RELATING TO DIGITAL REGENERATOR AMPLIFIER STAGES

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The invention relates to digital regenerator amplifier stages, and is a modification of or improvement in an amplifier as claimed in our co-pending Kingdom Patent Application No. 37798/76 (Specification No. 1,565,665).

In CCD circuits it is necessary to regenerate the information after a specific number of transmissions in order to retain the original information. In this respect the regenerator stages are subject to a plurlaity of requirements. They need to be substantially independent of variations of threshold voltage and supply voltage. On the other hand a reference voltage which is required for the analysis of the input signal needs to be produced within the circuits themselves, if possible. the output amplitude of the regenerator stages should be as high as possible. Furthermore, these regenerator stages are required to facilitate the production of a determinate basic charge in the CCD arrangement to give reliable processing of digital information. Finally they need to fit in with the configurations utilised for the construction of CCD-arrangements.

Our United Kingdom Patent Application No. 37798/76 (Specification No. 1,565,665) describes and claims a digital regenerator amplifier stage in which a first field effect transistor (11) has one channel terminal connected to an input point (152) and its gate terminal (112) connected to a terminal to which is applied, when operating, a first control potential (V_{P11}), an input shunt capacitance (16) is provided between said input point (152) and a first supply voltage terminal, the gate terminal (131) of a second field effect transistor (13) is connected to said input point (152), the channel of said second transistor (13) is connected between an output terminal (132) of said amplifier stage and a junction point (122), the channel of a third field effect transistor (12) is connected between said junction point (122) and a second supply voltage terminal (111), said third transistor having its gate terminal connected to a terminal to which is applied, when operating, a second control potential (V_{P12}), a second shunt capacitance (17) is provided between the junction point (122) and said first supply voltage terminal, the gate terminal (141) of a fourth field effect transistor (14) is connected to the junction point (122), the channel of said fourth transistor (14) is connected between the second supply voltage terminal (111) and said output terminal (132), an output shunt capacitance (19) is provided between said output terminal (132) and said first supply voltage terminal, and a current sink (180) is arranged between said output terminal (132) and a further terminal (181), such that the output potential is determined with respect to the ratio of the potentials across said input capacitance and said second capacitance, without reference to any fluctuations of the supply voltage or of any threshold voltage.

That proposed constructions substantially satisfies the above described requirements. One object of the present invention consists in providing a further improved construction which makes possible a substantial reduction in switching times is achieved.

The invention consists in a digital regenerator amplifier stage as claimed in Claim 1 of our United Kingdom Patent Application No. 37798/76 (Specification No. 1,565,665), in which a fifth field effect transistor (21) is connected between the point (24) and the first supply voltag terminal, the gate (211) of the fifth transistor is connected to a further point (25), a

sixth field effect transistor (20) is connected between the further point (25) and the second supply voltage terminal (111), a seventh field effect transistor (22) is connected between the further point (25) and the first supply voltage terminal, the gate (221) of the seventh transistor (22) is connected to the point (24), whereby the fifth transistor (21) and the seventh transistor (22) form a flip-flop stage, and an eighth field effect transistor (23) which can be separately controlled via its gate terminal (231), is connected between the further point (25) and the first supply voltage terminal.

The invention will now be described with reference to the drawings, in which:-

Figure 1 is a schematic circuit diagram of one exemplary digital regenerator amplifier stage constructed in accordance with the invention;

Figure 2 illustrates one alternative embodiment of the circuit;

Figure 3 is a set of explanatory waveform diagrams; and

Figure 4 is a graph illustrating the characteristic curve of a flip-flop stage.

The digital regenerator amplifier stage 1 illustrated in Figure 1 closely resembles that described in the parent Patent Application, and fundamentally consists of transistors 11 to 15. The transistor 15 is connected between an input terminal 151 and to an input point 152. The transistor 15 can be controlled by a pulse train $\emptyset$ applied to its gate terminal 153. The so-called first transistor 11 is connected between the input point 152 and a line 111 to which a supply voltage V_{CC} is connected. The transistor 11 can be controlled via its gate terminal 112 by a potential V_{P11}. The input point 152 is also connected to the gate terminal 131 of the so-called second transistor 13. The channel of the transistor 13 is connected between an output terminal 132, and, via the channel of the so-called third transistor 12 to the line 111. The transistor 12 can be controlled, via its gate terminal 121, by the potential V_{P12}. The gate terminal 141 of the fourth transistor 14 is connected to a junction point 122 at which the transistors 12 and 13 are connected in series. The transistor 14 is connected between the output 132 and the line 111. The transistors 11 and 12 serve to bias the parasitic shunt capacitances 16 and 17, whereas the trasistors 13 and 14, together with a current sink 18 produce a reference voltage and effect the amplification of the input signal. The current sink 18 is connected between the output terminal 132 and a terminal 181 to which a voltage V_B may be applied. The transistor 15 connects the input 151 to the nodal input point 152. In the following the mode of functioning of the circuit illustrated in Figure 1 will be described in association with Figure 3. At the time t_0 the transistors 11 and 12 are switched conductive so that the parasitic shunt capacitances 16 and 17 are charged to the voltage V_{CC}. If the trasistors 13 and 14 possess the same geometric dimensions, the current which flows through them is $i_{13} = i_{14} = i_g/2$, where i_g is the current flowing through the current sink 18. Then a voltage of $U_A = V_{CC} - U_T$ is connected to the output 132 of the differential amplifier 1, where U_T is the threshold voltage of the transistors 11 to 15. At the time t_1 the transistor 11 is switched off. This is achieved by disconnecting the potential V_{P11} at the gate terminal 112. This results in no change in the voltage across the shunt capacitance 16 and the current ratio $i_{13} = i_{14}$ is maintained. As illustrated in Figure 1, the input terminal 151 is connected to a current sink 190, at which the presence of a current i_S corresponds to a binary "1" and the absence of the current i_S corresponds to a binary "0". When the transistor 15 is conductive, the shunt capacitance 16 is thereby either discharged to the voltage $U_E = 0$ or remains biased at the voltage $U_E = V_{CC}$. In this way the output 132 can assume two different states at the time t_3.

(a) If $U_E < V_{CC}$, the transistor 13 is non-conductive as the voltage between its gate terminal and its source terminal is $U_E - U_A < U_T$. The voltage U_N across the shunt capacitance 17 remains at $U_N = V_{CC}$, and therefore the output voltage $U_A = V_{CC} - U_T$ is retained at the output 132 of the amplifier.

(b) If $U_E = V_{CC}$, the transistor 13 remains conductive as a result of which the gate and the source terminal of the transistor 14 are connected to one another.

This results in the transistor 14 being switched non-conductive and the current sink 180 discharging the output 132 in the direction of the potential V_B.

The two states (a) and (b) are subject to the condition that the transistor 12 should be blocked.

As the output voltage U_A is dependent only upon the ratio of the voltage U_N to U_E across the shunt capacitances 16 and 17, where $U_A = V_{CC} - U_T$, when $U_E < U_N$ and $U_A = V_B$, when $U_E = U_N$, fluctuations in supply voltage and threshold voltage have no influence upon the amplification process.

Figure 2 illustrates a circuit variant 10 of the digital regenerator amplifier stage 1 shown in Figure 1. Those details already described with reference to Figure 1 bear corresponding references. The transistor 110 which corresponds to the transistor 11 in Figure 1, is not, as in Figure 1, connected between the input point 152 and the line 111, but between the input point 152 and the nodal junction point 122. This has the advantage that the voltage drop which occurs across the transistor 12 when the shunt capacitance 17 is biased, affects the

shunt capacitance 16 to the same extent. In this way voltage differences across the two shunt capacitances 16 and 17 are advantageously avoided.

As can be seen from Figure 1 and 2, the digital regenerator amplifier stages corresponding to the invention possess further transistors 20 to 23, which are not present in Figures 1 and 2 of the parent Patent Application. The sixth transistor 20, which can be controlled by a potential V_{P20} at its gate 201, is connected between the supply voltage line 111 and a seventh transistor 22. The transistor 22 is connected between the transistor 20 and a terminal 222 which preferably carries a reference potential such as earth. The gate 221 of the transistor 22 is connected to a point 24 of the differential amplifier, which point 24 carries the potential U_A. The fifth transistor 21 is connected between the point 24 and a terminal 212 which preferably likewise carries a reference potential such as earth. The gate 211 of the transistor 21 is connected to a point 25, at which the transistors 20 and 22 are connected in series. The transistors 21 and 22 form a flip-flop stage. The transistor 23 is connected in parallel with the transistor 22, and can be controlled at its gate 231 by a potential V_{P23}. The transistor 23 is connected between the point 25 and a terminal 232, which preferably again carries a reference potential, such as earth.

Figure 4 illustrates the behaviour of the flip-flop stage in dependence upon the voltages U_{21} and U_{22} connected to the points 24 and 25. Straight line 26 separates the two stable states 28 and 29 from one another.

In the following, the function of the flip-flop is to be described in association with the transistors 23 and 20 serving to reduce the switching time of the digital regenerator amplifier stage. Until a time t_3, the terminal 201 of the transistor 20 is connected to a potential of 0 V and the terminal 231 of the transistor 23 is connected to the potential V_{P23}. This causes the transistor 20 to block, the transistor 23 to become conductive, and a potential of 0 V to be connected to the point 25. Thus a determinate starting state exists. At the time t_3 the flip-flop stage is activated. The terminal 201 of the transistor 20 is then connected to the potential V_{P20}, and the terminal 231 of the transistor 23 is connected to the potential 0 V. This causes the transistor 20 to become conductive and the transistor 23 to block.

In the one situation, in which the voltage $U_A = V_{CC} - U_T$, the transistor 22 remains conductive even when the transistor 23 blocks. On activation the flip-flop is set to the stable point 29 (Figure 4).

In the other situation, in which the voltage U_A is discharged by the current source, the flip-flop firstly triggers back to the point 29 at the time t_3, as U_A has initially only slightly discharged. The discharge of the output node 24 is firstly determined only by the current source 180 and $U_{21} = U_A$ reduces. The voltages U_{21} and U_{22} change along a potential state trajectory indicated by arrows in Figure 4. If the state trajectory exceeds the separatrix 26, the flip-flop stage can no longer trigger into the stage 29 and from now onwards the switching time is fundamentally determined by the switching time of the flip-flop stage.

A symmetrical flip-flop stage is obtained if the switching transistors 21 and 22 are identical and the load transistors 14 and 20 are identical. Fluctuations in the threshold voltages of these transistors give rise to asymmetry and a shifting of the separatrix. A displacement of the labile point 27 indicates that the time triggering is varying. The separatrix is overshot at an earlier or later point than the symmetrical flip-flop so that the reduction in switching time is increased or reduced.

In Figure 3, the arrow 3 indicates the switching time of the regenerator circuit without the flip-flop stage and the arrow 4 indicates the switching time of the regenerator circuit with the flip-flop stage. As can readily be seen, the flip-flop stage produces a considerable reduction in switching time.

As described in the parent Patent Application the circuits corresponding to the invention illustrated in Figure 1 and 2 can be employed in association with output stages and input stages of CCD-arrangements. The parent Patent Application also illustrates current sinks such as are employed in association with the digital regenerator amplifier stage corresponding to the present invention. The circuits shown in Figures 1 and 2 can be constructed in accordance with the technology described in detail in the parent Patent Application.

In the following claims there are included circuit, element and potential reference letters or numerals to assist the reader in identifying relevant components or circuit points in the specific description, but these are not intended to introduce specific limitations in the individual claims.

WHAT WE CLAIM IS:-

1. A digital regenerator amplifier stage as claimed in Claim 1 of our United Kingdom Patent Application No. 37798/76 (Specification No. 1,565,665), in which a fifth field effect transistor (21) is connected between the point (24) and the first supply voltage terminal, the gate (211) of the fifth transistor is connected to a further point (25), a sixth field effect

transistor (20) is connected between the further point (25) and the second supply voltage terminal (111), a seventh field effect transistor (22) is connected between the further point (25) and the first supply voltage terminal, the gate (221) of the seventh transistor (22) is connected to the point (24), whereby the fifth transistor (21) and the seventh transistor (22) form a flip-flop stage, and an eighth field effect transistor (23), which can be separately controlled via its gate terminal (231) is connected between the further point (25) and the first supply voltage terminal.

2. An amplifier stage as claimed in Claim 1, in which the first transistor (11) is connected to the junction point (122).

3. An amplifier stage as claimed in Claim 1, in which the first transistor (11) is connected to the second supply voltage terminal (111).

4. An amplifier stage as claimed in any preceding claim, in which between the input point (152) and the input terminal (151) of the amplifier stage (1, 10) there is arranged a fifth transistor (15) which can be controlled, via its gate terminal (153), by a pulse train $\emptyset$.

5. An amplifier stage as claimed in any preceding claim, in which the amplifier stage (1, 10) is constructed in an aluminium-silicon-technique.

6. An amplifier stage as claimed in any preceding claim, in which means are provided to cause the shunt capacitance 16 to either be discharged to voltage ($U_E < V_{CC}$) , or retain a voltage (V_{CC}) across the capacitance, that in dependence upon the information present at the input point (152) further means acting to block the second transistor (13) in the event of a binary "1" for ($U_E < V_{CC}$) being present, for which reason, the blocked third transistor (12) causes the voltage (U_N) to be retained across the second shunt capacitance (17) as ($U_N = V_{CC}$), and for which reason the output voltage (U_A) is likewise retained at the output (132), whilst said means act in the event of a binary "0" for ($U_E = V_{CC}$) to maintain the second transistor (13) conductive, as a result of which the fourth transistor (14) is blocked, and as a result of which the current sink (180) discharges the output (132) in the direction of the potential (V_B), and in order to accelerate this discharge process means are provided by which the sixth transistor (20) is switched conductive and the eighth transistor (23) is brought into the conductive state, as a result of which the flip-flop stage (21, 22, 11, 20) is activated.

7. A digital regenerator amplifier stage substantally as described with reference to Figure 1 or Figure 2.

For the Applicants,
G. F. REDFERN & CO.,
Marlborough Lodge,
14 Farncombe Road,
Worthing,
BN11 2BT.

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2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

Fig.1

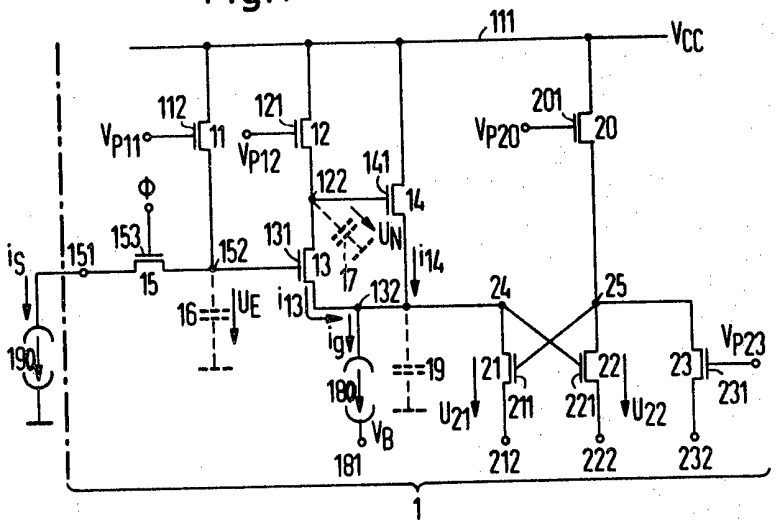


Fig. 2

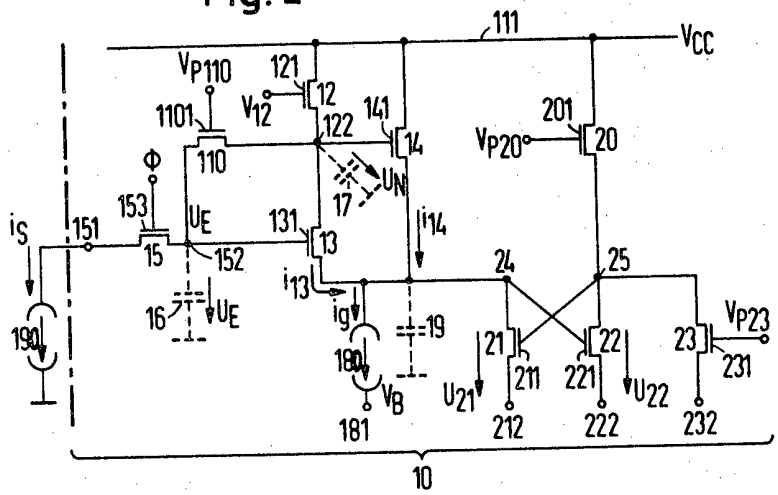
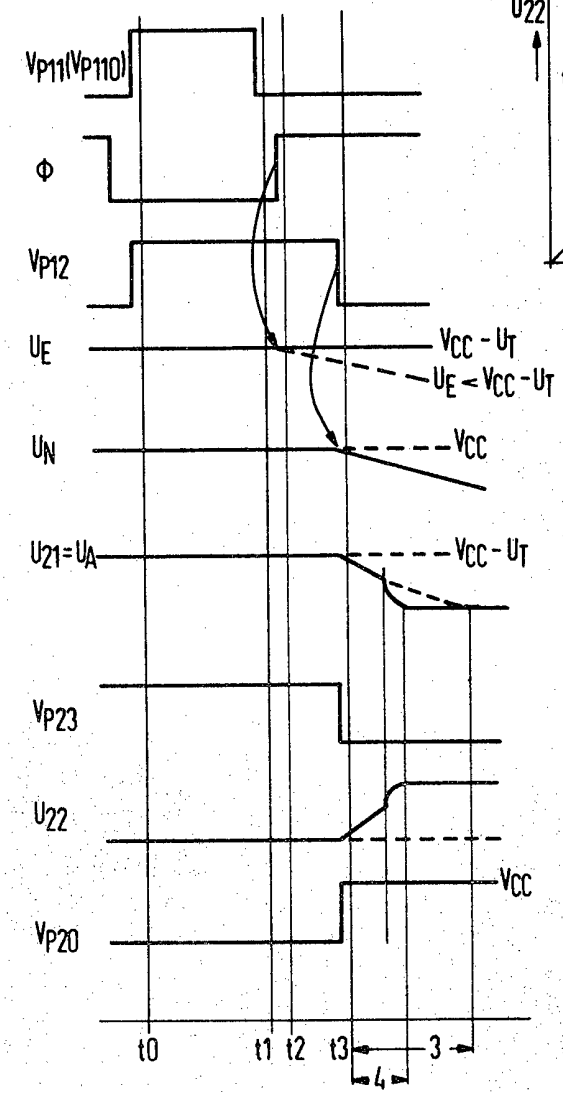


Fig. 3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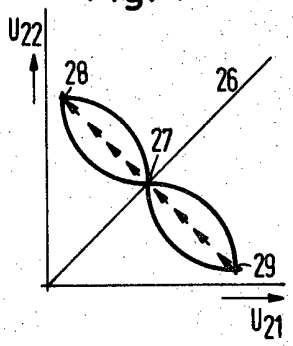
Φ
VP12
UE
VCC - UT
UE < VCC - UT
UN
VCC
U21=UA
VCC - UT
VP23
U22
VCC
VP20
t0
t1
t2
t3
3
4

Fig. 4


U22
28
26
27
29
U21