ABSTRACT

A new and improved method and apparatus for reliably and accurately controlling one or more operations of subsurface well drilling and well control equipment, and for reducing the likelihood of inadvertent actuation of such apparatus from stray or other undesired or spurious signals, is disclosed.

11 Claims, 7 Drawing Figures
Harold W. Moroney
Lester R. Hathcote
Thomas W. Sparkman
INVENTORS

BY
Pharel Wilson & Matthews
ATTORNEYS
BACKGROUND OF THE INVENTION

1. Field of the Invention
The present invention relates to methods and apparatus for controlling operations of subsurface well drilling and well control equipment.

2. Description of the Prior Art
In the prior art apparatus and methods for controlling down hole or subsurface well equipment, radiated electromagnetic energy was sent by a transmitter at the surface and sensed by the subsurface apparatus. The prior art apparatus often sensed stray or spurious undesired radio signals which would cause operation of the downhole equipment at a time when operation was not desired or wanted, damaging the well and equipment and causing needless expense and waste. Highly sensitive and accurate radio receiving circuitry to increase the selectivity and sensitivity of the downhole apparatus were affected by the temperatures of the earth adjacent the well and by the jostling and vibratory forces when such circuitry was being lowered into the well and were thus undesirable.

The use of magnetic structure, or acoustic signals or mechanical vibrations as signals to initiate downhole control did not overcome the problem since such signals had to be converted into electrical signals upon receipt by the downhole apparatus, limiting the sensitivity of the apparatus to that of the conversion equipment. Further, control of more than one downhole operation by other than electrical signals was difficult to achieve.

SUMMARY OF THE INVENTION

Briefly, the present invention provides a new and improved method and apparatus for controlling the operation of subsurface well drilling and well control equipment wherein predetermined numbers of pulses of electrical current at a preselected frequency are sent through the earth in the vicinity of the subsurface well equipment and are sensed by an inductive coil. Pulses or signals of other than the preselected frequency are excluded by a selective filter and the pulses of the preselected frequency are counted. A control signal, controlling operation of the subsurface well equipment, is formed in response to the presence of a predetermined count. Plural subsurface well tools and equipment as well as plural functions therein, each assigned a predetermined operating code number of pulses, may be selectively controlled in response to transmission and receipt of the predetermined code number in the method and apparatus of the present invention.

It is an object of the present invention to provide a new and improved subsurface well control apparatus and method.

It is an object of the present invention to provide a new and improved method and apparatus for subsurface well control which is not operated by stray or spurious signals.

It is an object of the present invention to provide a new and improved method and apparatus which selectively controls plural subsurface well tools and equipment.
electrical current to be transmitted through the earth between the casing 12 and the ground 14 adjacent the well with which the apparatus A is being used.

The subsurface equipment control portion S includes a sensing coil 21 (FIG. 2), a receiver/buffer 40 (FIG. 3), a frequency selective digital filter 60 (FIG. 3), a digital filter oscillator 61, a coded station control circuit 70 and a switch which operates in response to an output signal from the control circuit 70, as will be more evident hereinbelow. The buffer 40, the filter 60, the oscillator 61 and the control circuit 70 are mounted in a capsule or container 23 within the chamber 20a. The container 23 is mounted with the tubular member 20 by a suitable structure of the well known type.

The sensing coil 21 (FIG. 2) includes a spool shaped laminated magnetic core 21a which is mounted within the chamber 20a of the tubular member 21 by being snugly fit against the inner wall 20b of the tubular member 20 or by other suitable structure. A coil 21b formed by a plurality of turns of an electrically conductive wire is mounted about the center portion of the spool shaped core 21 and produces an electrical current in response to changes in the magnetic flux in the core 21a. A pair of electrical conductors 21c and 21d connect the coil 21b to the receiver/buffer 40 within the container 23. The core 21a senses the changes in magnetic flux in the earth formed by the passage of pulses of electrical current through the earth induced by the transmitter portion T of the apparatus A, and such changes in flux cause a current to flow in the coil 21b which is conducted to the receiver/buffer, as will be more evident hereinbelow.

A pair of output conductors 24a and 24b are electrically connected with the control circuit 70 within the container 23 and pass from the container 23 into the chamber 20a. The conductor 24a electrically connects the control circuit 70 to an electrically compatible switch in a subsurface tool or instrument E whose operation is to be controlled by the apparatus A of the present invention. If plural subsurface tools or instruments are to be controlled by the apparatus A of the present invention, as will be more evident hereinbelow, a plurality of output conductors connects each of such tools or instruments individually to a control output generator within the control circuit 70. The electrical conductor 24b connects the control circuit 70 to an electrical reference or common ground, for example the tubular member 20.

The switch in the tool or instrument E receiving the control signal over the conductor 24a may be a transistor, a relay, a silicon-controlled rectifier, or other suitable electrically operated switching device which responds to an input signal of electrical current and operates to permit the flow of electrical current from a self contained power source within the tool or instrument to operate such tool or instrument.

The tool or instrument E may be for example an explosive charge, a solenoid to operate a valve or other subsurface mechanical structure, or other subsurface well drilling and well control equipment, as has been previously set forth. An electrical conductor 24c connects the switch within the tool E to an electrical common or reference in order that the current from the control circuit 70 will pass through such switch to operate the tool E, as will be set forth hereinbelow.

The transmitter section T includes a transmitter circuit 50, a transmitter oscillator 51 and a drive/buffer 32 in addition to the structure previously set forth. The drive/buffer 32 is an impedance matching buffer of the well-known type which matches the output of the transmitter circuit 50 to the impedance of the relay or other control apparatus which operates the switch 16 in the transmitter T.

The transmitter circuit 50 receives a coded input signal in accordance with the equipment to be controlled, or the operation to be performed by such equipment, and forms such input signal into a train of pulses of a predetermined frequency which are converted in the impedance matching driver/buffer 32 to a proper level to cause the apparatus controlling switch 16 to close in response to each pulse. As has been set forth hereinabove, each closure of the switch 16 sends a pulse of electrical current through the earth adjacent the well. Thus, the transmitter circuit 50 controls the transmitter section T to send a preselected coded number of pulses at a predetermined frequency through the earth adjacent the well to control the operation of subsurface well drilling or well control equipment E through the subsurface equipment control portion S.

The transmitter 50 (FIG. 5) includes the transmitter oscillator 51, a transmitter binary counter 52, a transmit control switch 53, a control NAND gate 54, a control NAND gate 55, a control flip-flop 56 and a blocking flip-flop 57. An input signal corresponding to the preselected number of pulses to be transmitted is loaded into the transmitter counter 52 under the control of the switch 53, the gates 54 and 55 and the flip flop 56, as will be more evident hereinbelow. Subsequently, the switch 53, the gate 54 and 55 and the flip-flop 56 control the flip-flop 57 to permit pulses equal in number to the input count stored in the counter 52 to pass from the oscillator 51 through the flip-flop 57 to the drive/buffer 32 to open and close the switch 16 once for each of the pulses.

The switch 53 is a single pole, double throw switch having an arm 53a which connects a contact 53b to an electrical ground when the switch 53 is in a load position to cause the input count to be loaded into the transmitter counter 52. The arm 53a connects a contact 53c of the switch 53 to ground when the switch 53 is in a transmit position, controlling the gates 54 and 55 and the flip-flop 56 to allow the blocking flip-flop 57 to pass pulses from the oscillator 51 to the driver/buffer 32. An input 55a of the gate 55 is connected to ground, or logical "O" when the switch 53 is in the load position. The input 55a receives a logical "Y" through a current limiting resistor 53e from a positive power supply terminal 53b when the switch 53 is in the transmit position. An input 54a of the gate 54 receives a logical O when the switch 53 is in the transmit position, grounding such input through the contact 53c and the arm 53a. The input 54a receives a logical I from the positive power supply terminal 53d through a current limiting resistor 53f when the switch 53 is in the load position.

The second input 55b of the gate 55 is connected to an output terminal 54b of the gate 54 and receives the output of the gate 54 as one input. Similarly, an output.
55c of the gate 55 is connected to a second input 54c of the gate 54 to provide the output of the gate 55 as an input to the gate 54.

When the switch 53 is in the load position, as has been set forth hereinabove, the input 55a receives a logical 1 and the input 54a receives a logical 1. The logical 1 at the input 54a drives the output 54b of the gate 54 to a logical O, which is furnished to the input 55b of the gate 55. Presence of a logical O level at the inputs 55a and 55b causes the output 55c of the gate 55 to assume a logical "1" level. Thus, when the switch 53 is in the load position, the output terminal 55c of the gate 55 is a logical 1.

Presence of a logical 1 at the output 54b drives the output 55c of the gate 55 to a logical O. Thus, the output terminal 55c is a logical O when the switch 53 is in the transmit position.

An electrical conductor 56a connects the output 55c of the gate 55 to a J input 56b and a clock pulse 56c of the flip-flop 56. The flip-flop 56 is a master-slave flip-flop, reading in data into the J input 56b in response to a positive going clock signal, and transferring such signal to a Q output terminal 56e in response to a negative going clock signal. A K input 56d of the flip-flop 56 is grounded. The Q output terminal 56e of the flip-flop 56 is electrically connected by a conductor 56f to a load input 52b of the transmitter counter 52 and by an electrical conductor 56g to a clear input 57e of the flip-flop 57. A clear input 56h of the flip-flop 56 is electrically connected to a borrow output terminal 52e of the counter 52 by an electrical conductor 52f.

The transmitter counter 52 receives an input binary signal over a plurality of input terminals 52a corresponding to the binary count equaling the number of pulses to be sent by the transmitter T. A clear input 52d of the counter 52 is connected to ground to prevent inadvertent clearance of the loaded input binary number before the proper count is achieved. An up count input terminal 52g of the counter 52 is connected through a current limiting resistor 52h to a positive power supply terminal 52i in order to prevent the counter 52 from counting upward. A down count input terminal 52c of the counter 52 is electrically connected by a conductor 57f to a Q output terminal 57d of the blocking flip-flop 57. The transmitter counter 52 receives a binary input count corresponding to the number of pulses desired to be transmitted over the conductors 52a and counts downward from such binary count in response to pulses furnished to the down count input 52c by the flip-flop 57 over the conductor 57f. The counter 52 continues its count downward until a count of zero is reached at which time a logical O is provided to the clear input 56h of the flip-flop 56 over the conductor 52f.

The transmitter oscillator 51 is an oscillator of the well-known type and oscillates at a preselected frequency of twice the frequency of the signal output of the transmitter section T. An electrical conductor 51a connects the transmitter oscillator 51 to a J input 57a, a clock pulse input 57b, and a K input 57c of the flip-flop 57. The flip-flop 57 changes state at the Q output terminal 57d in response to each positive zero crossing in the output signal from the transmitter oscillator 51, dividing the output frequency of the oscillator 51 by two and providing an electrical signal of the preselected frequency to the driver/buffer 32 over an electrical conductor 57g and to the transmitter counter 52 over the electrical conductor 57f.

In the operation of the transmitter 50, a push-button switch or other suitable means is electrically connected to the input conductors 52a and used to provide electrical signals over such conductors corresponding to the number of pulses to be transmitted. As will be more evident below, upon completion of the previous transmission, the Q output 56e is a logical O, and such signal is presented to the load input 52b of the counter 52, allowing the input count to enter the counter 52.

If not already in the load position, the switch 53 is moved to the load position, providing a logical 1 at the output terminal 55c of the gate 55. The logical 1 is received at the inputs 56b and 56c of the flip-flop 56, and stored within the flip-flop 56. On receipt of a negative going pulse at the clock pulse input 56c, the logical 1 is transferred to the Q output 56e of the masterslave flip-flop 56. The logical O at the flip-flop 56 remains until the negative going clock signal is conducted to the blocking flip-flop 57, preventing such flip-flop from operating by maintaining the Q output terminal 57d at a logical O.

When it is desired to transmit, the switch 53 is moved from the load position to the transmit position, allowing current to flow from terminal 53d into the input 55a, driving the output terminal 55c from a logical 1 to a logical O, a negative-going transition which is conveyed by conductor 56a to the clock pulse input 56c of the flip-flop 56. The negative going clock pulse transfers the logical 1 previously stored within the masterslave flip-flop 56 to the Q output terminal 56e.

Presence of a logical 1 at the terminal 56e permits the flip-flop 56 to open, and allows the clock pulses from the oscillator 51 to appear at the terminal 57d as output pulses. The output pulses are furnished to the driver/buffer 32 over the conductor 57g and pass from the driver/buffer 32 to the switch 16 to cause pulses of electrical current to be sent through the earth in the vicinity of the well, as has been previously set forth. Each of the output pulses from the terminal 57d are supplied to the counter 52 by the conductor 57f and cause a downward binary count of 1 in response to each pulse. Counter 52 counts downwardly until the input count has been depleted, and at this time presents a borrow signal, or logical O to the clear input 56h of the flip-flop 56 over the conductor 52f. Presence of a logical O at the clear input terminal 56h drives the Q output terminal 56e of the flip-flop 56 to a logical O regardless of the inputs present at the input terminals 56b, 56c and 56d. The logical O at the output terminal 56e is presented to the clear input terminal 57e of the blocking flip-flop 57 by the conductor 56g, and drives the Q output terminal 57d to a logical O regardless of the presence of the output of oscillator 51 at the input terminals 57a, 57b and 57c thereby blocking any further pulses from the oscillator 51 from reaching the driver/buffer 32 in response to the counter 52 having counted the predetermined number of output pulses.

An input capacitor 41 (FIG. 4) of the receiver/buffer 40 is electrically connected in a parallel circuit with the magnetic coil 21a and the coil 21b of the sensing coil 21 between the conductors 21c and 21d. The impedance value of the input capacitor 41 is chosen in order to tune the sensing coil 21 to be sensitive to the preselected frequency of the transmitting section T. A pair of operational amplifiers 42 and 43 connected in a cas-
caded arrangement by a coupling capacitor 44 amplify the signals provided across the input capacitor 41 and furnish the amplified signals over an output conductor 45 to the frequency selective digital filter 60. A feedback resistor 42a is connected between an output terminal 42b and an input terminal 42c of the amplifier 42 to limit the gain of such amplifier. A variable feedback potentiometer 43a is connected between an output 43b and an input 43c of the amplifier 43 to control the gain. The resistance value of the potentiometer 43a is adjustable in order to selectively adjust the gain as may be desired. A potentiometer 46 is electrically connected between the output conductor 45 and ground at the output 43b of the amplifier 43. The potentiometer 46 is an impedance matching potentiometer to match the input impedance of the frequency selective digital filter 60. It should be noted that the receiver/buffer 40 amplifies the incoming signal and furnishes such incoming signal without modification of the duration or length of such signal to the frequency axis selective digital filter, since adjusting the duration of the incoming signal would cause the incoming signal to be rejected by the filter, as will be more evident hereinbelow.

The frequency selective digital filter 60 (FIG. 6) receives the signals from the receiver/buffer 40 and rejects and excludes signals of other than the preselected frequency being transmitted by the transmitter section T. The digital filter 60 includes the digital filter oscillator 61, a pair of D-type control flip-flops 62 and 63, an output D-type flip-flop 64, a pair of binary counters 65 and 66, a coding output circuit 67 and an output NAND gate 68. The control flip-flops 62 and 63 respond to positive axis crossings in the input signal on the conductor 45 and establish an interval during which the clock pulses from the oscillator 61 are counted by the binary counter 65 and 66. The frequency of the oscillator 61 is chosen to be a predetermined constant multiple of the preselected frequency being transmitted by the transmitter T so that a predetermined number of output pulses of such oscillator 61 will occur between positive zero crossings of the input signal. In the embodiment illustrated in the accompanying drawings, the filter oscillator 61 has an output frequency 200 times the preselected frequency sent from the transmitter T. The coding circuitry 67 and the output NAND gate 68 permit a control signal to pass to the output flip-flop 64 in response to a second positive zero crossing of the input signal at the end of one cycle of the input signal if the number of clock pulses from the oscillator 61 counted in the counters 65 and 66 is 198, 199 or 200. In this manner, only output signals of the preselected frequency are permitted to pass through the frequency selective digital filter 60, excluding and rejecting spurious signals and permitting accurate and reliable control of the subsonic well equipment E by the apparatus A.

The input conductor 45 provides the input signal to a clock pulse input 62a of the flip-flop 62. A D input 62b of the flip-flop 62 is connected to ground in order that the flip-flop 62 will provide a logical O at a Q output 62c in response to a positive axis crossing at the clock pulse input 62a and a logical 1 output at a Q output 62d. A clear input 62e is maintained at a logical 1 in input in response to a bias voltage furnished to the input 62e over a conductor 62f and a current limiting resistor 60a from a positive power supply 60b.

An electrical conductor 62g connects the output 62c of the flip-flop 62 to a D input 63a of the flip-flop 63. A clock input 63b of flip-flop 63 is electrically connected by a conductor 63c and an output conductor 61a to receive the clock pulses from the filter oscillator 61. A Q output 63d of the flip-flop 63 is connected by a conductor 63e to a preset input 62h of the flip-flop 62. Presence of a logical 0 at the preset input 62h of the flip-flop 62 sets the output 62c of the flip-flop 62 to a logical 1 level regardless of the presence of a clock-pulse at the input terminal 62a. A Q output 63f of the flip-flop 63 is connected by an electrical conductor 63g to a clear input 65a of the counter 65 and a clear input 66a of the counter 66. Presence of a logical 1 at the output terminal 63f of the flip-flop 63 clears the count from the counter 65 and 66. A clear input 63h of the flip-flop 63 is maintained at a logical 1 by the power supply terminal 60b through the current limiting resistor 60a to prevent the output 63f of the flip-flop 63 from being driven to a logical 1 at the improper times. A preset input 63i of the flip-flop 63 is connected by a conductor 63j to the output 62d of the flip-flop 62. Presence of a logical 0 at the output 62d when conducted to the input 63i of the flip-flop 63 sets the output 63d of the flip-flop 63 to a logical 1.

An electrical conductor 61b provides the clock pulses from the oscillator 61 to an up count input 65b of the binary counter 65 causing the binary counter 65 to count the pulses from the oscillator 61. A down count input 65c and a plurality of input terminals 65d of the counter 65 are maintained inactive by the presence of a logical 1 at such inputs from the positive power supply terminal 60b, the current limiting resistor 60a and an electrical conductor 60c. In a like manner, a down count input 66c and a plurality of input 66d of the counter 66 are maintained in an inactive state by the presence of a logical 1 on the conductor 60c.

The binary counter 65 counts the pulses from the oscillator 61 and provides a binary indication of such counter on a plurality of output terminals 65g. A carry output terminal 65f of the counter 65 provides a signal to an up count input 66b of the counter 66 when the counter 65 has counted to its capacity, and allows the counter 66 to begin counting in conjunction with the counter 65 in order to increase the counting capacity of the digital filter 60. A carry output 66f of the counter 66 is connected to a load input 65e and a load input 66e of the counter 65 and 66, respectively, to lock the counter 65 and 66 at the maximum counting capacity of such counters in the event that the maximum counting capacity of such counters is reached in order to prevent recycling and erroneous output counts from the counter 65 and 66.

The coding circuit 67 includes an inverter 67a connected to the "4" output of the counter 65, an inverter 67b connected to the "32" output of the counter 66, an inverter 67c connected to the "16" output of the counter 66 and a two input NAND gate 67d connected to the "2" and "1" outputs of the counter 65. The coding circuits 67 are selected to provide a predetermined input signal to the output NAND gate when the counters 65 and 66 have reached a predetermined count. In the embodiment illustrated in FIG. 6, the coding circuit 67 will furnish an electrical signal to the NAND gate 68 driving the output 68a of the NAND gate 68 to a logical O when the output count of the counter 65 and 66 is a decimal 200, 201 or 202. Other coding circuits may be used in accordance with the frequency of oscillator 61.
An electrical conductor 68b connects the output 62d of the flip-flop 62 to an input of the NAND gate 68. The output terminal 62d of the flip-flop 62 is a logical 1 for the first clock pulse cycle of the oscillator 61 after the positive going transition in the input signal on the conductor 45 is received at the clock input 68 of the flip-flop 62. Subsequent to such first clock cycle of the oscillator 61, the output 63d of the flip-flop 63 is driven to a logical O, which is furnished to the preset input 62h of the flip-flop 62 returning the output 62c of the flip-flop 62 to a logical 1 and the output 62b of the flip-flop 62 to a logical O.

The logical 1 during the one cycle of the oscillator 61 previously set forth serves as a strobe or scan signal for the NAND gate over the conductor 68b. During the presence of such logical 1 on the conductor 68b, the output count of the counter 65 and 66 as modified in the coding circuitry 67 will drive the output 68a of the gate 68 to a logical O only if the count of the counter 65 and 66 is 200, 201 or 202, as has been previously set forth.

At the end of the scan or strobe pulse on the conductor 68b, the oscillator 61 will energize a clock input 64a of the output flip-flop 64, transferring the signal present at the output 68a of the gate 68 to a D input 64b of the flip-flop 64 over an electrical conductor 68c. As has been set forth previously, the output 68b of the gate 68 is a logical O if the predetermined count corresponding to the duration of an input signal of the predetermined frequency has occurred between positive axis crossings of the input signal present on the conductor 45. The presence of a logical O on the input 64b of the flip-flop 64 causes a Q output 64c of the flip-flop 64 to assume a logical O in response thereto. If the count of the counter 65 and 66 as modified in the coding circuitry 67 is not the preselected number 200, 201 or 202, the output of the NAND gate 68 on the input 64b of the flip-flop 64 is a logical 1, and such logical 1 is transferred to the Q output 64c.

The Q output terminal 64c of the flip-flop 64 furnishes the output of the frequency selective digital filter 60 to the coded station control circuit 70 over an output conductor 69. The output signal of the digital filter 60 present on the conductor 69 is normally a logical 1 level, and is a logical O only if the duration of the input signal furnished to the digital filter 60 by the receiver/buffer 40 over the conductor 45 is of a duration corresponding to the period of the preselected frequency of the transmitter T. Accordingly, the digital filter 60 excludes and rejects unwanted and spurious signals and provides reliable and accurate control of the subsurface well equipment E.

The coded station control circuit 70 (FIG. 7) includes a timing control circuit 71, a binary counter 72, a coding gate circuit 73, a pair of control output generator flip-flops 74 and 75 and a power supply reset circuit 76. The control circuit 70 receives pulses over the conductor 69 from the filter 60, with the timing circuit 71 providing a timing control pulse in response to the first incoming pulse. The timing control pulse limits the time of receipt of pulses to a predetermined time interval in order that spurious and undesired signals are not counted or received. The binary counter 72 counts the number of the incoming pulses on the conductor 69 until cleared by the timing control circuit 71 at the end of the time interval transfers the output count of the counter 72 through the coding gates 73 to the control output generators 74 and 75. The generators 74 and 75 provide an output pulse over conductors 77 and 78, respectively in response to the presence of a predetermined code at their inputs, and furnish the signal over the conductors 77 and 78 to the switch mounted with the equipment E to be controlled by the apparatus of the present invention. The power supply reset circuit 76 resets the control output generator 74 and 75 and the timing circuit 71 when the subsurface equipment portion S of the apparatus A is initially energized at the surface of the earth before being lowered into the well to operate the equipment E, as will be more evident hereinbelow.

The timing circuit 71 is a retriggerable monostable multivibrator with clear integrated circuit, such as for example a Texas Instruments Part No. SN74122. The timing circuit 71 is connected to the conductor 69 at a pair of inputs 71a by a conductor 69a, A high to low transition on the conductor 79, formed in response to the presence of a pulse of the preselected frequency sensed by the digital filter 60 causes the timing circuit 71 to form a positive going pulse at such time as a Q output 71b thereof. A Q output 71c provides an output signal which is the inverted signal of the Q output 71b, and forms a negative going, logical O pulse at the same time that the output 71b forms the positive going pulse. The duration of the pulse formed in the timing circuit 71 is controlled by an external resistor 71d and an external capacitor 71e. The resistor 71d and capacitor 71e receive current from a power supply terminal 71f and permit the timing circuit 71 to provide an output pulse until the current from the power supply 71f through the resistor 71g discharges the capacitor 71e to a level to cause the control circuit 71 to terminate the positive output signal from the output terminal 71b and provide a positive output signal from the output terminal 71c.

An electrical conductor 69b connects an up count input 72a of the binary counter 72 and furnishes the pulses of the preselected frequency from the digital filter 60 to the binary counter 72. The binary counter 72 counts the number of such pulses furnished to the control circuit 70 by the filter 60 and provides a binary output count at a plurality of output terminals 72b to the coding circuit 73. A clear input terminal 72c of the counter 72 is connected to the output 71c of the timing circuit 71 by a conductor 71g and responds to the transition to a logical O of the output terminal 71c in response to the initial incoming pulse to clear the binary counter 72 and begin a new count in response to the incoming pulses.

A down count input 72d of the counter 72 and a plurality of input terminals 72e of the counter 72 are provided with a logical 1 from a positive power supply terminal 76a through a current limiting resistor 76b to prevent the counter 72 from downward counting and to load in the maximum output count of the binary count and prevent recycling of the counter should the maximum count be exceeded. A carry output 72f of the counter 72 is connected to a load input 72g of the counter 72 and provides an output signal in response to the counter 72 reaching its maximum count, which is furnished to the load input 72g. The input signal at the load input 72g causes the logical "l" present at the input terminal 72e of the counter 72 to be loaded into the counter, and prevents further counting by the counter 72 when the maximum count of such counter
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has been reached. The coding circuitry 73 receives the output from the output terminal 72b of the counter 72 and provides control signals to the control output generator 74 and 75 in response to the presence of a predetermined code output from the counter 72. The coding control circuit 73 includes a plurality of inverters 73g, 73h, 73i and 73j. The AND gates 73b, 73c, 73e and 73f are further electrically connected to the output 71b of the timing circuit 71 by an electrical conductor 71h. The conductor 71h provides the negative-going transition of the signal present at the output terminal 71b at the termination of the time interval determined by the resistors 71d and 71e of the timing circuit 71 to the above-reference AND gates and to a clock pulse input 74a and a clock pulse input 75a of the control output flip-flops 74 and 75, respectively. The negative-going transition serves as a strobe or read-in signal and causes the output of the output terminal 72b of the counter 72 to be transferred to the control output generator flip-flops 74 and 75 in response to a preselected coded number of pulses of the predetermined frequency being received by the filter 60 and transferred to the control circuit 70.

A J input terminal 74b of the flip-flop 74 receives a logical 1 input signal from the AND gates 73b, 73a and the inverters 73g and 73h when the output count of the counter 72 is a binary count corresponding to the decimal number 3 at the time of the strobe signal on the conductor 71h. An K input 74c of the flip-flop 74 receives a logical 1 from the AND gates 73a and 73c and the inverters 73g and 73j at the time of the strobe signal if the binary count and the counter 72 corresponds to a decimal 6. A J input 75b of the flip-flop 75 receives a logical 1 from the AND gates 73d and 73e and the inverters 73h and 73i at the time of the strobe signal on the conductor 71h if the binary count of the counter 72 corresponds to a decimal 9. A K input 75c of the flip-flop 75 receives a logical 1 from the AND gates 73d and 73f and the inverters 73i and 73j at the time of the strobe signal on the conductor 71h if the output count of the counter 72 corresponds to a decimal 12.

The output control generators 74 and 75 thus individually respond to a preselected code signal corresponding to a preselected number of pulses of the predetermined frequency sensed by the digital filter 60 and furnished to the control circuit 70. The control output flip-flop 74 provides a logical 1 at a Q output 74d at the time of the strobe signal over a conductor 77 to the switch in the equipment E in response to a transmission and receipt of three pulses of the predetermined frequency. Transmission, receipt, filtering and counting of six pulses during the time interval established by the timing circuit 71 will cause a logical 1 signal to be present at the output 74d and furnished to the switch in the equipment E, reversing the operation of such switch. In a like manner, a Q output terminal 75d of the flip-flop 75 provides a logical 1 over a conductor 78 to a switch controlling a second well control tool or equipment to be controlled by the apparatus A when nine pulses of the predetermined frequency have been transmitted, received, filtered and counted by the surface-face portion S of the apparatus A. When 12 pulses are transmitted, received, filtered and counted during the time interval control by the timing circuit 71, the output terminal 75d provides a logical 1 signal over the output conductor 78 to the switch in the second piece of equipment, reversing the operation controlled by the switch.

The power reset circuit 76 includes a current limiting resistor 76c which provides electrical current from the positive power supply terminal 76a to a pair of inputs 76d of an AND gate 76e. A resistor 76f and a capacitor 76g prevent the current from the resistor 76c from reaching the inputs 76d of the gate 76e until the capacitor 76g has charged to a sufficient level. The resistance value of the resistor 76f and the capacitance value of the capacitor 76g are chosen to be a preselected value to establish a time during which the inputs 76d of the gate 76e receive very little current, thus providing a logical 0 over an output conductor 76h to a clear input 76i of the timer circuit 71 and a clear input 74e of the flip-flop 74 and a clear input 75e of the flip-flop 75. The duration of the time for the R-C combination of resistor 76f and capacitor 76g provides a safety feature by disabling the timing circuit 71 and the output generator 74 and 75 due to the presence of a logical 0 on the inputs 71e, 74e and 75e. The presence of a logical 0 on the condenser 76h inhibits the input and receipt of signals by the timing circuit 71 on the input conductor 69a. Similarly, the presence of a logical 0 on the conductor 76h prevents the presence of a logical 1 at the output 74d and 75d of the flip-flops 74 and 75. The presence of such 0 does prevent inadvertent receipt of signals or activation of the control output generator 74 and 75 when the apparatus is at the surface before being inserted into the well, thus providing a safety feature and preventing accidents or damage to equipment or personnel in the area of the well. After the passage of time sufficient to allow the current through the resistor 76c to charge the capacitor 76g, the conductor 76h is driven to a logical 1 level in response to the current at the input 76d of the gate 76e, permitting the timing circuit 71 and the output generator 74 and 75 to operate in the manner previously set forth in response to input signals.

The foregoing disclosure and description of the invention are illustrative and explanatory thereof, and various changes in the size, shape, materials, wiring connections and contacts as well as in the details of the illustrated circuitry and construction may be made without departing from the spirit of the invention.

We claim:

1. An apparatus for controlling the operation of subsurface well drilling and well control equipment, comprising:
   a. a transmitter means for sending a predetermined number of electrical current pulses of a predetermined frequency through the earth in the vicinity of the subsurface well equipment; and
   b. subsurface equipment control means, comprising:
      1. coil means mounted with the subsurface well equipment for sensing the transmitted pulses;
      2. selective filter means for excluding and rejecting signals other than the preselected excluding frequency sensed by said coil means;
      3. control circuit means responsive to the predetermined number of pulses for generating a control signal, said control circuit means including timing means for deactivating said control circuit means in response to passage of a predetermined time interval wherein stray and spurious signals occurring outside the time interval are prevented from generating a control signal; and
4. switch means responsive to the control signal for controlling operation of the subsurface well equipment.

2. The structure of claim 1, wherein said transmitter means includes:
transmitter counter means for receiving selected input counts, said counter means controlling said transmitter means and permitting transmission of selected predetermined numbers by said transmitter means in accordance with the input count.

3. The apparatus of claim 1, wherein said selective filter means comprises:
digital filter means for timing the period of the signals sensed by said coil means, said digital filter means blocking signals by duration outside the frequency limit of said filter means, wherein stray and spurious signals are prevented from reaching said control circuit means and causing an erroneous signal to be generated.

4. The structure of claim 1, wherein said control circuit means comprises:
a plurality of control output means, each of said output means responding to an individual preselected code wherein plural selected subsurface equipment operations are individually controlled in response to the presence of the individual preselected codes.

5. The structure of claim 1, wherein said control circuit means comprises:
a. receiver counter means for counting the pulses sensed by said coil means; and
b. means for providing an output signal in response to a predetermined count in said receiver counter means to control the subsurface well equipment.

6. A method of controlling the operation of subsurface well drilling and well equipment, comprising the steps of:
a. sending a predetermined number of pulses of electrical current of a preselected frequency through the earth in the vicinity of the subsurface well equipment;
b. sensing the transmitted pulses;
c. excluding signals other than the preselected frequency of transmitted pulses;
d. generating a control signal in response to the presence of the predetermined number of pulses;
e. limiting the time interval of said step of generating to prevent stray and spurious signals from being included in said step of generating; and
f. controlling operation of the subsurface well equipment in response to the control signal.

7. The method of claim 6, further including the steps of:
a. receiving a selected input count; and
b. transmitting pulses of electrical current of the preselected frequency equal in number to the selected input count during said step of sending.

8. The method of claim 6 wherein said step of excluding includes the steps of:
a. timing the period of the signals received during said step of sensing; and
b. blocking signals of time duration outside the limits of the predetermined frequency of the pulses formed during said step of sensing.

9. The method of claim 6, wherein said step of controlling comprises the step of:
controlling a selected one of plural subsurface equipment operations in accordance with the number of pulses sent during said step of sending.

10. The method of claim 6, wherein said step of generating comprises the steps of:
a. counting the sensed pulses; and
b. generating a control signal in response to a predetermined count from said step of counting.

11. An apparatus for controlling the operation of subsurface well drilling and well control equipment, comprising:
a. transmitter means for sending a predetermined number of electrical current pulses of a preselected frequency through the earth in the vicinity of the subsurface well equipment; and
b. subsurface equipment control means, comprising:
1. coil means mounted with the subsurface well equipment for sensing the transmitted pulses;
2. selective filter means for excluding and rejecting signals other than the preselected frequency sensed by said coil means, said selective filter means comprising digital filter means for timing the period of the signals sensed by said coil means, said digital filter means blocking signals of duration outside the frequency limit of said filter means, wherein stray and spurious signals are prevented from reaching said control circuit means and causing an erroneous signal to be generated;
3. control circuit means responsive to the predetermined number of pulses for generating a control signal, said control circuit means including timing means for deactivating said control circuit means in response to passage of a predetermined time interval wherein stray and spurious signals occurring outside the time interval are prevented from generating a control signal; and
4. switch means responsive to the control signal for controlling operation of the subsurface well equipment.