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(54) **MARGIN TEST METHODS AND CIRCUITS**

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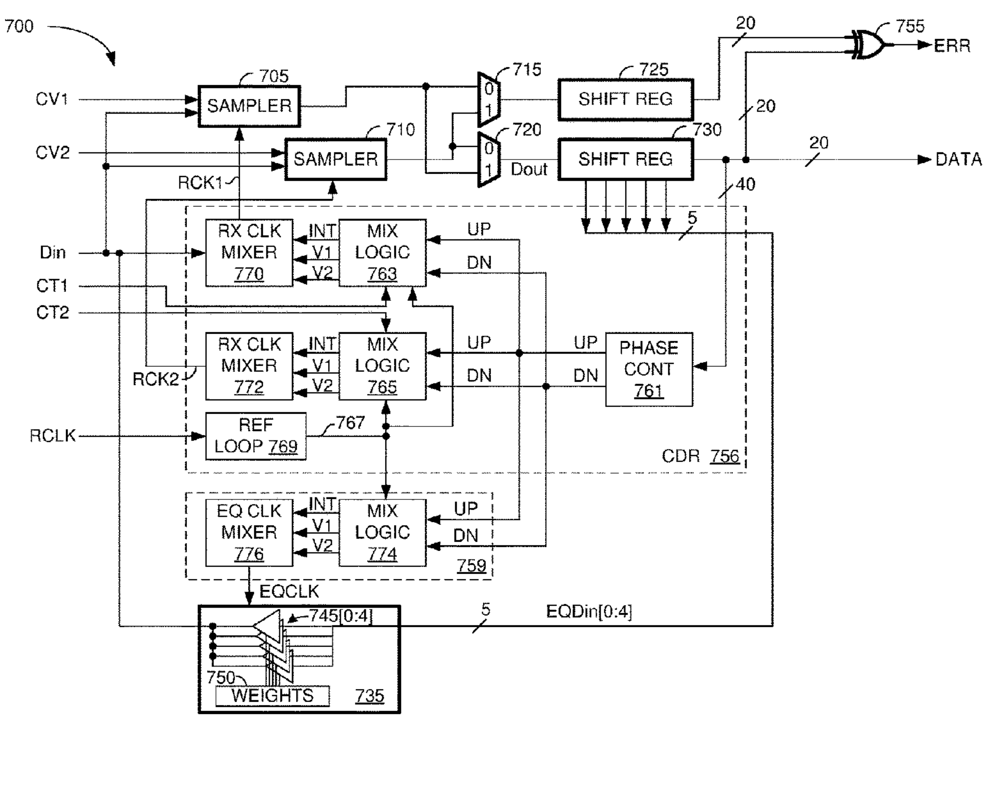
(57) **ABSTRACT**

Described are methods and circuits for margin testing digital receivers. These methods and circuits prevent margins from collapsing in response to erroneously received data and can thus be used in receivers that employ historical data to reduce intersymbol interference (ISI). Some embodiments detect receive errors for input data streams of unknown patterns and can thus be used for in-system margin testing. Such systems can be adapted to dynamically alter system parameters during device operation to maintain adequate margins despite fluctuations in the system noise environment due to e.g. temperature and supply-voltage changes. Also described are methods of plotting and interpreting filtered and unfiltered error data generated by the disclosed methods and circuits. Some embodiments filter error data to facilitate pattern-specific margin testing.



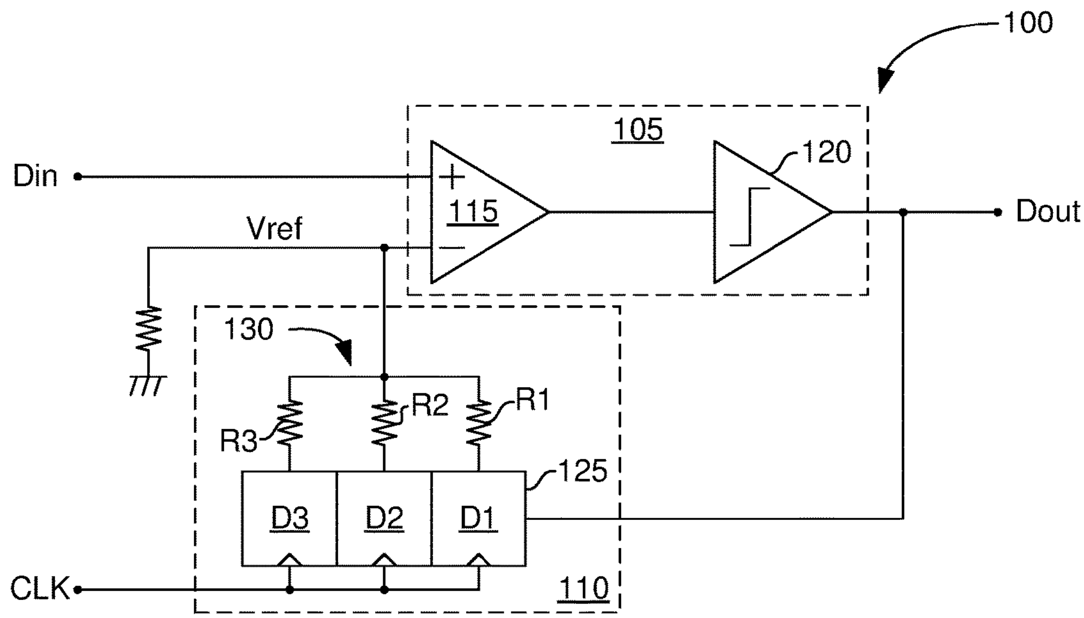


FIG. 1 (PRIOR ART)

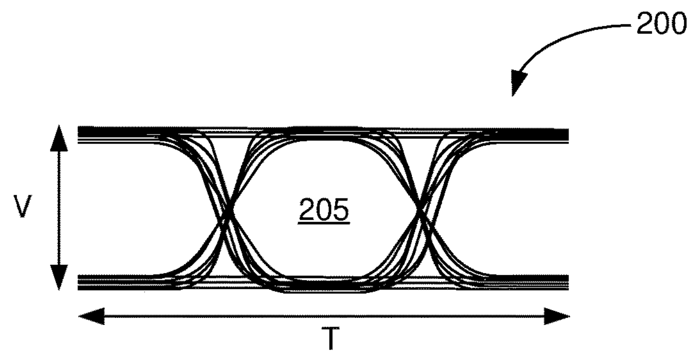


FIG. 2 (PRIOR ART)

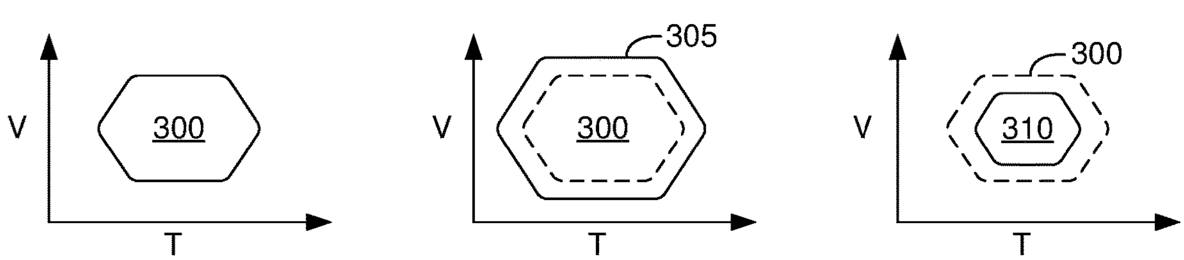


FIG. 3A (PRIOR ART) FIG. 3B (PRIOR ART) FIG. 3C (PRIOR ART)

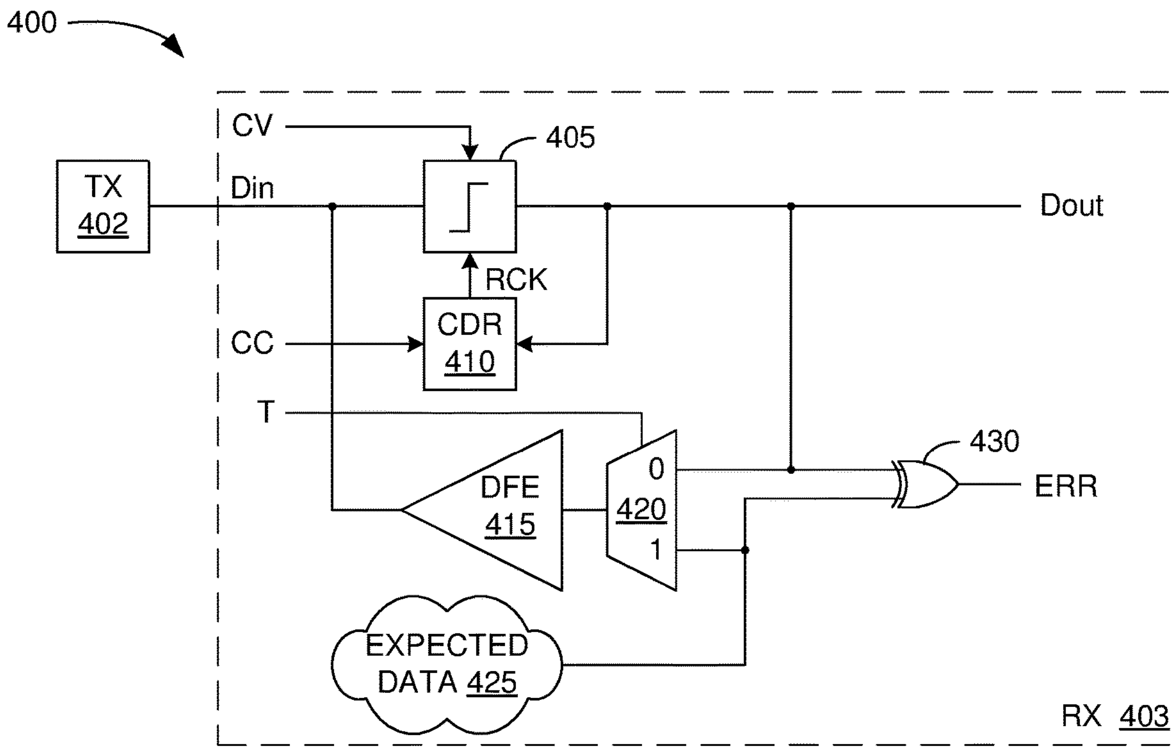

400
CV
405
TX
402
Din
Dout
RCK
CDR
410
CC
T
0
430
DFE
415
420
ERR
1
EXPECTED
DATA 425
RX 403

FIG. 4

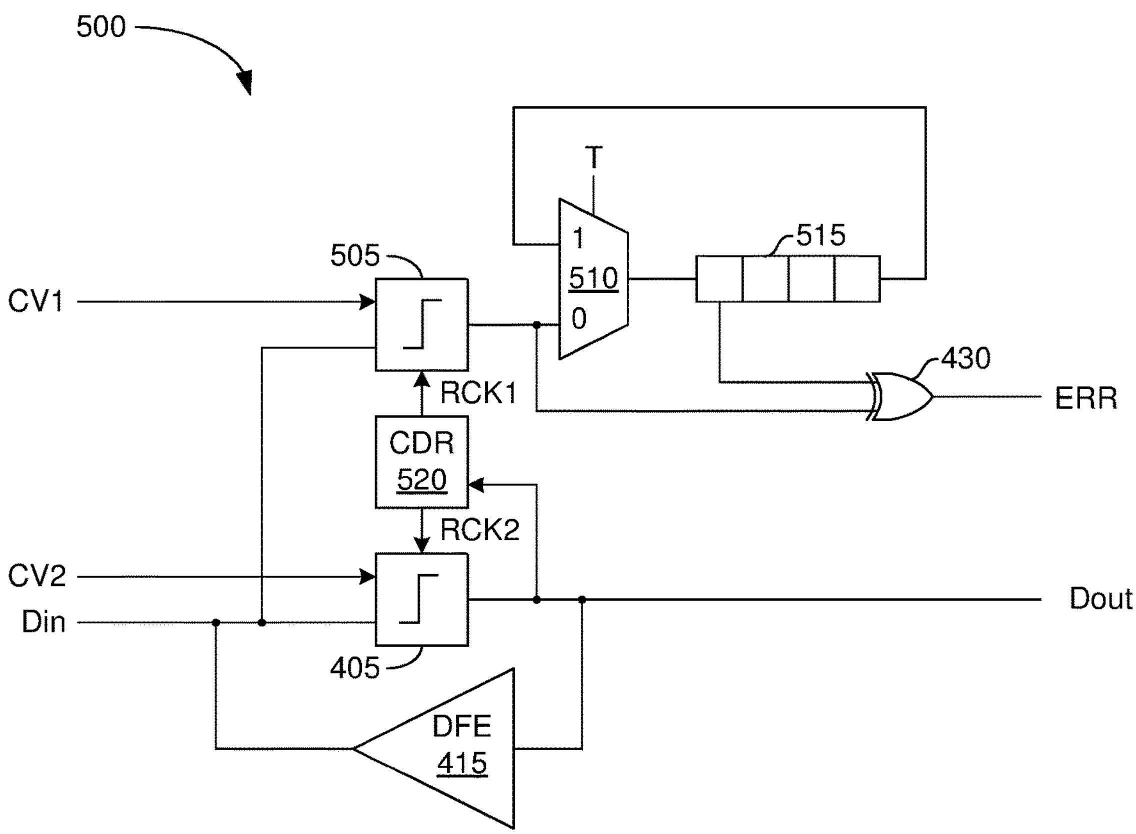

500
T
1
515
505
510
CV1
0
430
RCK1
ERR
CDR
520
RCK2
CV2
Dout
Din
405
DFE
415

FIG. 5

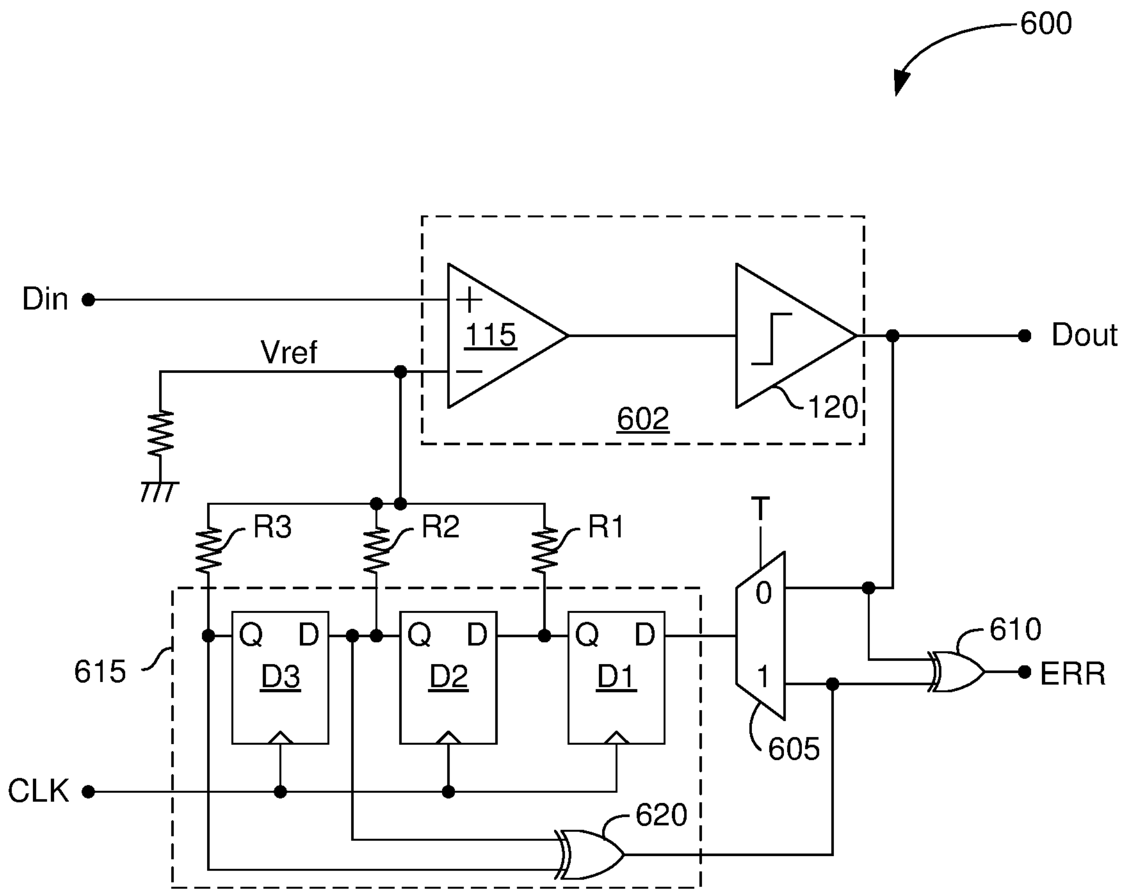

600
Din
Vref
115
120
602
Dout
R3
R2
R1
T
0
1
Q D
D3
D2
D1
615
610
ERR
605
CLK
620

FIG. 6

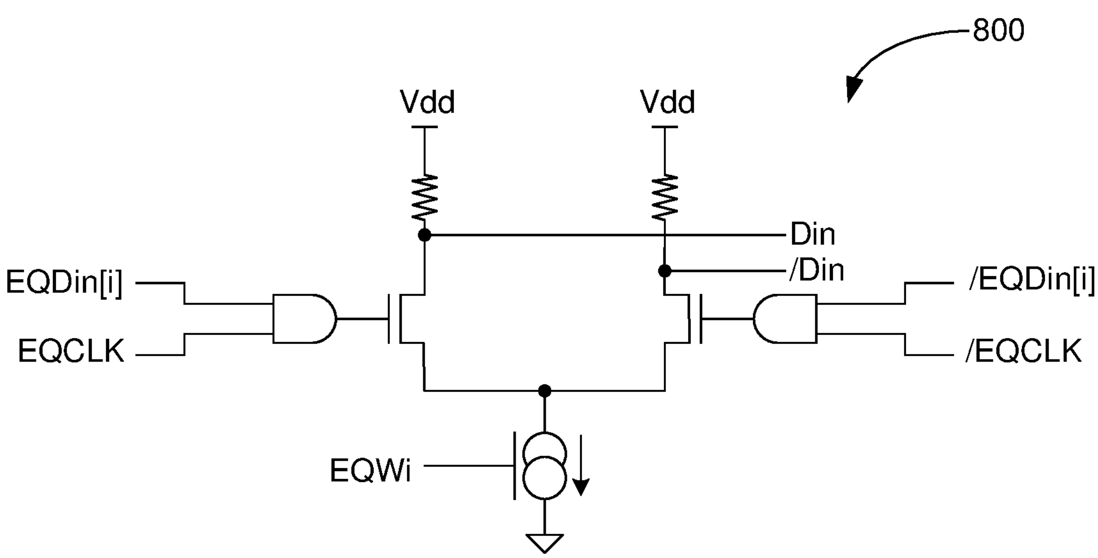
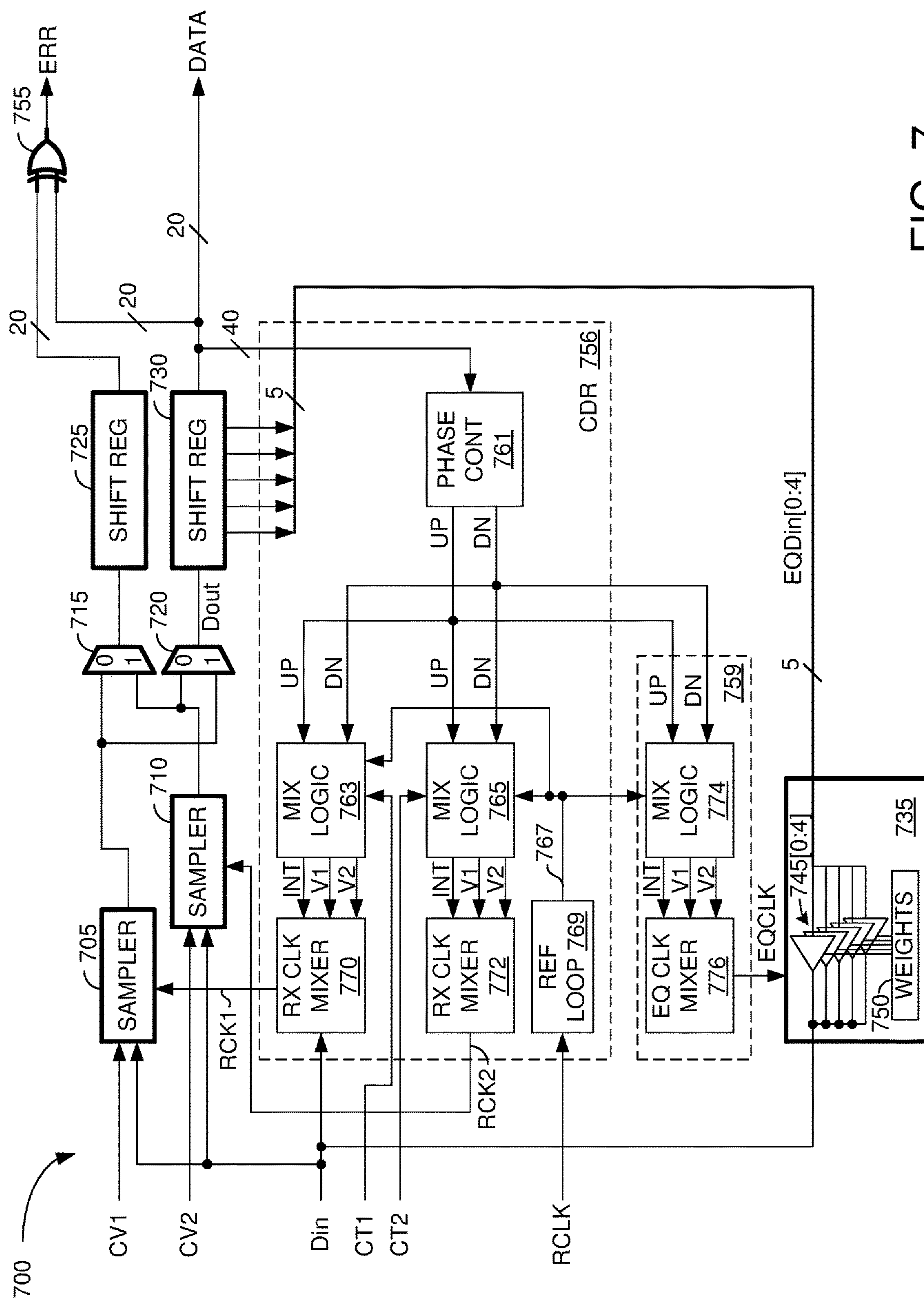

800
Vdd
Vdd
Din
/Din
EQDin[i]
EQCLK
/EQDin[i]
/EQCLK
EQWi

FIG. 8



700
CV1
CV2
Din
CT1
CT2
RCLK
SAMPLER
705
SAMPLER
710
715
720
Dout
SHIFT REG
725
SHIFT REG
730
755
ERR
DATA
20
20
20
40
5
PHASE CONT 761
UP
DN
CDR 756
MIX LOGIC 763
MIX LOGIC 765
MIX LOGIC 774
INT
V1
V2
RX CLK MIXER 770
RX CLK MIXER 772
REF LOOP 769
767
EQ CLK MIXER 776
759
RCK1
RCK2
EQCLK
EQDin[0:4]
745[0:4]
750
WEIGHTS
735

FIG. 7

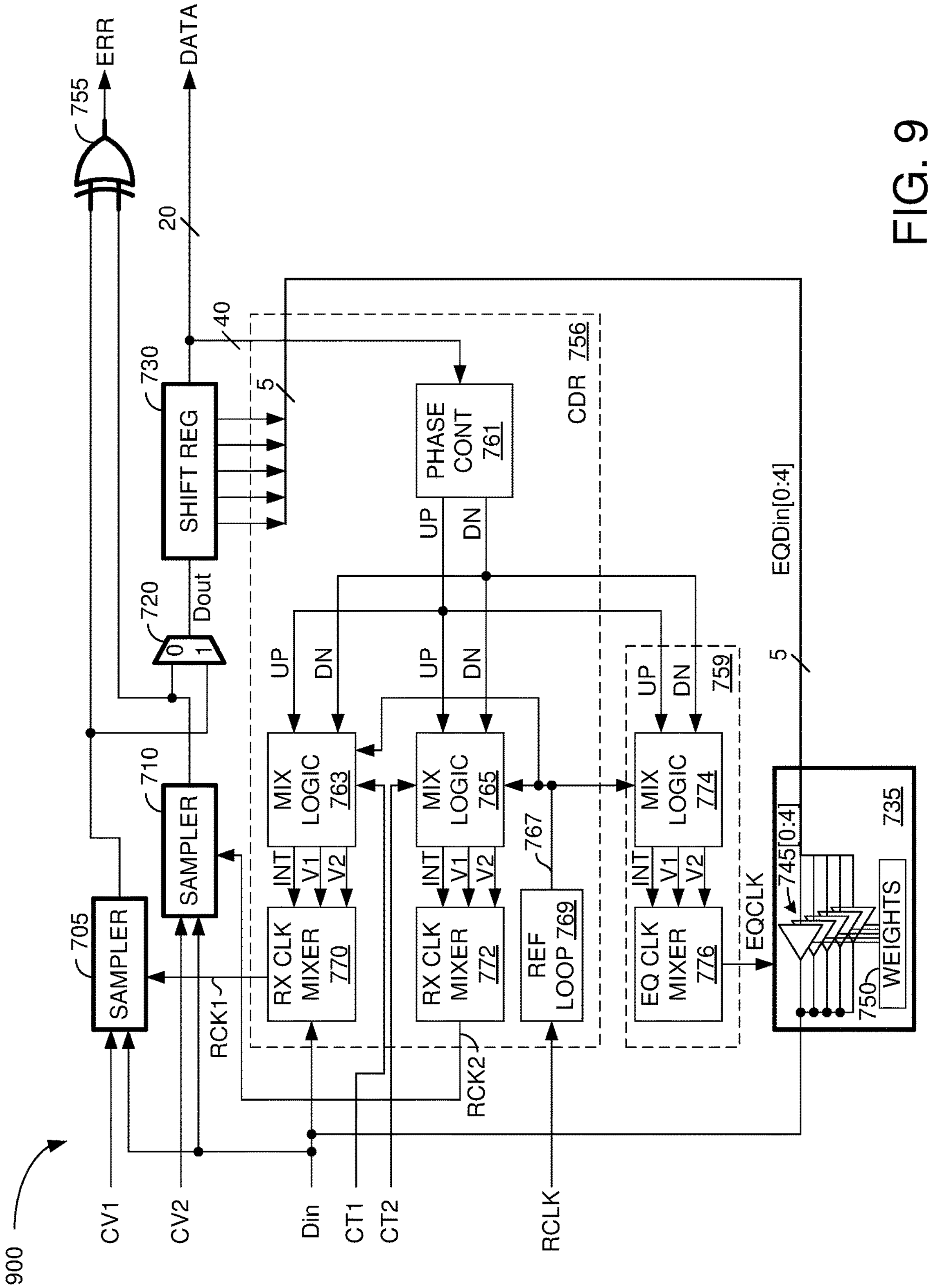

900
CV1
CV2
Din
CT1
CT2
RCLK
SAMPLER 705
SAMPLER 710
720
0
1
Dout
SHIFT REG 730
755
ERR
DATA
20
40
5
PHASE CONT 761
UP
DN
CDR 756
MIX LOGIC 763
MIX LOGIC 765
MIX LOGIC 774
759
INT
V1
V2
RX CLK MIXER 770
RX CLK MIXER 772
REF LOOP 769
767
EQ CLK MIXER 776
EQCLK
RCK1
RCK2
EQDin[0:4]
745[0:4]
750
WEIGHTS
735

FIG. 9

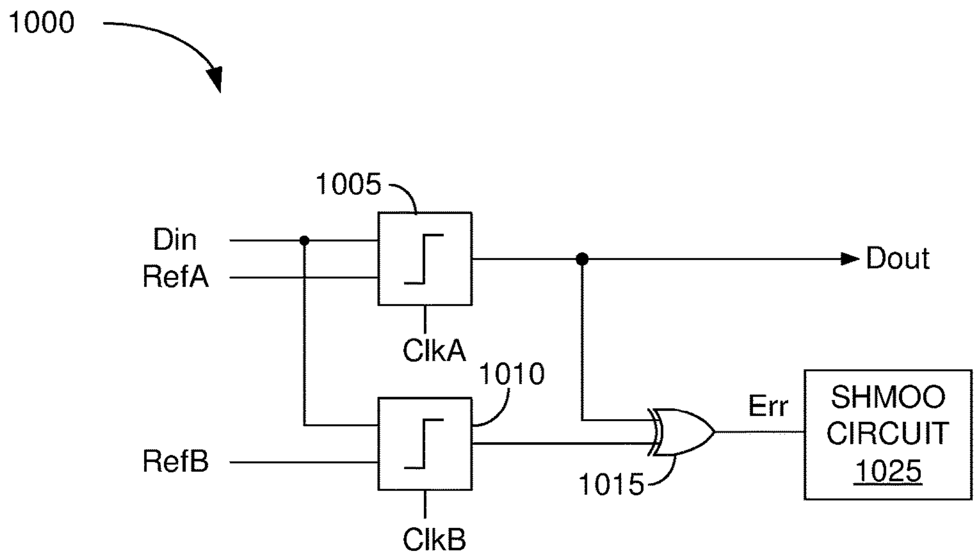


FIG. 10A

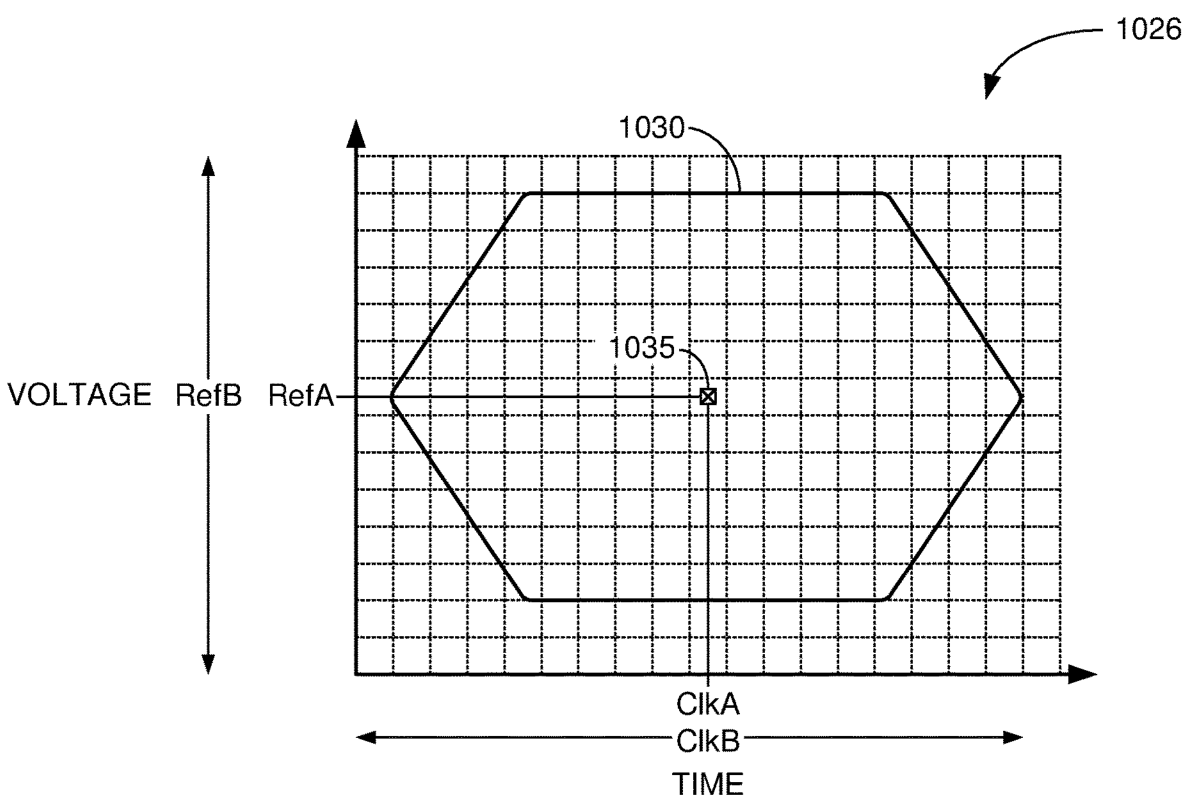


FIG. 10B

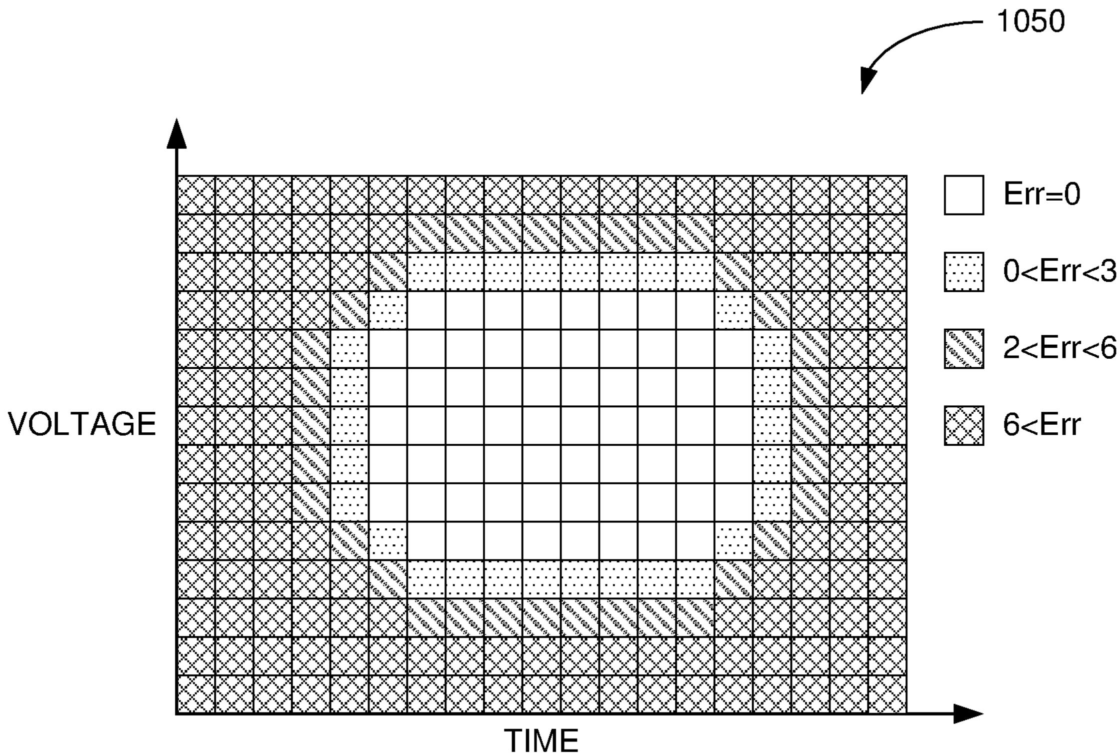


FIG. 10C

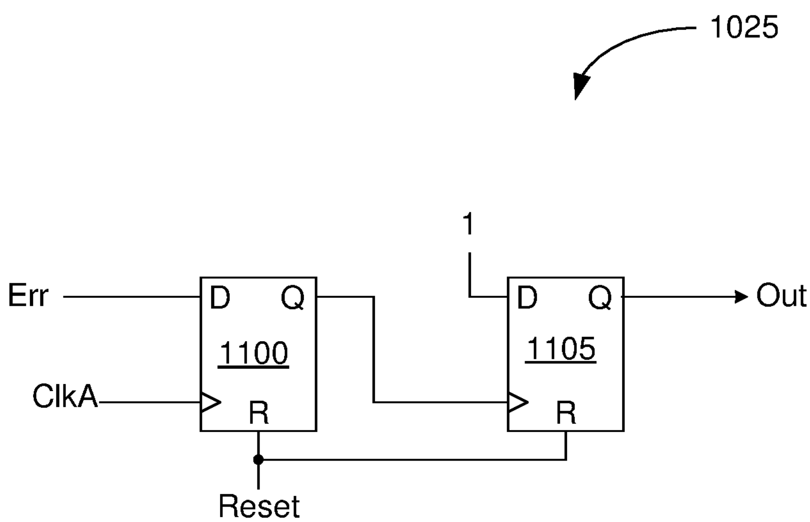


FIG. 11

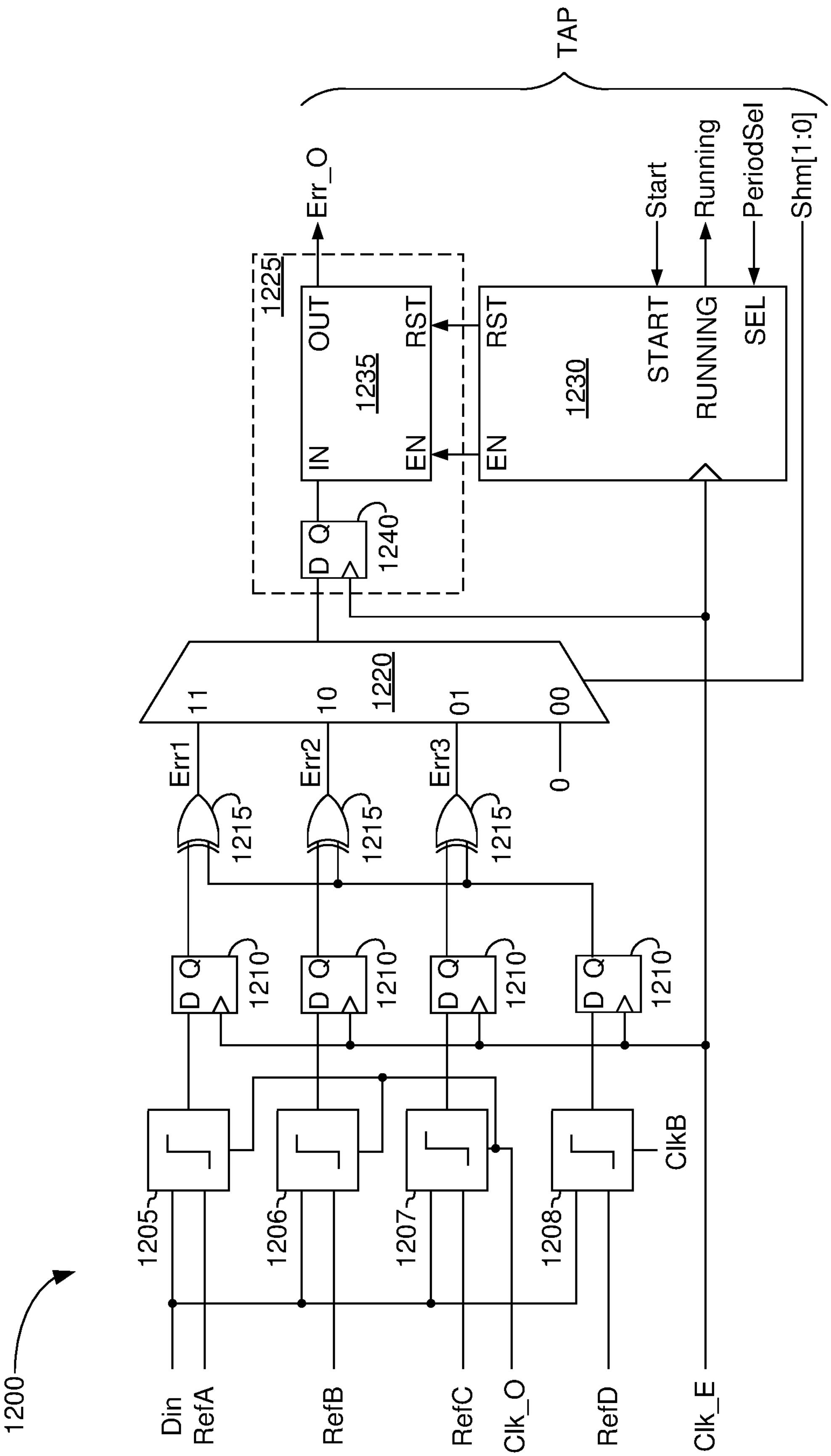

1200
Din
RefA
RefB
RefC
Clk_O
RefD
Clk_E
ClkB
1205
1206
1207
1208
1210
1215
Err1
Err2
Err3
0
11
10
01
00
1220
1225
1240
IN
OUT
1235
EN
RST
1230
START
RUNNING
SEL
Err_O
Start
Running
PeriodSel
Shm[1:0]
TAP

FIG. 12

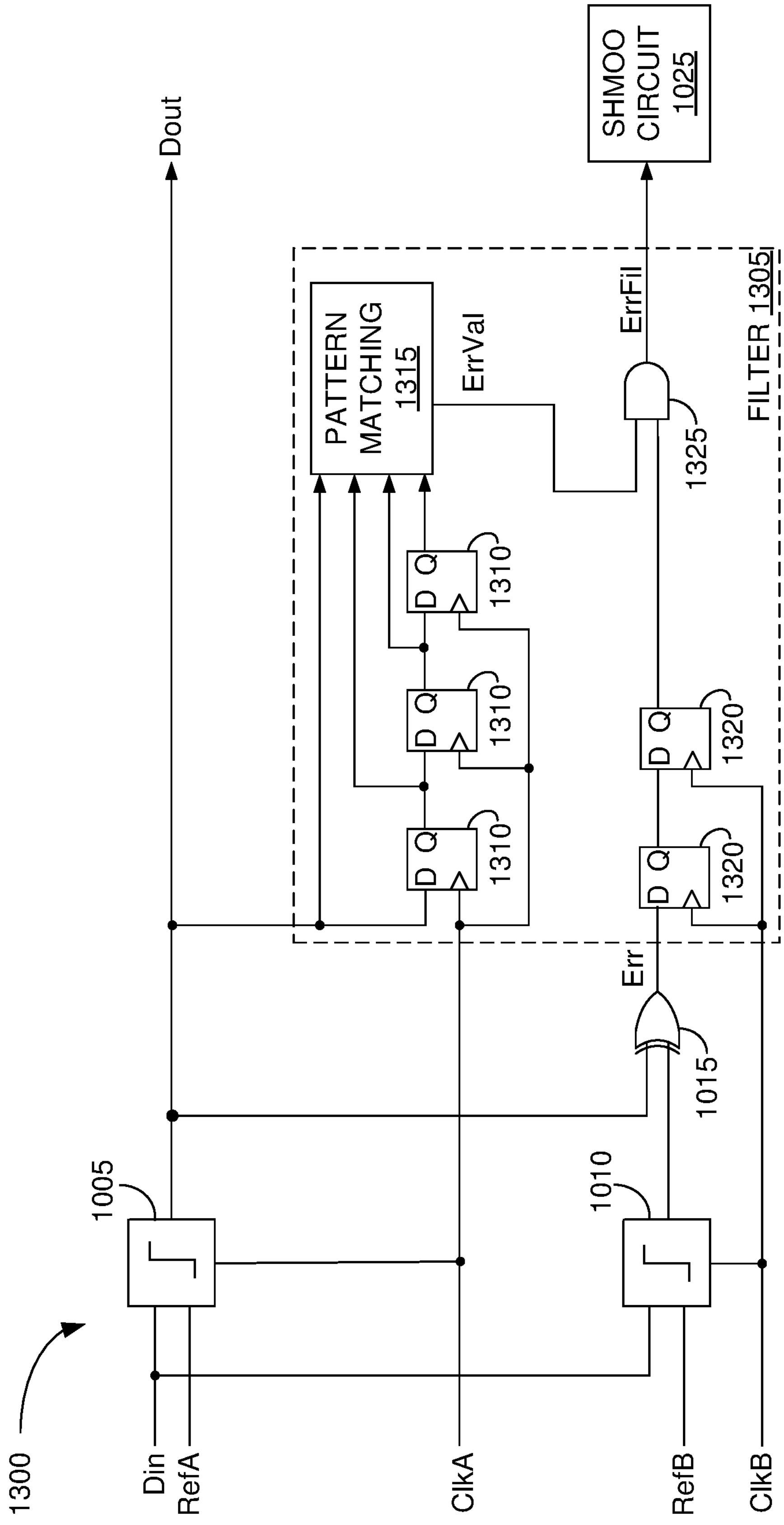

1300
Din
RefA
ClkA
RefB
ClkB
1005
1010
1015
Err
Dout
FILTER 1305
PATTERN MATCHING 1315
ErrVal
D Q
1310
1310
1310
D Q
1320
1320
1325
ErrFil
SHMOO CIRCUIT 1025

FIG. 13

MARGIN TEST METHODS AND CIRCUITS

BACKGROUND

[0001] Signal distortion limits the sensitivity and bandwidth of any communication system. A form of distortion commonly referred to as "intersymbol interference" (ISI) is particularly problematic and is manifested in the temporal spreading and consequent overlapping of individual pulses, or "symbols." Severe ISI prevents receivers from distinguishing symbols and consequently disrupts the integrity of received signals.

[0002] FIG. **1** (prior art) depicts a conventional receiver **100**, which is used here to illustrate the ISI problem and a corresponding solution. Receiver **100** includes a data sampler **105** and a feedback circuit **110**. Sampler **105** includes a differential amplifier **115** connected to a decision circuit **120**. Decision circuit **120** periodically determines the probable value of signal Din and, based on this determination, produces a corresponding output signal Dout.

[0003] Sampler **105** determines the probable value of signal Din by comparing the input signal Din to a voltage reference Vref at a precise instant. Unfortunately, the effects of ISI depend partly on the transmitted data pattern, so the voltage level used to express a given logic level varies with historical data patterns. For example, a series of logic zero signals followed by a logic one signal produces different ISI effects than a series of alternating ones and zeroes. Feedback circuit **110** addresses this problem using a technique known as Decision Feedback Equalization (DFE), which produces a corrective feedback signal that is a function of received historical data patterns.

[0004] DFE feedback circuit **110** includes a shift register **125** connected to the inverting input of amplifier **115** via a resistor ladder circuit **130**. In operation, receiver **100** receives a series of data symbols on an input terminal Din, the non-inverting input terminal of amplifier **115**. The resulting output data Dout from sampler **105** is fed back to shift register **125**, which stores the prior three output data bits. (As with other designations herein, Din and Dout refer to both signals and their corresponding nodes; whether a given designation refers to a signal or a node will be clear from the context.)

[0005] Shift register **125** includes a number of delay elements, three flip-flops D**1**-D**3** in this example, that apply historical data bits to the reference voltage side of the differential amplifier **115** via respective resistors R**1**, R**2**, and R**3**. The value of each resistor is selected to provide appropriate weight for the expected effect of the corresponding historical bit. In this example, the value of resistor R**3** is high relative to the value of resistor R**1** because the effect of the older data (D**3**) is assumed to be smaller than the effect of the newer data (D**1**). For the same reason, the resistance of resistor R**2** is between the resistors R**1** and R**3**. Receiver **100** includes a relatively simple DFE circuit for ease of illustration: practical DFE circuits may sample more or fewer historical data values. For a more detailed discussion of a number of receivers and DFE circuits, see U.S. Pat. No. 6,493,394 to Tamura et al., issued Dec. 10, 2002, which is incorporated herein by reference.

[0006] The importance of accurate data reception motivates receiver manufacturers to characterize carefully their system's ability to tolerate ISI and other types of noise. One such test, a so-called "margin" test, explores the range of voltage and timing values for which a given receiver will properly recover input data.

[0007] FIG. **2** depicts a fictional eye pattern **200** representing binary input data to a conventional receiver. Eye pattern **200** is graphed in two dimensions, voltage V and time T. The area of eye **205** represents a range of reference voltages and timing parameters within which the data represented by eye **205** will be captured. The degree to which the voltage V and time T of the sampling point can vary without introducing an error is termed the "margin."

[0008] FIGS. **3**A through **3**C depict three signal eyes **300**, **305**, and **310** illustrating the effects of DFE on margins and margin testing. Referring first to FIG. **3**A, eye **300** approximates the shape of eye **205** of FIG. **2** and represents the margin of an illustrative receiver in the absence of DFE. FIG. **3**B represents the expanded margin of the same illustrative receiver adapted to include DFE: the DFE reduces the receiver's ISI, and so extends the margins beyond the boundaries of eye **300**. Increasing the margins advantageously reduces noise sensitivity and improves bit error rates (BER).

[0009] In-system margin tests for a receiver are performed by monitoring receiver output data (e.g., Dout in FIG. **1**) while varying the reference voltage and sample timing applied to the input waveform Din. With reference to FIG. **2**, such testing samples various combinations of voltage and time to probe the boundaries of eye **205**, the boundaries being indicated when the output data does not match the input data. Margin tests thus require the receipt of erroneous data to identify signal margins. Zerbe et al. detail a number of margin tests in "Method and Apparatus for Evaluating and Optimizing a Signaling System," U.S. patent application Ser. No. 09/776,550, which is incorporated herein by reference.

[0010] A particular difficulty arises when determining the margins of DFE-equipped receivers. While feeding back prior data bits increases the margin (FIG. **3**B), the effect is just the opposite if the feedback data is erroneous. Erroneous feedback emphasizes the ISI and consequently reduces the margin, as shown in FIG. **3**C. The margin of a DFE-equipped receiver thus collapses when a margin test begins to probe the limits of the test signal (e.g., the boundaries of eye **205**). The incompatible requirements of erroneous data for the margin test and correct data for the DFE thus impede margin testing. There is therefore a need for improved means of margin testing DFE-equipped receivers.

[0011] The need for accurate margin testing is not limited to DFE-equipped receivers. Errors in margin testing lead integrated-circuit (IC) designers to specify relatively large margins of error, or "guard bands," to ensure that their circuits will perform as advertised. Unfortunately, the use of overly large margins reduces performance, an obvious disadvantage in an industry where performance is paramount. There is therefore a need for ever more precise methods and circuits for accurately characterizing the margins of high-speed integrated circuits.

SUMMARY

[0012] The present disclosure is directed to methods and circuits for margin testing high-speed receivers. Some embodiments equipped with Decision Feedback Equalization (DFE) or other forms of feedback that employ historical data to reduce inter-symbol interference (ISI) perform margin tests using a known input data stream. The receiver injects a copy of the known input data stream (i.e., the "expected data") into the feedback path irrespective of whether the receiver correctly interprets the input data. The margins are therefore maintained in the presence of receiver errors, allowing in-system margin tests to probe the margin boundaries without collapsing the margin. Receivers in accordance with some embodiments include local sources of expected data.

[0013] Other embodiments do not rely on "expected data," but can be margin tested in the presence of any pattern of received data. These embodiments are particularly useful for in-system margin testing. Also important, such systems can be adapted to dynamically alter system parameters during device operation to maintain adequate margins despite fluctuations in the system noise environment due to e.g. temperature and supply-voltage changes.

[0014] Also described are methods of plotting and interpreting error data generated by the disclosed methods and circuits. One embodiment generates shmoo plots graphically depicting the results of margin tests. Some embodiments filter error data to facilitate pattern-specific margin testing.

[0015] This summary does not limit the invention, which is instead defined by the allowed claims.

BRIEF DESCRIPTION OF THE FIGURES

[0016] FIG. **1** (prior art) depicts a conventional digital receiver **100**.

[0017] FIG. **2** depicts a fictional eye pattern **200** representing binary input data to a conventional receiver.

[0018] FIGS. **3**A through **3**C depict three signal eyes **300**, **305**, and **310** illustrating the effects of DFE on margins and margin testing.

[0019] FIG. **4** depicts a communication system **400**, including a conventional transmitter **402** connected to a DFE-equipped receiver **403** adapted in accordance with one embodiment.

[0020] FIG. **5** depicts a DFE-equipped receiver **500** adapted in accordance with an embodiment to include improved means of margin testing.

[0021] FIG. **6** depicts a receiver **600** in accordance with another embodiment.

[0022] FIG. **7** depicts a receiver **700** in accordance with yet another embodiment.

[0023] FIG. **8** depicts an embodiment of a buffer **800**, which may be used as one of amplifiers **745** in weighting circuit **735** of FIG. **7**.

[0024] FIG. **9** depicts a receiver **900** in accordance with another embodiment.

[0025] FIG. **10**A depicts a receiver **1000**, a simplified version of receiver **900** of FIG. **9** used to illustrate margin mapping in accordance with one embodiment.

[0026] FIG. **10**B is a diagram illustrating the relationship between each of samplers **1005** and **1010** of FIG. **10**A and a data eye **1030**.

[0027] FIG. **10**C depicts a shmoo plot **1050** graphically depicting an illustrative margin test in accordance with one embodiment.

[0028] FIG. **11** details an embodiment of shmoo circuit **1025** of FIG. **10**A.

[0029] FIG. **12** details a receiver **1200** in accordance with another embodiment adapted to accommodate margin shmooing.

[0030] FIG. **13** depicts a receiver **1300** that supports error filtering in accordance with another embodiment.

DETAILED DESCRIPTION

[0031] FIG. **4** depicts a communication system **400**, including a conventional transmitter **402** connected to a receiver (receive circuit) **403** equipped with Decision Feedback Equalization (DFE). In a normal operational mode, receiver **403** samples an input data stream from transmitter **402**. The sampled data provides DFE feedback to reduce intersymbol interference (ISI). In a margin-test mode, receiver **403** samples a known input data stream using ranges of sample timing and reference voltages. To prevent a collapse of the margins, the DFE feedback path disregards the potentially erroneous sampled data in favor of an identical version of the known input data stream. In-system margin tests can therefore probe the margin without collapsing the margin limits.

[0032] Receiver **403** conventionally includes a sampler **405**, an optional clock-and-data recovery (CDR) circuit **410**, and a DFE circuit **415**. During normal operation, receiver **403** receives a data stream (e.g., a series of data symbols) on sampler input terminal Din. Sampler **405** samples the data stream using a recovered clock RCK from CDR circuit **410** and produces the resulting sampled data stream on a sampler output terminal Dout. DFE circuit **415** stores a plurality of prior data samples and uses these to condition the input data in the manner discussed above in connection with FIG. **1**. In addition to the conventional components, receiver **403** includes a multiplexer **420**, an expected-data source **425**, and some comparison logic **430**, in this case an exclusive OR (XOR) gate.

[0033] During normal operation, a test control signal T to multiplexer **420** is set to a logic zero to connect the output data Dout to the input of DFE **415**. Thus configured, receiver **403** acts as a conventional DFE-equipped receiver. In a margin-test mode, however, select signal T is set to a logic one so as to convey an expected data stream from data source **425** to the input of DFE **415**. Transmitter **402** then supplies known test data on terminal Din while the expected data is applied to DFE **415**. The expected data is an identical, time-shifted version of the known data applied to input terminal Din, so DFE **415** produces the correct feedback without regard to the output signal Dout. In essence, multiplexer **420** provides the feedback path with a first input terminal for sampled output data in the operational mode and with a second input terminal for expected data in the margin-test mode.

[0034] The repeated reference herein to "terminal" Din, as opposed to the plural form "terminals," is for brevity. Receivers may include more than one data-input terminal, such as those that rely upon differential signaling. Likewise, other clock, reference, and signal paths noted herein can be single-ended, differential, etc., as will be evident to those of skill in the art. The preferred manner in which particular test circuits and methods are adapted for use with a given receiver will depend, in part, on the receiver architecture.

[0035] A voltage control signal CV on a like-named sampler input terminal alters the reference voltage used by sampler **405** to sample input data. A clock control signal CC to CDR circuit **410** modifies the timing of recovered clock signal RCK. Control signals CV and CC are used in margin testing to explore the voltage and timing margins of receiver **403**. When the margin tests reach the margin limits, and thus introduce errors in output signal Dout, expected-data source **425** continues to provide the correct DFE feedback signal and consequently prevents the margins from collapsing in response to the errors. Comparison circuit **430** monitors the sampled-data series for errors by comparing the output data with the expected data from expected-data source **425**. In the event of a mismatch, comparison circuit **430** produces a logic one error signal ERR. A sequential storage element (not shown) captures any error signal. Receiver **403** thus facilitates margin testing of DFE-equipped receivers without collapsing the margin of interest. (Error signal ERR may or may not be monitored in the operational mode.)

[0036] Expected-data source **425** produces the same data as expected on input terminal Din. Source **425** can be a register in which is previously stored a known data pattern to be provided during margin testing. Source **425** might also be a register that goes through an expected sequence of data, such as a counter or a linear-feedback shift register (LFSR). Regardless of the source, the expected data presents the expected output data, appropriately timed, to the input of the feedback circuit DFE **415**.

[0037] FIG. **5** depicts a receiver circuit **500** in accordance with another embodiment. Receiver **500** is similar in some ways to receiver **403** of FIG. **4**, like-numbered elements being the same. Receiver **500** is extended to include a second sampler **505** that is substantially identical to, and consequently mimics the behavior of, sampler **405**. The margin tests are performed on replica sampler **505** so that margin-testing circuitry has little or no impact on the performance of receiver **500** in the operational mode.

[0038] Receiver **500** includes a multiplexer **510** connected to a shift register **515**. A modified clock and data recovery circuit CDR **520** controls the timing of both samplers **505** and **405**. The timing control terminal is omitted for brevity.

[0039] Prior to a margin test, test signal T is set to logic zero and the storage elements within register **515** are loaded with an expected-data sequence. Then, in the test mode, test terminal T is set to logic one so that shift register **515** feeds its output back to its input via multiplexer **510**. To perform a margin test, sampler **505** samples input data Din. Comparison circuit **430** compares the resulting samples with the expected-data sequence provided by the first storage element in register **515**. Any difference between the data sampled by the replica sampler **505** and the expected sequence from register **515** induces comparison circuit **430** to produce a logic one error signal on line ERR. Clocking circuitry, e.g. within CDR **520**, can be adapted to control separately the recovered clock signals RCK**1** and RCK**2**.

[0040] FIG. **6** depicts a receiver **600** in accordance with another embodiment. Receiver **600** is similar to the conventional receiver **100** of FIG. **1**, but is modified to support improved margin testing.

[0041] Receiver **600** includes a sampler **602** that, like sampler **105** of FIG. **1**, includes a differential amplifier **115** and a decision circuit **120**. Although not shown, sampler **602** includes conventional means of adjusting the reference voltage and timing to support margin testing. DFE of receiver **600** performs conventionally in the operational mode and provides expected data in the margin-test mode.

[0042] Receiver **600** includes a multiplexer **605**, a comparison circuit **610**, and a dual-mode register **615**. Multiplexer **605** conveys output signal Dout to register **615** in the operational mode. Thus configured, receiver **600** functions analogously to receiver **100** of FIG. **1**. That is, register **615** shifts in the output data Dout and employs three bits of historic data to provide ISI-minimizing feedback to sampler **602**.

[0043] During margin testing, test signal T is set to logic one. In that case, multiplexer **605** provides the output of an XOR gate **620** to the input of register **615**. The inclusion of XOR gate **620** and the path through multiplexer **605** converts register **615** into a linear-feedback shift register (LFSR) that provides a pseudo-random but deterministic sequence of bits to both the input of register **615** and comparison circuit **610**. Also during the margin test, the same pseudo-random sequence produced by register **615** is provided on input terminal Din. This test sequence is applied one clock cycle ahead of the expected data in flip-flop D**1** of register **615**, so the DFE will reflect the appropriate data regardless of whether output data Dout is correct. The timing and reference voltage of sampler **602** can therefore be adjusted while monitoring output data Dout for errors without fear of collapsing the margin limits. Comparison circuit **610**, an exclusive OR gate in this example, flags any mismatches between the output data and the expected data to identify errors.

[0044] In the example of FIG. **6**, the pseudo-random sequence of test bits applied to input terminal Din is assumed to come from an external source, such as a conventional tester. The disclosed embodiments can also be adapted to support built-in self test (BIST) or in-system testing. For example, a linked transmitter/receiver pair adapted in accordance with one embodiment can margin test the intervening link. In other embodiments, receiver **600** is modified so that register **615** or another on-chip source provides the input test sequence. In some embodiments, register **615** is extended to include additional storage elements to produce more complex pseudo-random bit sequences. In such cases, the number of outputs from register **615** to the input of sampler **602** can be the same as or different from the number of storage elements employed by the LFSR. For additional details regarding LFSRs, see “What’s an LFSR,” document no. SCTA036A from Texas Instruments™ (12/1996) and the Xilinx™ application note entitled “Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators,” by Peter Alfke, XAPP 052, 7 Jul. 1996 (Version 1.1), both of which are incorporated herein by reference.

[0045] FIG. **7** depicts a receiver **700** in accordance with yet another embodiment. FIG. **7** includes a number of elements that are incidental to the inventive margin-testing circuitry, and so are only touched upon briefly here. The main components of the margin-testing circuitry are highlighted using bold outlines to distinguish them from incidental features. The emphasized components include a pair of conventional samplers **705** and **710** receiving input data on the same input terminal, Din, a pair of multiplexers **715** and **720**, a pair of shift registers **725** and **730**, and a data-weighting circuit **735**.

[0046] In the operational mode, multiplexers **715** and **720** both select their zero input. The input data Din captured by samplers **705** and **710** is thus conveyed to respective shift registers **725** and **730**. The data in shift register **730** is the output data DATA of receiver **700**, and is fed back to weighting circuit **735**. For equalization feedback, all or a subset of the bits stored in the plurality of storage elements that make up shift register **730** are provided to weighting circuit **735**. In one embodiment, shift registers **725** and **730**

each store twenty bits. Of these, five bits from register **730** are conveyed to weighting circuit **735**. The selected bits and their associated weighting are optimized for a given receiver. For a detailed discussion of methods and circuits for performing such optimization, see U.S. application Ser. No. 10/195,129 entitled "Selectable-Tap Equalizer," by Zerbe et al., filed Jul. 12, 2002, which is incorporated herein by reference. The details of that reference pertain to the optimization of a number of novel receivers. The margining methods and circuits disclosed herein may be of use in any systems that employ historical data to reduce ISI.

[0047] Weighting circuit **735** produces a weighted sum of a plurality of historical bits and applies this sum to input terminal Din. This is the same general function provided by the DFE ladder circuit of FIG. **1**, though the manner in which these weighting circuits perform this function differs significantly.

[0048] Weighting circuit **735** includes five amplifiers **745** [0:4], each of which receives a bit from shift register **730**. A weight-reference circuit **750** provides each amplifier **745** with a reference signal (e.g., a constant current) that determines the weight given to the associated bit. The output terminals of amplifiers **745**[0:4] are connected to input terminal Din to provide a weighted sum of five historical data values from shift register **730**. A current-controlled embodiment of an amplifier **745**[i] is detailed below in connection with FIG. **8**.

[0049] In the margin-test mode, each of multiplexers **715** and **720** selects its "one" input. The output of sampler **705** is thus conveyed to shift register **730** and the output of sampler **710** is conveyed to shift register **725**. Recall that a function of the margin-test mode is to provide expected data to the input of the DFE circuitry. In this case, the expected data is the input data sampled by sampler **705** and captured in shift register **730**. A voltage-control signal CV**2** and timing control signal CT**2** allow a tester or test personnel to alter the reference voltage and received clock RCK**2** as necessary to probe the margin boundaries for sampler **710**. Similar control signals CV**1** and CT**1** afford similar control over sampler **705** and are set to appropriate levels to ensure sampler **705** correctly captures the input data.

[0050] During a margin test, erroneous data bits from sampler **710** pass through shift register **725**. Comparison circuit **755** therefore produces a logic-one error signal on line ERR. In this embodiment, it is not necessary to store expected data in advance or to provide a dedicated source of expected data. Instead, the expected data is derived from input data on terminal Din sampled by sampler **705**. The sampler used to produce output data in the operational mode, sampler **710**, is the same register subjected to the margin test. Testing the receive circuitry, as opposed to a replica, is advantageous because it provides a more accurate reading of the actual receive-circuitry performance. Also important, sampler **705** can be margined in a normal operating mode, assuming that it has independent timing and voltage control relative to sampler **710**. Sampler **705** can also be margin tested and the respective sample point (voltage and timing) centered in the data eye prior to margin testing sampler **710**.

[0051] Receiver **700** of FIG. **7** is an equalizing receiver that generates receive and equalization clock signals. The following discussion outlines various features of receiver **700**. For a more detailed discussion of similar receivers, see the above-incorporated application to Zerbe et al.

[0052] In addition to the components discussed above in relation to the margin-testing methods and circuits, receiver **700** includes a CDR circuit **756** and an equalizer clock generator **759**. Samplers **705** and **710** sample incoming data signal Din in response to respective receive-clock signals RCK**1** and RCK**2**, both the which are derived from a reference clock RCLK. The samples taken by sampler **710** are shifted into register **730**, where they are stored for parallel output via output bus DATA to some application logic (not shown) and to CDR circuit **756**.

[0053] Receive clock signal RCLK includes multiple component clock signals, including a data clock signal and its complement for capturing even and odd phase data samples, and an edge clock signal and a complement edge clock signal for capturing edge samples (i.e., transitions of the data signal between successive data eyes). The data and edge samples are shifted into shift registers **725** and **730**. Samples in register **730** are then supplied as parallel words (i.e., a data word and an edge word) to a phase control circuit **761** within CDR circuit **756**. Phase control circuit **761** compares adjacent data samples (i.e., successively received data samples) within a data word to determine when data signal transitions have taken place, then compares an intervening edge sample with the preceding data sample (or succeeding data sample) to determine whether the edge sample matches the preceding data sample or succeeding data sample. If the edge sample matches the data sample that precedes the data signal transition, then the edge clock is deemed to be early relative to the data signal transition. Conversely, if the edge sample matches the data sample that succeeds the data signal transition, then the edge clock is deemed to be late relative to the data signal transition. Depending on whether a majority of such early/late determinations indicate an early or late edge clock (i.e., there are multiple such determinations due to the fact that each edge word/data word pair includes a sequence of edge and data samples), phase control circuit **761** asserts an up signal (UP) or down signal (DN). If there is no early/late majority, neither the up signal nor the down signal is asserted.

[0054] Each of a pair of mix logic circuits **763** and **765** receives a set of phase vectors **767** (i.e., clock signals) from a reference loop circuit **769** and respective timing control signals CT**1** and CT**2** as noted above. The phase vectors have incrementally offset phase angles within a cycle of a reference clock signal. For example, in one embodiment the reference loop outputs a set of eight phase vectors that are offset from one another by 45 degrees (i.e., choosing an arbitrary one of the phase vectors to have a zero degree angle, the remaining seven phase vectors have phase angles of 45, 90, 135, 180, 225, 270, and 315 degrees). Mix logic circuits **763** and **765** maintain respective phase count values, each of which includes a vector-select component to select a phase-adjacent pair of the phase vectors (i.e., phase vectors that bound a phase angle equal to 360°/N, where N is the total number of phase vectors), and an interpolation component (INT). The interpolation component INT and a pair of phase vectors V**1** and V**2** are conveyed from each of mix logic circuits **763** and **765** to respective receive-clock mixer circuits **770** and **772**. Mixer circuits **770** and **772** mix their respective pairs of phase vectors according to the interpolation component INT to generate complementary edge clock signals and complementary data clock signals that collectively constitute first and second receive-clock signals RCK**1** and RCK**2**, which serve as input clocks for samplers

705 and **710**, respectively. Timing control signals CT**1** and CT**2** facilitate independent control of the timing of clock signals RCK**1** and RCK**2**.

[0055] Mix logic circuit **765** increments and decrements the phase count value in response to assertion of the up and down signals, respectively, thereby shifting the interpolation of the selected pair of phase vectors (or, if a phase vector boundary is crossed, selecting a new pair of phase vectors) to retard or advance incrementally the phase of the receive clock signal. For example, when the phase control logic **761** determines that the edge clock leads the data transition and asserts the up signal, mix logic **765** increments the phase count, thereby incrementing the interpolation component INT of the count and causing mixer **772** to incrementally increase the phase offset (retard the phase) of receive-clock signal RCK**1**. At some point, the phase control signal output begins to dither between assertion of the up signal and the down signal, indicating that edge clock components of the receive clock signal have become phase aligned with the edges in the incoming data signal. Mix logic **763** and mixer **770** are analogous to mix logic **765** and **772**, but control the receive clock RCK**1** to sampler **705**. These redundant circuits are provided so the receive-clock timing to samplers **705** and **710** can be independently adjusted during margin testing.

[0056] The equalizer clock generator **759** receives the phase vectors **767** from the reference loop **769** and includes mix logic **774** and an equalizer clock mixer **776**, which collectively operate in the manner described above in connection with mix logic **765** and mixer **772**. That is, mix logic **774** maintains a phase count value that is incrementally adjusted up or down in response to the up and down signals from the phase control circuit **761**. The mix logic selects a phase-adjacent pair of phase vectors **767** based on a vector select component of the phase count. The mix logic then outputs the selected vectors (V**1**, V**2**) and interpolation component of the phase count (INT) to the equalizer clock mixer **776**. Clock mixer **776** mixes the selected vectors in accordance with the interpolation component of the phase count to generate the equalizer clock signal EQCLK. The equalizer clock signal, which may include complementary component clock signals, is provided to weighting circuit **735** (or another type of equalization circuit) to time the output of equalizing signals onto data input terminal Din.

[0057] FIG. **8** depicts an embodiment of a buffer **800** that may be used as one of amplifiers **745** in weighting circuit **735** of FIG. **7** in an embodiment in which the data input Din is a two-terminal port receiving differential input signals Din and /Din. Clock signal EQCLK is also a differential signal EQCLK and /EQCLK in this embodiment.

[0058] Buffer **800** receives one of five differential feedback signals (EQDin[i] and /EQDin[i]) and the differential clock signal (EQCLK and /EQCLK) from mixer **776**. Reference circuit **750** provides a reference voltage EQWi that determines the current through buffer **800**, and consequently the relative weight of the selected feedback data bit.

[0059] The above-described embodiments are adapted for use in receivers of various types. The embodiment of FIG. **6**, for example, is applied to a receiver adapted to receive single-ended input signals, while the embodiments of FIGS. **7** and **8** are applied to receivers adapted to receive complementary signals. These examples are not limiting, as these and other embodiments can be applied to receivers adapted to communicate signals in any of a number of communication schemes, including pulse-amplitude modulated (PAM) signals (e.g., 2-PAM and 4-PAM), which may be used in some embodiments to provide increased data rates.

[0060] FIG. **9** depicts a receiver **900** in accordance with another embodiment. Receiver **900** is similar to receiver **700** of FIG. **7**, like-identified elements being the same or similar. Receiver **900** differs from receiver **700** in that receiver **900** omits multiplexer **715** and shift register **725**. XOR gate **755** detects errors by comparing the data symbols from samplers **705** and **710**. As in receiver **700**, both samplers **705** and **710** can be margined in a normal operating mode. The operation of receiver **900** is otherwise similar to that of receiver **700**.

[0061] Receivers **700** and **900**, detailed in connection with respective FIGS. **7** and **9**, do not require a predetermined pattern of data (i.e., an "expected" data pattern"), and can thus be margined in the presence of the data patterns received during normal operation. The ability to detect system margins in system and without disrupting the normal flow of data enables accurate in-system margin test. In addition, receivers so equipped can be adapted to dynamically alter system parameters to maintain adequate margins.

Margin Mapping (Shmoo Plots)

[0062] FIG. **10**A depicts a receiver **1000**, a simplified version of receiver **900** of FIG. **9** used to illustrate margin mapping in accordance with one embodiment. Receiver **1000** includes two samplers **1005** and **1010**, an XOR gate **1015**, and a "shmoo" circuit **1025**. As used herein, a shmoo circuit is used to develop shmoo data, shmoo data is information that represents margin test results for a given sample point, and a shmoo plot is a graph that represents shmoo data to illustrate how a particular margin test or series of margin tests passes or fails in response to changes in the reference voltage and reference timing. Samplers **1005** and **1010** receive the same input data Din, but have independently adjustable reference voltages RefA and RefB and reference clocks ClkA and ClkB.

[0063] FIG. **10**B is a diagram **1026** illustrating the relationship between each of samplers **1005** and **1010** and a data eye **1030**. Each Cartesian coordinate on diagram **1026** represents a sample coordinate, the Y axis being representative of sample voltage and the X axis being representative of sample time. A data point **1035** is centered in data eye **1030** along both axes, and thus represents an ideal sample point for sampler **1005**.

[0064] To perform a margin test, reference voltage RefB and reference clock ClkB are adjusted along their respective Y and X axes to sample data symbols at each coordinate one or more times to probe the boundaries of eye **1030**. Margins are detected when XOR gate **1015** produces a logic one, indicating that sampler **1010** produced different data than sampler **1005**. Shmoo circuit **1025** correlates errors with the respective reference voltage RefB and clock signal ClkB for sampler **1010** and stores the resulting X-Y coordinates. Care should be taken to ensure proper clock-domain crossing of the two reference clocks ClkA and ClkB to prevent data samplers **1005** and **1010** from sampling different data eyes (e.g., to prevent respective samplers from sampling different ones of two successive data symbols). Signals RefB and ClkB can be interchanged with respective signals RefA and ClkA in FIG. **10**B to margin sampler **1010**. Methods and circuits for adjusting clock phases and reference voltages are well known in the art, and are therefore omitted here for brevity.

[0065] FIG. **10**C depicts a shmoo plot **1050** graphically depicting an illustrative margin test in accordance with one embodiment. During margin test, reference voltage RefB and reference clock ClkB are adjusted to sample incoming data at each voltage/time square (sample point) represented in FIG. **10**C. The number of errors encountered over a fixed time is then recorded for each sample coordinate. The resulting plot for a given receiver will bear a resemblance to plot **1050**, though will typically be less uniform than this illustration.

[0066] Plot **1050** can be used in a number of ways. Returning to FIG. **10**B, for example, data point **1035** is depicted in the center of eye **1030**, an ideal circumstance. Plot **1050** can be used to precisely locate the true center of eye **1030**. Once this center is known, reference voltage RefA and reference clock ClkA can be adjusted as needed to maximize the margins for sampler **1005**.

[0067] Plot **1050** can also be used to establish different margins depending upon the allowable bit-error rate (BER) for the communication channel of interest. Different communication schemes afford different levels of error tolerance. Communications channels can therefore be optimized using margin data gathered in the manner depicted in FIG. **10**C. For example, an error-intolerant communication scheme might require the zero-error margin, whereas a more tolerant scheme might be afforded the larger margin associated with a small number of errors per unit time.

Adaptive Margining

[0068] Some embodiments detect and maintain margins without storing the shmoo data graphically depicted in FIG. **10**C. One or more additional samplers can be used to probe the margins periodically or dynamically, and the sampler used to obtain the sampled data can be adjusted accordingly. In one embodiment, for example, the reference voltage and clock of the sampler used to obtain the sampled data are adjusted in response to perceived errors to maintain maximum margins. With reference to FIG. **10**A, sampler **1010** can periodically probe the high and low voltage margins and then set reference voltage RefA between them. With reference voltage RefA thus centered, the process can be repeated, this time adjusting the phase of reference clock ClkB to detect the timing margins. The phase of reference clock ClkA can then be aligned in eye **1030**. In other embodiments, additional samplers can simultaneously probe different margins of eye **1030**. Dynamic margining systems in accordance with these embodiments thus automatically account for time-variant system parameters (e.g., temperature and supply-voltage).

[0069] FIG. **11** details an embodiment of shmoo circuit **1025** of FIG. **10**A. Shmoo circuit **1025** includes a pair of flip-flops **1100** and **1105**. Flip-flop **1100** synchronizes error signal Err with a clock signal Clk. Flip-flop **1105**, a ones detector, produces a logic-one output signal OUT in response to any logic ones received from flip-flop **1100**. In operation, both flip-flops are reset to zero and error signal Err is monitored for a desired number of data samples at a given timing/voltage setting. Flip-flop **1100** captures any logic-one error signals Err, and ones detector **1105** transitions to logic one and remains there in response to any logic ones from flip-flop **1100**. A logic one output signal OUT is therefore indicative of one or more error signals received in the sample period. In other embodiments, flip-flop **1105** is replaced with a counter that counts the number of captured errors for a given period. The number and duration of the sample periods can be changed as desired.

[0070] FIG. **12** details a double-data-rate (DDR) receiver **1200** in accordance with another embodiment adapted to accommodate margin shmooing. Receiver **1200** includes four data samplers **1205-1208** timed to an odd-phase clock Clk_O, four respective flip-flops **1210** timed to an even-phase clock Clk_E, three error-detecting XOR gates **1215**, a multiplexer **1220**, error-capturing logic **1225**, and shmoo control logic **1230**. An external tester (not shown) issues test instructions and receives margin-test results via a test-access port TAP. In another embodiment, the outputs from the three flip-flops **1210** following samplers **1205**, **1206**, and **1207** connect directly to corresponding inputs of multiplexer **1220**. A single XOR gate on the output side of multiplexer **1220** then compares the selected sampler output signal with the output from sampler **1208**.

[0071] As is conventional, DDR receivers receive data on two clock phases: an odd clock phase Clk_O and an even clock phase Clk_E. Receiver **1200** represents the portion of a DDR receiver that captures incoming data using the odd clock phase Clk_O. Signals specific to only one of the clock phases are indicated by the suffix "_E" or "_O" to designate an even or odd phase, respectively. Samplers **1205**, **1206**, and **1207** are portions of the "odd" circuitry. Similar samplers are provided for the even circuitry but are omitted here for brevity. The odd and even clock phases of a DDR high-speed serial input signal can be shmooed separately or in parallel.

[0072] Receiver **1200** enters a shmoo mode at the direction of the external tester. Shmoo select signals Shm[1:0] then cause multiplexer **1220** to connect the output of one of XOR gates **1215** to the input of error-capturing logic **1225**. The following example assumes multiplexer **1220** selects error signal Err**1** to perform margin tests on sampler **1205**. Margin tests for the remaining samplers **1206** and **1207** are identical.

[0073] The external tester initiates a shmoo test cycle by issuing a rising edge on terminal Start. In response, control logic **1230** forces a signal Running high and resets a ones detector **1235** within error-capturing logic **1225** by asserting a reset signal RST. When signal Start goes low, control logic **1230** enables ones detector **1235** for a specified number of data clock cycles—the "shmoo-enable interval"—by asserting an enable signal EN. When period-select signal PeriodSel is zero, the number of data clock cycles in the shmoo-enable interval is 160 (320 symbol periods). When signal PeriodSel is one, the number of data clock cycles in the shmoo-enable interval is 128 (256 symbol periods).

[0074] The lower-most sampler **1208**, in response to control signals from the external tester, shmoos the margins for the sampler **1205** selected by multiplexer **1220**. The shmooing process is similar to that described above in connection with FIGS. **10**A, **10**B, and **10**C. The process employed by receiver **1200** differs slightly, however, in that receiver **1200** takes advantage of the presence of even clock Clk_E and flip-flops **1210** to retime the input signals to XOR gates **1215**. Even clock Clk_E is 180 degrees out of phase with respect to odd clock Clk_O. Clock signal ClkB can therefore be varied up to 90 degrees forward or backward with respect to odd clock Clk_O without fear of sampling different data symbols with the selected sampler **1205** and sampler **1208**.

[0075] The upper-most XOR gate **1215** produces a logic one if, during the shmoo-enable interval, one or more bits from sampler **1205** mismatches the corresponding bit from sampler **1208**. A flip-flop **1240** captures and conveys this logic one to ones detector **1235**. At the end of the shmoo-enable interval, controller **1230** brings signal Running low and holds that state of signal Err_O. A logic one error signal Err_O indicates to the tester that at least one mismatch occurred during the shmoo-enable interval, whereas a logic zero indicates the absence of mismatches.

[0076] The shmoo interval can be repeated a number of times, each time adjusting at least one of reference voltage RefD and clock CLKB, to probe the margins of input data Din. A shmoo plot similar to that of FIG. **10**B can thus be developed for sampler **1205**. This process can then be repeated for the remaining samplers.

[0077] Control logic **1230** does not interfere with the normal operation of receiver **1200**, so shmooing can be performed for any type of input data Din. Also advantageous, receiver **1200** allows for the capture of real data eyes under various operating conditions, and can be used to perform in-system margin tests.

[0078] Other embodiments repeat the process a number of times for each of an array of voltage/time data points to derive margin statistics that relate the probability of an error for various sample points within a given data eye. Still other embodiments replace ones detector **1235** with a counter that issues an error sum count for each shmoo-enable interval.

[0079] In one embodiment, receiver **1200** samples four-level, pulse-amplitude-modulated (4-PAM) signals presented on terminal Din, in which case each of samplers **1205**-**1207** samples the input data symbols using a different reference voltage level. In general, the methods and circuits described herein can be applied to N-PAM signaling schemes, where N is at least two. Such systems typically include N−1 samplers for each data input node.

[0080] FIG. **13** depicts a receiver **1300** that supports error filtering in accordance with another embodiment. Receiver **1300** is similar to receiver **1000** of FIG. **10**A, like-numbered elements being the same or similar. Receiver **1300** differs from receiver **1000** in that receiver **1300** includes data filter **1305** that allows receiver **1300** to shmoo particular data patterns. This is a benefit, as a receiver's margin may differ for different data patterns, due to ISI for example. Data filter **1305** allows receiver **1300** to perform pattern-specific margin tests to better characterize receiver performance.

[0081] Data filter **1305** includes a series of N data registers **1310** that provide a sequence of data samples Dout to a pattern-matching circuit **1315**. In this case N is three, but N may be more or fewer. Data filter **1305** also includes a series of M (e.g., two) error registers **1320** that convey a sequence of error samples to an input of an AND gate **1325**. AND gate **1325** only passes the error signals from registers **1320** as filtered error signal ErrFil if pattern-matching circuit **1315** asserts an error-valid signal ErrVal on the other input of AND gate **1325**. Pattern-matching circuit **1315** asserts signal ErrVal only if the pattern presented by registers **1310** matches some predetermined pattern or patterns stored in pattern-matching circuit **1315**. In one embodiment external test circuitry (not shown) controls the patterns provided by matching circuit **1315**. Other embodiments support in-system testing with one or more patterns provided internally (e.g., on the same semiconductor chip).

[0082] Some of the foregoing embodiments employ an additional sampler to probe the margins of a given data input. Some receiver architectures already include the requisite additional sampler, to support additional signaling modes, for example. Other embodiments may be adapted to include one or more additional "monitor" samplers.

[0083] While the present invention has been described in connection with specific embodiments, variations of these embodiments will be obvious to those of ordinary skill in the art. Moreover, unless otherwise defined, terminals, lines, conductors, and traces that carry a given signal fall under the umbrella term "node." In general, the choice of a given description of a circuit node is a matter of style and is not limiting. Likewise, the term "connected" is not limiting unless otherwise defined. Some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance, the method of interconnection establishes some desired electrical communication between two or more circuit nodes, or terminals. Such communication may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. Furthermore, only those claims specifically reciting "means for" or "step for" should be construed in the manner required under the sixth paragraph of 35 U.S.C. section 112. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description.

1. (canceled)

2. A receiver circuit comprising:

a sampler having:
- a sampler input terminal to receive a series of symbols;
- a sampler reference terminal to receive a reference signal against which to compare the series of symbols; and
- a sampler timing terminal to receive a timing signal;
- the sampler to sample the series of symbols with reference to the reference signal in time with the timing signal to produce a series of samples;

comparison logic having:
- a first comparison-logic input terminal coupled to the sampler to receive the series of samples;
- a second comparison-logic input terminal; and
- a comparison-logic output terminal;

a multiplexer having:
- a first multiplexer input terminal coupled to the sampler to receive the series of samples;
- a second multiplexer input terminal; and
- a multiplexer output terminal; and

a shift register having:
- a shift-register input terminal coupled to the multiplexer output terminal; and
- at least one shift-register output terminal coupled to the second multiplexer input terminal and the second comparison-logic input terminal.

3. The receiver circuit of claim **2**, wherein the timing signal comprises a recovered clock signal.

4. The receiver circuit of claim **2**, further comprising a second sampler having:
- a second sampler input terminal to receive the series of symbols;
- a second sampler reference terminal to receive a second reference signal against which to compare the series of symbols;
- a second sampler timing terminal to receive a second timing signal; and
- a second sampler output terminal to produce a second series of samples.

5. The receiver circuit of claim **4**, further comprising timing circuitry to adjust the timing signal relative to second timing signal.

6. The receiver circuit of claim **5**, the timing circuitry having a timing-circuitry input terminal coupled to the second sampler output terminal, the timing circuitry to recover the second timing signal responsive to the second series of samples.

7. The receiver circuit of claim **4**, further comprising a decision-feedback equalizer coupled between the second sampler output terminal and the second sampler input terminal, the decision-feedback equalizer to equalize the series of symbols responsive to the second series of samples.

8. The receiver circuit of claim **7**, further comprising a shmoo circuit coupled to the second sampler output terminal and the comparison-logic output terminal, the shmoo circuit to correlate error signals from the comparison-logic output terminal with the second series of samples.

9. The receiver circuit of claim **2**, the comparison-logic output terminal produce mismatch signals, the receiver further comprising a filter to exclude the mismatch signals as errors unless the series of samples matches a with a pattern.

10. A method of calibrating a receiver circuit, the receiver circuit comprising a sampler to produce a first series of samples responsive to a first series of symbols and a second series of samples responsive to a second series of symbols, the method comprising:

- sampling the first series of symbols relative to a first reference to produce the first series of samples;
- storing the first series of samples in a shift register;
- feeding an output of the shift register to an input of the shift register to produce an expected-data sequence;
- sampling the second series of symbols relative to a second reference different from the first reference to produce a second series of samples; and
- comparing the expected-data sequence with the second series of samples.

11. The method of claim **10**, further comprising varying the second reference during the comparing.

12. The method of claim **11**, further comprising flagging mismatches between the expected-data sequence and the second series of samples and correlating the mismatches with the second reference.

13. The method of claim **12**, wherein the second reference comprises at least one of a voltage reference and a timing reference.

14. The method of claim **12**, further comprising storing shmoo data responsive to the mismatches.

15. The method of claim **10**, further comprising comparing at least one of the expected-data sequence and the second series of samples with a pattern to identify pattern matches and flagging mismatches between the expected-data sequence and the second series of samples responsive to the pattern matches.

16. The method of claim **10**, further comprising recovering the first reference and the second reference from at least one of the first series of symbols and the second series of symbols.

17. A receiver circuit comprising:

- a sampler having:
  - a sampler input terminal to receive a series of symbols;
  - a sampler reference terminal to receive a reference signal against which to compare the series of symbols; and
  - a sampler timing terminal to receive a timing signal;
  - the sampler to sample the series of symbols with reference to the reference signal in time with the timing signal to produce a series of samples;
- means for loading a shift register with a sequence of expected data from the series of samples; and
- means for comparing the sequence of expected data with incoming ones of the series of samples while looping the sequence of expected data through the shift register and changing at least one of the reference signal and the timing signal, the means for comparing identifying mismatches between the sequence of expected data and the series of samples.

18. The receiver circuit of claim **17**, further comprising means for correlating the mismatches between the sequence of expected data and the series of samples with the at least one of the reference signal and the timing signal.

19. The receiver circuit of claim **18**, further comprising a means for correlating patterns of the series of symbols with the mismatches.

20. The receiver circuit of claim **17**, further comprising a means for recovering the timing signal from the series of symbols.

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