United States Patent [19]

Zitelli et al.

[11] **3,860,914**

[45] **Jan. 14, 1975**

[54] **DIGITAL DATA RECORDER**

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[73] Assignee: **Westinghouse Electric Corporation,** Pittsburgh, Pa.

[22] Filed: **Jan. 8, 1973**

[21] Appl. No.: **321,910**

[52] **U.S. Cl.**..... **340/172.5,** 307/282, 340/174 SR

[51] **Int. Cl.**..... **G06f 1/00**

[58] **Field of Search**..... 340/172.5, 174 SR, 174 FA; 307/282; 328/39.5

[56] **References Cited**

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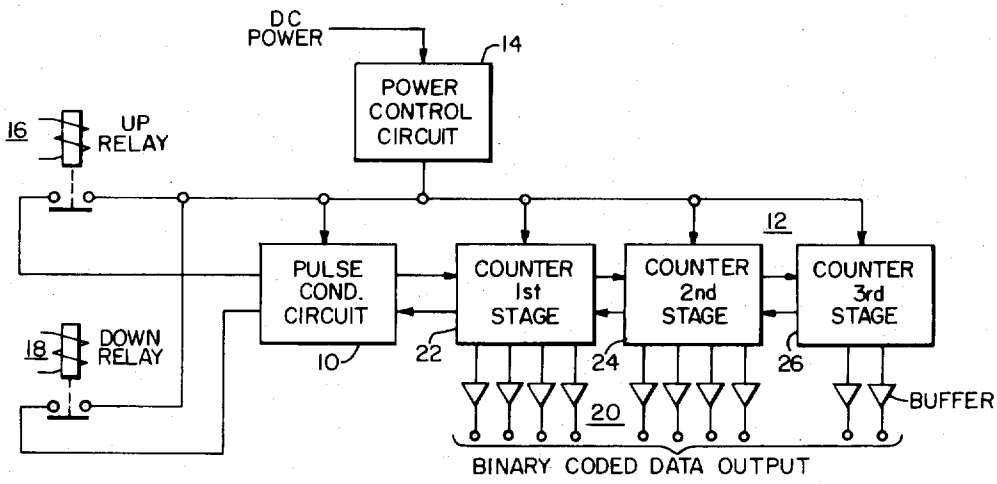
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Primary Examiner—Harvey E. Springborn
Attorney, Agent, or Firm—D. C. Abeles

[57] **ABSTRACT**

A digital data recorder is described having inherent circuitry characteristics that will re-establish the recorded data state previously established just prior to a power failure upon the return of the source power supply. The retentive characteristics of the recorder are supplied from an arrangement of magnetic memory cores which controllably vary the time constants associated with given portions of the circuitry of a digital counter comprising the major subunit of this invention. In one embodiment the counter is supplied with a zero inhibit to prevent reverse counting past the zero output state, thus preventing a false indication of the recorded data. The circuitry thus described, basically comprising solid state elements, provides a compact, resilient unit with no mechanical moving elements.

5 Claims, 11 Drawing Figures



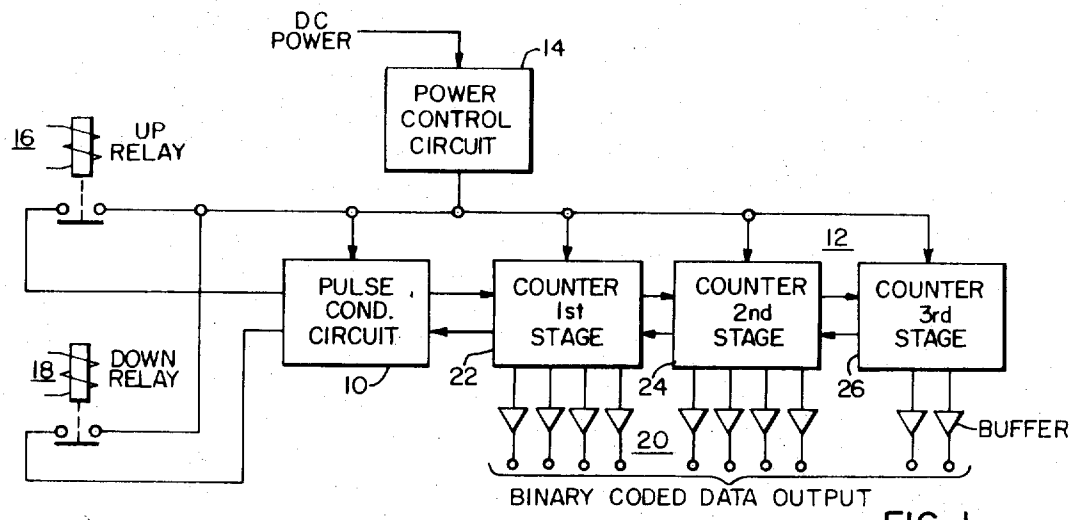


FIG. 1

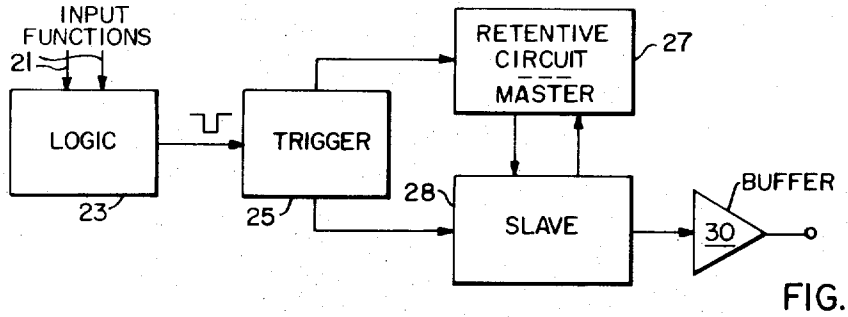


FIG. 2

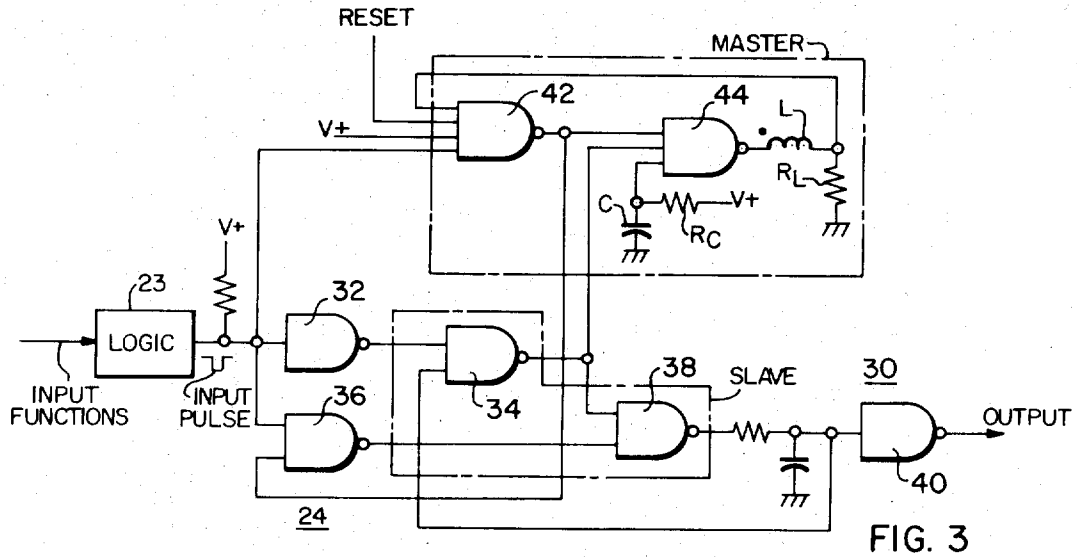


FIG. 3

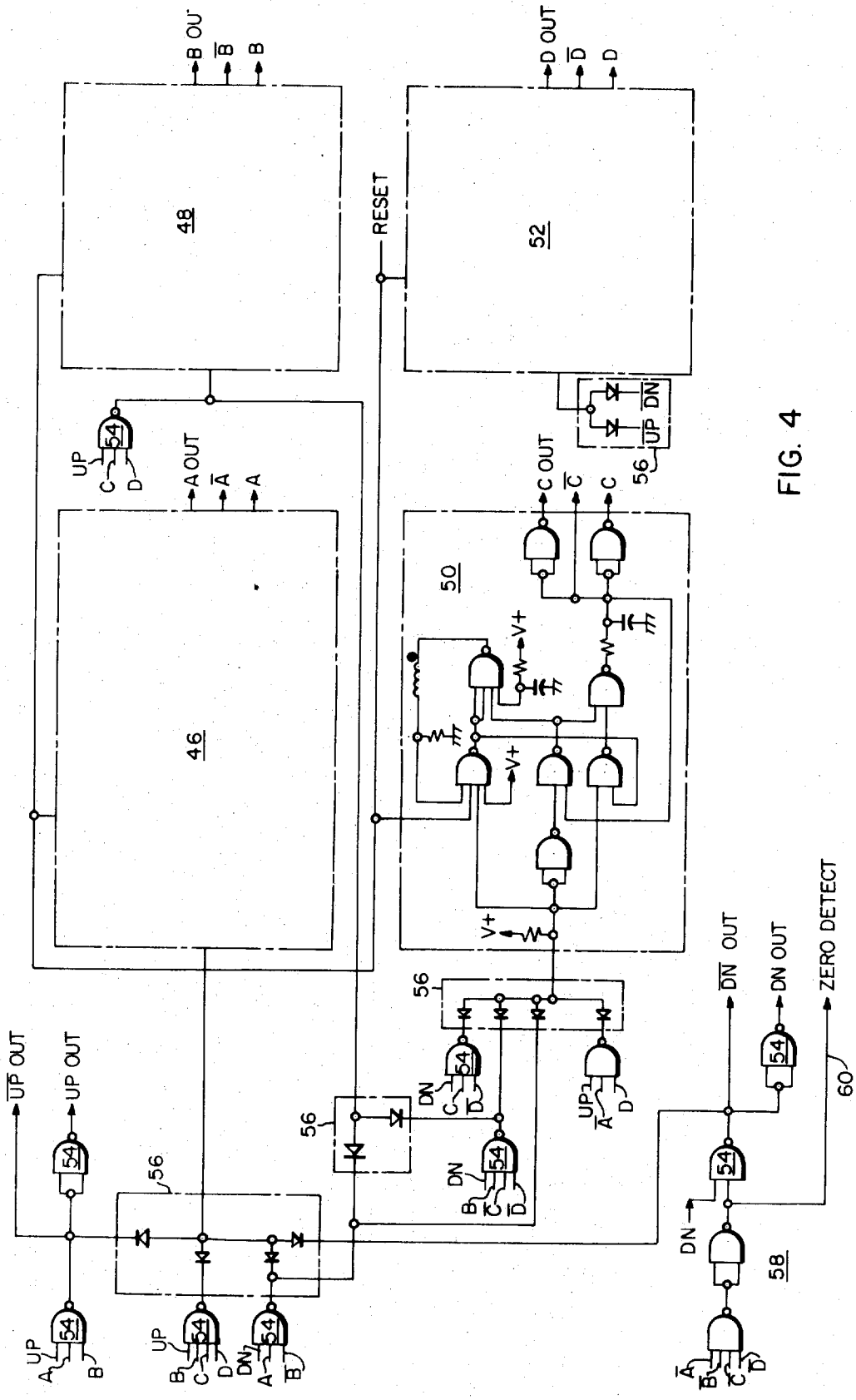

B OUT
D OUT
RESET
48
52
46
50
A OUT
C OUT
UP
DN
UP OUT
DN OUT
ZERO DETECT
54
56
58
60
V+

FIG. 4

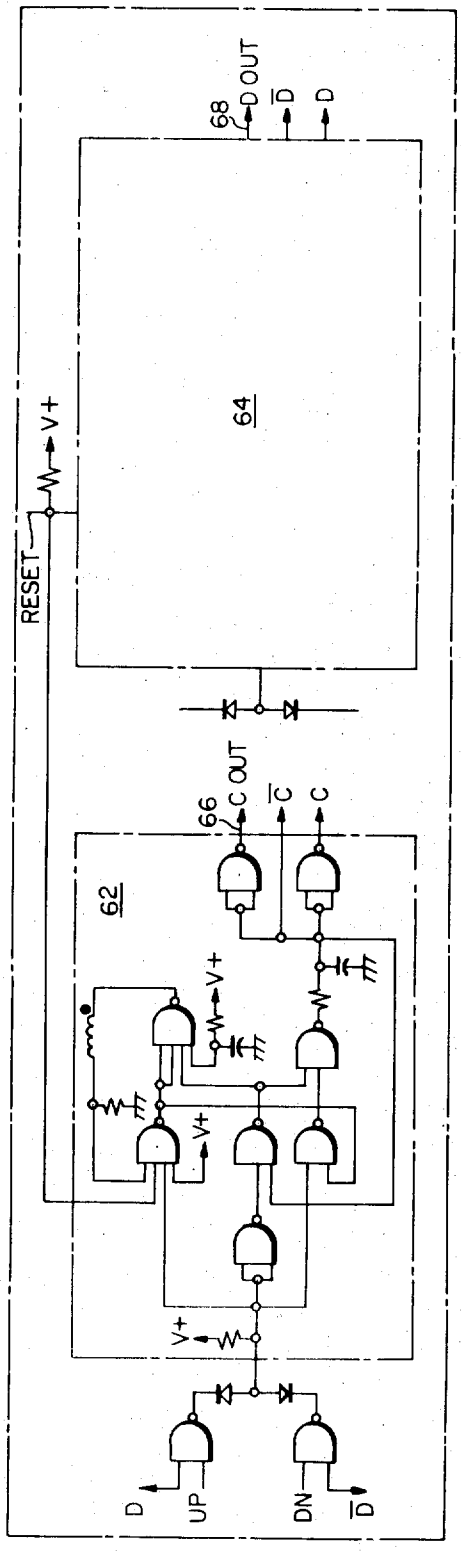

68
D OUT
$\overline{D}$
D
64
RESET
V+
66
C OUT
$\overline{C}$
C
62
V+
V+
V+
D
UP
DN
$\overline{D}$

FIG. 5

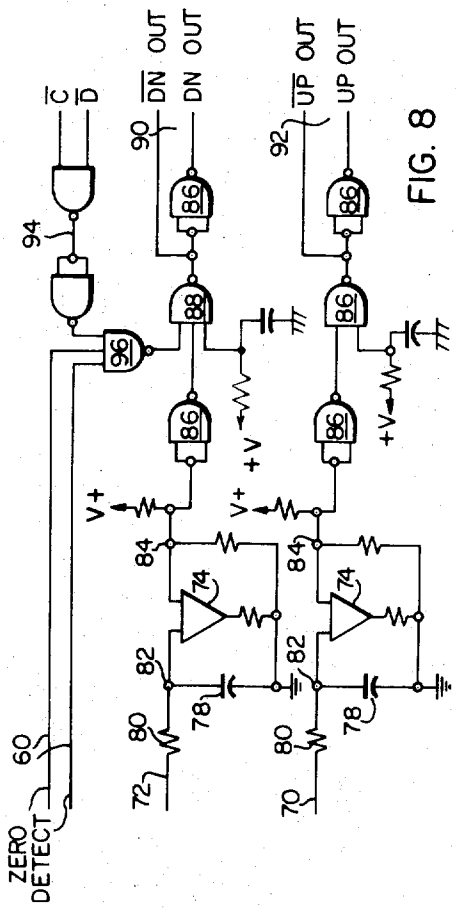

$\overline{C}$
$\overline{D}$
94
90
$\overline{DN}$ OUT
DN OUT
92
$\overline{UP}$ OUT
UP OUT
86
88
96
+V
V+
84
74
82
78
80
72
70
60
ZERO DETECT

FIG. 8

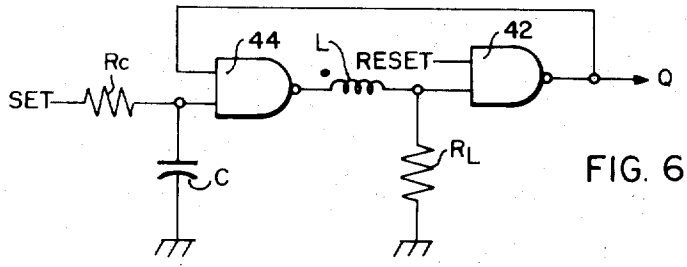


FIG. 6

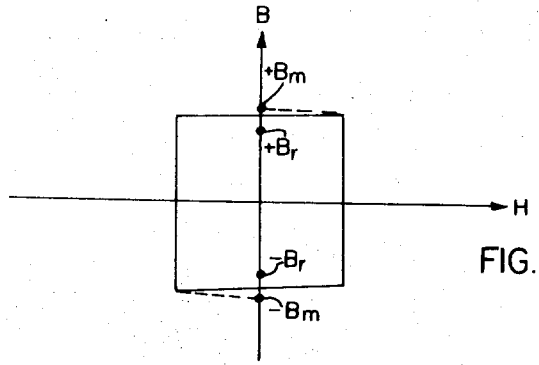


FIG. 7

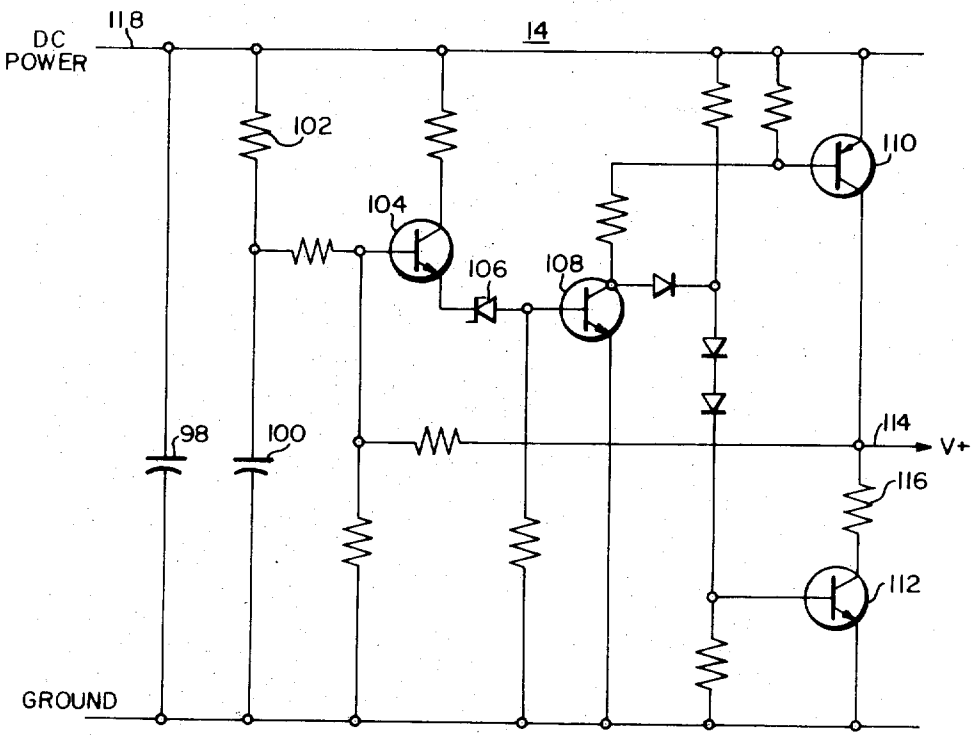
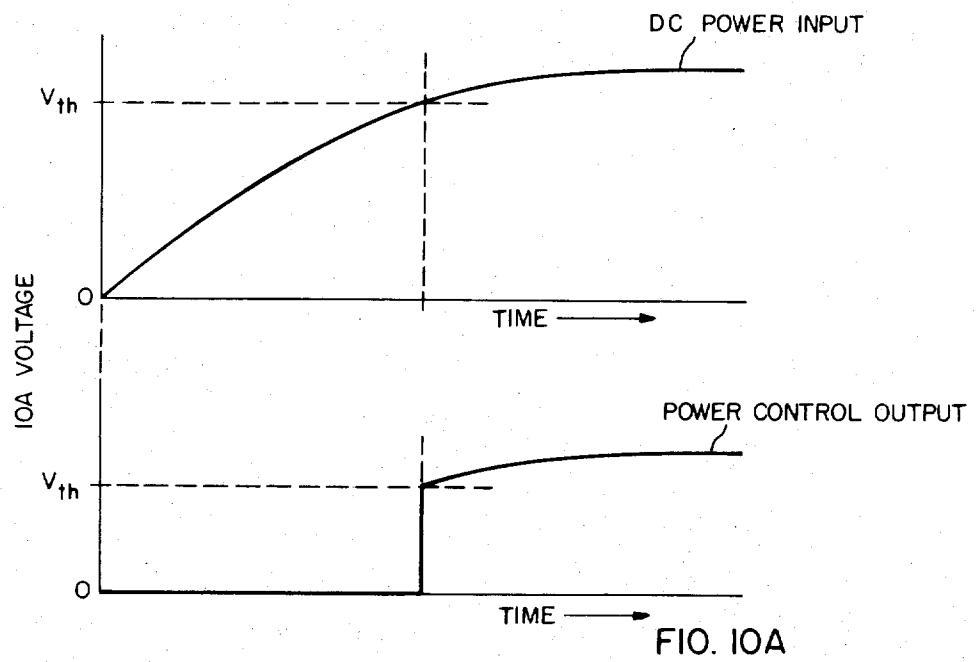


FIG. 9



FIO. IOA

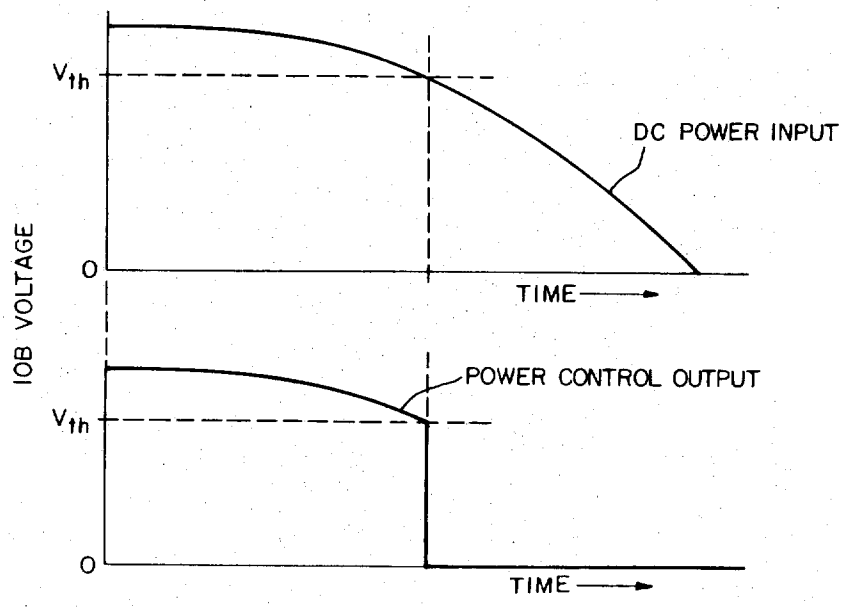


FIG. IOB

DIGITAL DATA RECORDER

BACKGROUND OF THE INVENTION

The present invention is related in general to digital data recorders and more particularly to such recorders that retain data information for later presentation upon loss of the recorder supply voltage.

In a nuclear reactor power plant, the plant power demand controls adjustment of the position of control rod banks within the reactor. An important safety feature in the operation of the plant is the ability to record the required control rod bank position and secure this information in the event of a loss of power to the recorder.

The rod position demand data is independent of the actual rod position data obtained from sensors positioned along the control rod housing and therefore it is specifically desirable to record the rod position demand data so that it can be compared with the actual rod position to insure that the rods are following their respective control signals. Additionally, in the event of a plant power supply failure, the apparatus assigned to record data will be required to maintain the information for presentation upon the resumption of power to enable the plant operator to determine the rod position demand at the time of failure.

At present, there are two designs of apparatus available for supplying the desired data recorder characteristics; both electromechanical. The first utilizes pulsed signals generated from relay contact closures to simulate discrete rod movement demands. The pulsed signals are communicated to a solenoid, which when energized, mechanically forces a stepping relay in the form of a wheel to be rotated one step. The wheel is numbered from zero to nine and is mechanically connected to other similarly numbered wheels geared in a manner to record and display a decimal output count. The decimal number is then representative of the position demand of the rod control bank. Since the stable output states of the counter are independent of the source power supply, the data can be maintained irrespective of a loss of plant power.

In the second arrangement pulsed signals generated from relay contact closures representative of discrete rod movement demands are communicated to a pulse conditioning circuit. This circuit modifies the pulses to drive an up-down counter formed basically from diode transistor logic gates. The outputs of the counter are then connected to relay drivers which energize latching reed relays. The digital output displayed by the latching reed relays is then proportional to the rod position demand and is retained in the state of the relays which can only be altered by further pulsing of the counter. In the manner, any loss of power to the system will not result in loss of the recorded information.

While both apparatus designs will theoretically function as desired they are subject to most of the deficiencies associated with electromechanical equipment in that they are bulky and subject to increased wear due to the adverse operating environment encountered within a reactor containment. The electromechanical characteristics exhibited by the prior art recorder designs thus render the output information suspect unless the equipment is continually checked.

SUMMARY OF THE INVENTION

Briefly, this invention provides a compact, resilient, electronic, digital data recorder having the inherent circuitry characteristics of re-establishing the recorded data state previously established just prior to a power failure upon the return of the source power supply. The retentive features of the recorder are supplied from a novel arrangement of magnetic memory cores which controllably vary the time constants associated with part of the recorder circuitry within the feedback loops of an incorporated digital counter. In one embodiment, the counter is supplied with a zero state inhibit to prevent counter stepping in reverse count past the zero data output state, which would otherwise exhibit itself as a false indication of the recorded data. The entire recorder unit, excluding memory cores, is amenable to solid state construction and is operable in extremely adverse environments, such as are found in nuclear reactor applications, to provide a reliable and durable output function.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, reference may be had to the preferred embodiment, exemplary of the invention, shown in the accompanying drawings, in which:

FIG. **1** is a block diagram of one embodiment of the data recorder of this invention;

FIG. **2** is a block diagram of a one bit stage of the counter identified in FIG. **1**;

FIG. **3** is a schematic circuitry diagram of the one bit stage previously identified in FIG. **2**;

FIG. **4** is a schematic circuitry diagram of the first two stages of the counter identified in FIG. **1**;

FIG. **5** is a schematic circuitry diagram of the third stage of the counter previously identified in FIG. **1**;

FIG. **6** is a simplified schematic circuitry diagram illustrative of the retentive characteristics of the circuits previously described in FIGS. **4, 5** and **6**;

FIG. **7** is a graphical illustration of the hysteresis loop of the magnetic memory core utilized in the circuits of FIGS. **4, 5** and **6**;

FIG. **8** is a schematic circuitry diagram of the pulse conditioning circuit previously identified in FIG. **1**;

FIG. **9** is a schematic circuitry diagram of the power control circuit previously identified in FIG. **1**; and

FIGS. **10A** and **10B** show graphical illustrations of the input and output signals exhibited by the circuit of FIG. **9** in response to changes in the source supply voltage.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In order to overcome the disadvantages of the prior art this invention provides a compact, resilient, electronic, digital data recorder having the inherent circuitry characteristics of re-establishing the recorded data state previously established just prior to a power failure upon the return of the source power supply. The recorder, excluding a novel arrangement of saturable magnetic cores within an incorporated digital counter, is amenable to solid state construction and the entire unit is operable in extremely adverse environments, such as are found in nuclear reactor applications, to provide a reliable and durable output function.

The preferred embodiment of this invention will therefore be described within a reactor environment, to best illustrate its advantageous characteristics.

Most nuclear reactors utilize three types of neutron absorber rods respectively known as shut down rods, part length rods and control rods. With each type of rod there is associated a number of rod banks, and within each bank there is contained a number of rod mechanisms. An example of such a nuclear reactor rod system is more fully described in U.S. Pat. No. 3,654,607 to Andre Wavre et al entitled "Signal Sequencing System," issued Apr. 4, 1972 and assigned to the assignee of the present invention. The shut down rods are operable to be either driven "full out" when the reactor is at full power or "full in" when the power is shut down. The control rods, on the other hand, are moved either up or down incrementally in banks, with all the rods within a given bank being moved to the same level simultaneously; the level depending upon the power demand of the plant. The part length rods act as verniers and are never entirely out of or in the reactive region, but are driven either up or down within a small range of steps. The full length control rods are moved up and down within pressurized housings by magnetic jack drive mechanism more fully described in U.S. Pat. No. 3,158,766, issued to E. Frisch and assigned to the assignee of the present invention. It takes approximately 232 pulsed steps to cover the total distance of control rod travel, which amounts to approximately a total distance of 144 inches. Other mechanisms generally exist for driving the part length rods to obtain their vernier control.

The pressure vessel containing the control rods makes it practically impossible for an operator to directly determine the actual position of the rods. A control rod drive shaft position sensor, normally located along the control rod housing is commonly provided for this purpose to sense the position of the control rod drive shafts which are affixedly coupled to the control rods. The position information thus obtained is then translated to actual control rod position. An example of such a monitoring device can be found in the application to J. A. Neuner, F. T. Thompson and L. Vercellotti entitled "Digital Multiplex Position Indication and Transmission System," Ser. No. 320,792, filed Jan. 3, 1973, (W.E. 44,067).

In order to assure the safe operation of the reactor plant it is desirable to compare the discrete signals employed to command control rod position with the signals received from the control rod monitoring equipment to assure that the command has been executed. Furthermore, it is desirable to know the last command issued by the reactor control equipment prior to a power failure in order to assure the safe and continued operation of the reactor.

For these purposes, the present invention provides a resilient, electronic, data recorder having the inherent circuitry characteristics of re-establishing the recorded data state previously exhibited just prior to a power failure upon the return of the source power supply. The entire recorder unit is designed to be operable in the extremely adverse environment of a reactor containment to provide reliable and durable output information which can be used for the comparisons required in nuclear applications. The digital data recorder thus contemplated is generally illustrated in FIG. **1** as basically comprising a pulse conditioning circuit **10**, an up-down retentive counter **12** and a power control circuit **14.**

The pulse conditioning circuit **10** will receive either an up or down control rod drive pulse from the relay contact closure **16** or **18** respectively, simulating discrete rod position movement demands. The signals are processed by the pulse conditioning circuit **10** to a form compatible with the up-down retentive counter **12.** Zero detect circuitry, forming a portion of the pulse conditioning unit **10,** monitors the counter's output, shown in binary coded form by reference character **20,** and is responsive to the zero counter state to inhibit further reverse counting which could otherwise result in returning the counter to maximum count.

The up-down retentive counter **12** is basically constructed from high threshold integrated logic circuits in a toggle flip-flop configuration. A block diagram of a one bit circuitry section of the counter is shown in FIG. **2.** The separate counter stages are synchronized by the up-down rod drive pulses emanating respectively from the relay outputs **16** and **18** shown as the input functions **21** in FIG. **2.** The up and down pulses **21** are supplied to a series of logic circuits which process the information conveyed to a form compatible with the digital counter output desired. The output from the logic unit is then applied to a trigger circuit **25** which drives a multiple configuration of toggle flip-flops. The toggle flip-flops basically comprise two stages of RS flip-flops. The first stage **27,** commonly known as the master, reacts to the falling edge of the input pulse, while the second stage **28** which forms the output circuit, commonly known as the slave, is responsive to the rising edge of the pulse to provide one bit of the digital output through an isolation buffer **30.** A retentive circuit which provides the desired memory characteristics of this invention is formed as an integral part of the master section of each toggle flip-flop and employs the principle of either setting or resetting, upon power turn off or turn on, the RS flip-flops to their prepower failure state. The set-reset decision is dependent upon the magnetic flux density existing within an inductive core located within a feedback loop of the master section of the flip-flop.

A simplified circuitry schematic of a one bit section of the counter circuitry is illustrated in FIG. **3** with the counter's three stages **22, 24** and **26** shown in more detail in FIGS. **4** and **5.** FIG. **6** provides a simplified schematic of the actual retentive circuit of the master section of one portion of the counter with the corresponding hysteresis loop of the inductor being illustrated in FIG. **7.** The figures in combination with the following description will provide a complete understanding of the operation of the circuits illustrated.

RETENTIVE DIGITAL COUNTER

The circuitry associated with a one bit section of the counter is illustrated in FIG. **3** and forms the basic building block of the counter, which comprises a plural arrangement of toggle flip-flops. As is known in the art, a toggle flip-flop is constructed from an arrangement of two RS flip-flops; the first forming the master and the second forming the slave stage. The master stage is generally indicated in FIG. **3,** by the NAND gates **42** and **44** and the slave stage is indicated by reference characters **34** and **38.** The memory characteristics of the circuit are essentially supplied by the inductive core L and its corresponding time constant associated with the feedback loop of the master stage. In addition, a time constant is associated with the reference supply voltage

input Vt provided at one input to NAND gate **44** and is dependent upon the value of the capacitor C, the resistor Rc and the internal pull up resistor associated with the gate. NAND gates **32** and **36** form the triggering portion of the circuit previously identified in FIG. **2** by reference character **25** and function to assure that the master stage is responsive to the falling edge and the slave stage is responsive to the rising edge of the input pulse. NAND gate **40** appearing at the output serves to provide output isolation and acts as the buffer **30** previously noted in FIG. **2**, to prevent current drain on the circuit.

FIG. **4** illustrates a four bit counter output stage and is employed to form the first and second stages **22** and **24** of the counter **12.** It is readily apparent that the circuit illustrated in FIG. **3** supplies the basic building block for the individual counter output bit circuits **46, 48, 50** and **52,** with the digital output bits **20** being identified by A, B, C and D, respectively. NAND gates **54** form the logic circuitry previously identified by reference characters **23** in FIG. **2,** and function to condition the inputs so that circuitry of the counter can provide the digital outputs in the desired form. The diodes **56** OR the NAND gate outputs to the appropriate counter bit circuit inputs, while the NAND gates identified by reference character **58** monitor the output bits of the counter to identify the zero count state. The latter information is then conveyed to the pulse conditioning circuit **10** at output terminal **60** for combination with the other counter monitoring outputs provided by the other two counter stages.

FIG. **5** illustrates the last stage of the counter previously identified by reference character **26** in FIG. **2,** which provides a two bit output. Circuits circuits **62** and **64** function in the same manner as the circuits previously described by reference characters **46, 48, 50** with **52,** and the appropriate counter output bits taken at terminals **66** and **68.**

The operation of the retentive memory cell which forms a portion of the feedback loop of the master section of the toggle flip-flop can best be understood by reference to the simplified schematic provided in FIG. **6** and the corresponding graphical illustration shown in FIG. **7.** The basic principle of operation is dependent upon a comparison to two time delays T_1 and T_2 corresponding to the time constants τ_1 and τ_2 associated with the toggle flip-flops. τ_1 is a fixed time constant dependent upon the characteristic of the capacitor C, the resistor R_c, and the internal pull up resistance associated with the reset input to NAND gate **42** in FIG. **6.** τ_2 is a time constant which varies depending upon the last output state Q of the flip-flop. As will be appreciated by those skilled in the art τ_2 is governed by the state of the magnetic core generally associated with the inductor L.

The saturable magnetic core L is desirably constructed from a magnetic material having magnetic characteristics which provide a substantially rectangular hysteresis loop, such as the one illustrated in FIG. **7.** Therefore, the output Q will assume either of two stable states, high or low. The following two examples which illustrate the two output states Q can assume, will completely describe the operation of the memory core in the event of a power failure.

Assume Q is high just prior to a power failure, rendering the output of gate **42** high and the output of gate **44** low. The current through the core will then have been flowing out of the dotted side of the magnetic core. Hence, the flux density within the magnetic core will correspond to the ordinate $-B_m$ indicated in FIG. **7.** When the power fails, this flux density will rise to $-B_r$, which is approximately $-0.9\ B_m$. When power is re-established, gate **44** will transition high due to the characteristics of the capacitor C, which initially acts as a short circuit. The output of gate **42** will also assume its high state inasmuch as the inductor L initially appears as an open circuit. Current will therefore begin to flow into the dotted side of the inductor L due to the higher potential appearing at the output of gate **44.** The inductance of the core will then tend to resist this current flow since the flux density is initially at $-B_r$. Thus, with the values of R_c and C appropriately chosen, τ_1 will be much less than τ_2 and the voltage across C will increase much faster than the voltage across R_L. Therefore, the output of gate **44** returns to its low state before forcing Q to its low state, thus latching Q in its high state.

On the other hand, assuming Q was low just prior to power failure, the outputs of gates **42** and **44** will be low and high respectively. Thus, current will flow into the dotted side of the magnetic core and its flux density will assume the value indicated by the ordinate $+B_m$. After a power failure, the flux density of the core will drop to $+B_r$ which is approximately $0.9\ B_m$. When the power is restored, the output of gates **42** and **44** will both intially transition to a high state as a result of the capacitance and inductance respectively exhibited by C and L. However, this time the inductance of the core will provide little resistance to the current flowing into the dotted portion of the coil L inasmuch as the flux density will retain a value approximately equal to the ordinate $+B_r$. Therefore, τ_2 will be much less than τ_1, and Q will return to its low state before the output of gate **44** goes to its low state, thus latching the outputs of gates **42** and **44** in their prepower failure state.

Accordingly, the retentative characteristics provided by the magnetic core L, within the feedback loop of the master section of the toggle flip-flop, retains the output established for each bit of the counter just prior to a source power failure and re-establishes this prior output state upon the resumption of the source power supply.

PULSE CONDITIONING CIRCUIT

The pulse conditioning circuit previously identified by reference character **10** in FIG. **1** is shown in schematic circuitry form in FIG. **8.** The up and down pulses, simulating the rod position demand data, are respectively received at terminals **70** and **72.** The resistor capacitive filter provided by resistors **80** and capacitors **78** establish a sufficient time delay to avoid multiple counts which might otherwise occur due to contact bounce of the relays **16** and **18.** When a sufficient time has elapsed for the capacitor **78,** associated with the relay energized, to charge to a voltage value sufficent to raise the corresponding circuit node **82** to a higher value than node **84,** then unijunction transistor **74** will conduct, sharply dropping the voltage level appearing at node **84** to a negligible value. This negligible voltage level will continue to appear until the respective input relay contact energized is opened, at which time unijunction transistor **74** will effectively open circuit, sharply raising the voltage level appearing at terminal **84** to its former value. Thus the output pulse appearing

at terminal **84** will be characterized by sharp falling and rising edges and will be further modified by NAND gates **86** and **88** for distribution to the counter circuitry at terminal **90** and **92** through the interface logic gates **54.**

The zero inhibit, as previously described, is responsive to the zero counter state to prevent further down rod command pulses from entering the counter. NAND gates **58** illustrated in FIG. **4** were described as the mechanism for monitoring the individual toggle flip-flop circuits to identify when the zero state had been assumed by the circuits respective outputs. When the zero output state is identified the respective outputs **60** from the first two stages are then applied to the input terminal **60** of the pulse conditioning circuit illustrated in FIG. **8.** In a similar manner, NAND gates **94** are used to monitor the last stage of the counter **12** to provide a corresponding output indicative of the zero state. The respective monitoring outputs from the three stages of the counter are then applied to the input of NAND gate **96** which inhibits NAND gate **88** upon the occurrence of the zero state, effectively disconnecting the output from further down stepping the counter.

Thus, the pulse conditioning circuit modifies the input data pulses to a form compatible with the counter and effects the zero inhibit to prevent counter stepping, in reverse count, past the zero data output state.

POWER CONTROL CIRCUIT

The power control circuit illustrated in FIG. **1** is schematically shown in FIG. **9** with a graphical illustration of the corresponding inputs and outputs provided in FIG. **10.** The circuit is designed to force the supply voltage furnished to the retentive counter to be switched on and off much faster than the shortest time constant of the counter in order to assure the retentiveness of the information maintained therein. The input time constant of the circuit, dependent upon the component values of resistor **102** and capacitors **98** and **100,** controls the rise time of the input power supply voltage applied between terminals **118** and ground. When the input supply voltage rises above the threshold voltage level governed by the diode drops appearing across transistors **104** and **108** and Zener **106,** transistors **104** and **108** conduct, essentially grounding the collector of transistor **108,** which, in turn, saturates transistor **110** and abruptly reverse biases transistor **112.** As transistor **110** abruptly transitions to its ON state, current is fed back to the base of transistor **104** forcing a sharp rising edge on the voltage displayed at output terminal **114.** This output voltage is then applied to the supply voltage inputs of the recorder circuitry. FIG. **10A** graphically illustrates the power on inputs and outputs of the power control circuit with a threshold voltage indicated by V_{th}. The Zener and transistors are chosen to supply a threshold voltage sufficient to support the working operation of each of the elements of the data recorder so that when the power supply reaches the threshold voltage level, upon turn on, an almost instantaneous operating voltage appears at the supply inputs to the data recorder circuitry.

In a similar fashion, when the input supply voltage drops to a level sufficient to reverse bias transistor **104,** the transistor transitions to its OFF state, turning off transistor **108.** The collector of transistor **108** will then effectively rise to a value sufficient to turn off transistor **110** and turn on transistor **112.** This essentially grounds the output appearing at terminal **114.** A current limiting resistor **116** is supplied in series with the collector of transistor **112** to prevent short circuiting transistors **110** and **112** for a short period when they are both conducting. When transistor **112** is turned on, current is removed from the base of transistor **104** which further reverse biases transistor **104** and provides a sharp falling edge as indicated by the graphs supplied in FIG. **10B.** Thus, a sharp falling edged pulse is provided at output terminal **114,** almost instantaneously turning off power to the individual element units of the data recorder. The transition point of the output **114** indicated by V_{th} in FIG. **10B** is slightly different from the threshold level indicated in the graph shown in FIG. **10A** due to the inherent hysteresis of the circuit. However, both threshold levels are chosen well within the working voltages of the individual element units of the recorder and a slight discrepancy in threshold level will not affect the operation of the circuit.

It is desirable to have the power control circuit supply the input supply voltage to each of the subunits of the recorder in order to assure minimum turn on and turn off times so as to prevent alteration of the data output state retained by the counter. The power control circuit is provided for this purpose.

Accordingly, the individual element units described are amenable to solid state construction and are arranged in the configuration illustrated in FIG. **1** to exhibit the desired characteristics, in extremely adverse environments such as are found in nuclear reactor applications, to provide a reliable and durable output function.

We claim as our invention:

1. A digital data recorder having an electronic counter responsive to a data input to provide a representative digital output exhibited by a plurality of bistable output bits, the counter including a plurality of toggle flip-flop output circuits corresponding to the plurality of output bits, each of said toggle flip-flops including a master and a slave stage with the corresponding output bit being provided by the slave stage, the master stage including a variable reactance within a feedback loop in the master stage, the value of the variable reactance being dependent upon the stable state of the output bit to control and vary a time constant of the feedback loop in a manner to re-establish the output bit last exhibited by the slave stage prior to a failure of supply voltage power to the counter after the supply power has been resumed.

2. The digital data recorder of claim **1** wherein the master stage of said toggle flip-flop has an input from the supply voltage powering the counter and exhibits a separate fixed, predetermined, time constant independent of said variable reactance which controls the rise time of the supply voltage input and is substantially greater than the value of the time constant of the feedback loop controlled by the value of the variable reactance corresponding to one of the bistable states of the output bit of the slave stage and is substantially less than the value of the time constant of the feedback loop controlled by the value of the variable reactance corresponding to the other of the bistable states of the output bit of the slave stage.

3. The digital data recorder of claim **1** wherein said variable reactance comprises an inductor wound on a saturable magnetic core exhibiting rectangular hysteresis with the saturable state of the core dependent upon

the stable state of the output bit provided by the slave stage.

4. The digital data recorder of claim **1** wherein the data is supplied to the counter by the closure of an electrical relay contact including means for delaying the data input to the counter for a predetermined time delay to avoid a false multiple count by said counter attributable to contact bounce of the relay providing the data input.

5. The digital data recorder of claim **1** wherein said counter advances count in response to the data input in either a forward or reverse counting direction corresponding to the data input receiver, including means for inhibiting said counter from advancing count in reverse count past the counter bit output state representative of a zero data count.

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