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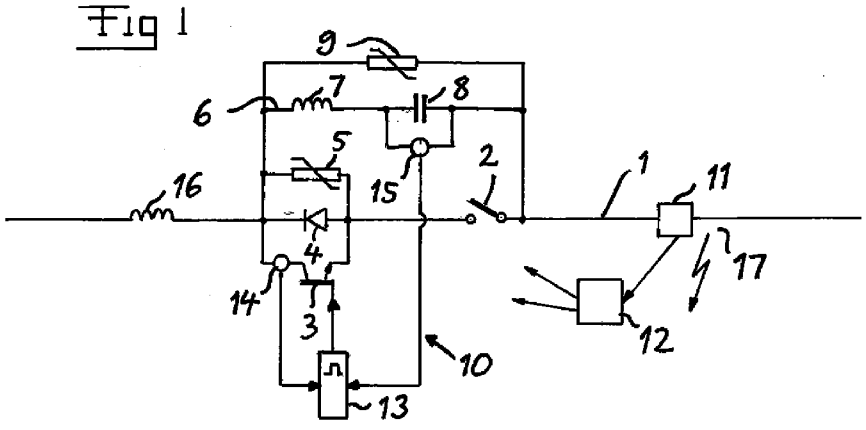
(54) **Title**: A HIGH VOLTAGE DC BREAKER APPARATUS




(57) **Abstract**: A high voltage DC breaker apparatus configured to interrupt a fault current occurring in a high voltage DC conductor (1) comprises a mechanical interrupter (2), a semiconductor device (3) connected in series with the interrupter, an arrester (5) connected in parallel with the semiconductor device and an LC-circuit (6) connected in parallel with the series connection of the semiconductor device and the interrupter. A control unit (12) is configured, upon detection of a fault current, to control switching of the semiconductor device (3) at a frequency adapted to the values of an inductance (7) and a capacitance (8) of the LC-circuit for charging the capacitance by the fault current while making the current through the interrupter (2) oscillating with an increasing amplitude and the interrupter to open for having the mechanical contacts thereof separated when current zero-crossing is reached for obtaining interruption of the fault current through the interrupter.

# *A high voltage DC breaker apparatus*

## FIELD OF THE INVENTION AND BACKGROUND ART

The present invention relates to a high voltage DC breaker apparatus configured to interrupt a fault current occurring in a high voltage DC conductor, said apparatus comprising

- at least one mechanical interrupter configured to be connected in series with said DC conductor,
- an arrangement configured to obtain zero-crossing of a fault current through said interrupter upon occurrence of a fault in said conductor,
- means configured to detect occurrence of a fault current in said DC conductor, and
- a unit configured to control said arrangement and mechanical interrupter upon occurrence of a said fault for obtaining interruption of a said fault current through the interrupter upon zero-crossing of the fault current.

High voltage means a voltage ≥ 10 kV and often a voltage of several hundreds kV with respect to ground.

Such a high voltage DC breaker apparatus may be arranged in a high DC voltage carrying system, for example in Voltage Source Converter based multi-terminal HVDC (High Voltage Direct Current) networks where fast-rising DC fault currents must be interrupted quickly at high voltages. Such faults may be line-to-line faults or line-to-ground faults, i.e. short-circuits of the DC conductor to earth.

In one type of known such breaker apparatuses said arrangement configured to obtain zero-crossing of a fault current through the interrupter comprises a passive LC-circuit generating an oscillation of fault current through the interrupter with the aim to obtaining a zero-crossing of the fault current. A disadvantage of using such an arrangement is the uncertainty as to when zero-crossing of the current will actually occur, which results in a risk of failing the arc extinguishing window when interruption of the current is possible, so that interruption of the fault current may not be reliably ensured.

Another type of known high voltage DC breaker apparatuses uses a said arrangement having a pre-charged capacitor connected in parallel with the mechanical interrupter for obtaining zero-crossing of the fault current. However, this solution is comparatively costly, since a large capacitor as well as a separate high voltage charging device for charging the capacitor are needed.

## SUMMARY OF THE INVENTION

The object of the present invention is to provide a high voltage DC breaker apparatus of the type defined in the introduction being improved in at least some aspect with respect to such apparatuses already known.

This object is according to the invention obtained by providing such an apparatus, which is characterized in that said arrangement comprises

- at least one semiconductor device of turn-off type configured to be connected in series with said mechanical interrupter and to conduct in the direction towards the interrupter,
- an arrester connected in parallel with said semiconductor device for defining a maximum voltage across said device, and
- an LC-circuit in the form of a series connection of an inductance and a capacitance connected in parallel with the series

connection of said semiconductor device and the mechanical interrupter,

and that said control unit is configured, upon detection of a said fault current by said means, to control switching of said semiconductor device at a frequency adapted to the values of said inductance and capacitance for charging said capacitance by the fault current while making this current oscillate through the mechanical interrupter with an increasing amplitude and that said at least one mechanical interrupter is configured to open for having the mechanical contacts thereof separated when said current zero-crossing is reached for obtaining interruption of the fault current through the mechanical interrupter.

By using the fault current to charge the capacitance no high voltage charging device is needed, but a well defined zero-crossing of the fault current will still be obtained by an appropriate control of said switching of the semiconductor device. Furthermore, only a small capacitance will be needed for obtaining said zero-crossing of the fault current. Thanks to the fact that said semiconductor device only needs to be rated for a voltage in the order of the protective voltage level of said arrester, which may be only a small fraction of the system voltage, i.e. the voltage of a said high voltage DC conductor with respect to ground, investment costs will be low. The on-state losses in said semiconductor device will also be low under normal operation of the high voltage DC system in question.

Another advantage of an apparatus according to the invention is that a gradually growing current oscillation through the interrupter prevents current zero over-shoot and results in a feasible switching duty for the mechanical interrupter, i.e. a low enough current and voltage time derivative. The protective voltage level of said arrester and the values of said inductance and capacitance of the LC-circuit may be selected for obtaining secure interruption by the mechanical interrupter within an acceptable pe-

riod of time after occurrence of a said fault. Accordingly, the need to generate current zero-crossings for obtaining interruption of the fault current is dealt with by the semiconductor device, whereas interrupting of the fault current is taken care of by the mechanical interrupter, which combines the benefits of the semiconductor device of fast switching and well-defined blocking voltage with the advantages of a mechanical interrupter relating to high dielectric withstand capability and low losses.

According to an embodiment of the invention the control unit is configured to carry out said switching of the semiconductor device at a frequency being 90%-110% of the eigenfrequency of said LC-circuit. The switching frequency close to the eigenfrequency of the LC-circuit will result in a desired oscillation of the fault current through the interrupter and reaching of zero-crossing of the fault current when the current derivative is also zero, so that it will be favourable to then interrupt the current.

According to another embodiment of the invention the apparatus further comprises measuring means configured to measure at least one parameter relating to the operation of said arrangement upon occurrence of a said fault and send the result of this measurement to said control unit configured to adapt said switching of this measurement result. Such a feedback for the switching of the semiconductor device results in a possibility to control how and when zero-crossing of the fault current will appear for obtaining reliable interruption of the fault current. Suitable parameters to measure may be the current through said semiconductor device and/or the voltage across said capacitance, which constitutes further embodiments of the invention.

According to another embodiment of the invention said control unit is configured to delay initiation of separation of the mechanical contacts of the interrupter by a determined period of time with respect to the start of the switching of said semicon-

ductor device for possibly refraining from opening the interrupter should said control unit receive information about a disappearance of said fault within this period of time. It has turned out that it is well possible to obtain interruption even if such a delay is used, which may then result in avoidance of unnecessary interruption in the case of a quick disappearance of the fault condition.

According to another embodiment of the invention the apparatus comprises a further arrester connected in parallel with said LC-circuit. This further arrester will limit the rising recovery voltage across the mechanical interrupter after interruption of the fault current.

According to another embodiment of the invention the protective voltage level of said arrester connected in parallel with the LC-circuit is at least 120% or 130%-200% of the DC voltage intended for a said DC conductor with respect to ground. A protective voltage level of about 150% of the system voltage is normally suitable for an arrester in parallel with such a mechanical interrupter.

According to another embodiment of the invention the apparatus comprises a current derivative limiting reactor configured to be connected in series with said parallel connection of the LC-circuit and the series connection of the semiconductor device and the mechanical interrupter in said DC conductor upstream this parallel connection as seen in the conducting direction of said semiconductor device. Such a reactor will limit the rise of the fault current to the moment of starting to separate the mechanical contacts of the interrupter facilitating proper obtaining of zero-crossing of the fault current.

According to another embodiment of the invention said control unit is configured to carry out said switching of the semiconductor device with a frequency of 100 Hz – 10 kHz or 500 Hz – 5

kHz. Such switching frequencies are suitable for the operation of a switching device in an apparatus of this type, in which the inductance may typically have a value of 0.1 mH – 10 mH and the capacitance a value of 10 nF – 100 µF or 0.5 µF – 5 µF.

IGBT:s (Insulated Gate Bipolar Transistors), GTO:s (Gate Turn-Off thyristors) and IGCT:s (Insulated Gate Commutated Thyristors) are examples of semiconductor devices suitable to be used in an arrangement of an apparatus according to the present invention.

According to another embodiment of the invention the apparatus is configured to interrupt a fault current occurring in a high voltage DC conductor intended to be on a voltage level of ≥ 10 kV, 10 kV – 1000 kV, 100 kV – 1000 kV or 300 kV – 1000 kV with respect to ground.

According to another embodiment of the invention the protective level of said arrester connected in parallel with said semiconductor device is less than 50% or less than 10% of the voltage level intended for said high voltage DC conductor with respect to ground. It may be mentioned that said protective voltage level may for instance be about 10 kV at the same time as the voltage level intended for said high voltage DC conductor with respect to ground may be 400 kV.

According to another embodiment of the invention the apparatus is configured to be connected to a said high voltage DC conductor in an AC/DC converter station, and according to another embodiment the apparatus is configured to be arranged in a DC grid for protecting equipment connected thereto.

US 5 517 378 discloses a high voltage DC breaker related to the apparatus according to the present invention.

The invention also relates to a plant for transmitting electric power through High Voltage Direct Current, which is characterized in that it is provided with a DC breaker apparatus according to the invention. Such a plant may benefit from the positive features mentioned above of such an apparatus.

The invention also relates to a method for controlling a high voltage DC breaker apparatus according to the invention so as to interrupt a fault current detected in said high voltage DC conductor according to the appended independent method claim as well as a computer program product and a computer readable medium associated with such a method.

Further advantages as well as advantageous features of the invention will appear from the following description.

## BRIEF DESCRIPTION OF THE DRAWING

With reference to the appended drawing, below follows a specific description of an embodiment of the invention cited as examples.

In the drawing:

Fig 1 is a very schematic view of a high voltage DC breaker apparatus according to an embodiment of the invention,

Fig 2 is a graph of the fault current I through the mechanical interrupter of the apparatus according to Fig 1 versus time t upon occurrence of a fault in the high voltage DC conductor shown in Fig 1, and

Fig 3 is a graph of the voltage U across the semiconductor device of the apparatus shown in Fig 1 versus time t upon occurrence of a said fault.

## DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

Fig 1 shows schematically a high voltage DC breaker apparatus according to an embodiment of the present invention. This apparatus is configured to interrupt a fault current occurring in a high voltage DC conductor 1 and comprises a mechanical interrupter 2 which may stand for one or several mechanical interrupters, e.g. an SF6- or vacuum-interrupter or a combination thereof, and connected in series therewith a semiconductor device 3 of turn-off type, here an IGBT, configured to conduct in the direction towards the interrupter. A rectifying diode 4 is connected in anti-parallel with the semiconductor device 3. An arrester 5 is connected in parallel with the semiconductor device for defining a maximum voltage across this semiconductor device by having a suitable protective voltage level, such as 10 kV. The blocking voltage capability of the semiconductor device 3 shall be higher than this protective voltage level. Accordingly, the arrester 5 ensures that the voltage across the semiconductor device will never reach the level of the voltage blocking capability of the semiconductor device when this is turned off.

Furthermore, an LC-circuit 6 in the form of a series connection of an inductance 7 and a capacitance 8 is connected in parallel with the series connection of the semiconductor device 3 and the mechanical interrupter 2. A further arrester 9 is connected in parallel with the LC-circuit 6, and this arrester has a protective voltage level exceeding the level of the DC voltage intended for said DC-conductor 1 with respect to ground and is for example 150% of that voltage level.

The apparatus also comprises an arrangement 10 configured to obtain zero-crossing of a fault current through the interrupter 2 upon occurrence of a fault in the DC conductor 1, and this arrangement will partly be formed by components of the apparatus

already described. Means 11 schematically indicated is arranged and configured to detect occurrence of a fault current in said DC conductor 1. The apparatus comprises a unit 12 configured to control said arrangement 10 and mechanical interrupter 2 upon occurrence of a said fault for obtaining interruption of a fault current through the interrupter upon zero-crossing of the fault current. The control unit 12 is in such a case configured to control switching of the semiconductor device 3, which is indicated by a pulse generator 13 to which the control unit sends control signals, and this switching is then carried out at a frequency adapted to the values of the inductance 7 and capacitance 8 for charging said capacitance by the fault current as will be described more in detail further below. It is illustrated how the apparatus may also have measuring means in the form of measuring means 14 measuring the current through the semiconductor device 3 and measuring means 15 measuring the voltage across the capacitance 8 for sending these measurement results to the control unit (pulse generator), which may then consider these results when controlling the switching of the semiconductor device 3. The apparatus also has a current derivative limiting reactor 16 connected in series with the parallel connection of the LC-circuit 6 and the series connection of the semiconductor device 3 and the mechanical interrupter 2 in said DC conductor upstream this parallel connection as seen in the conducting direction of the semiconductor device. A current limiting device in the form of at least one module of a parallel connection of a semiconductor device of turn-off type, such as an IGBT, and an arrester may be connected in series with the reactor 16 and assist this in limiting a fault current or even replace the reactor.

Possible values of components of the apparatus may be as follows: the reactor 16 has an inductance of 100 mH and the inductance 7 an inductance of 0.6 mH. The capacitance 8 is 1 μF. The DC conductor 1 is on a voltage of 320 kV with respect to ground and the protective level of the arrester 5 is 10 kV.

The operation of the apparatus in the case of occurrence of a fault will now be explained while making reference also to Figs 2 and 3. It is pointed out that the apparatus as shown in Fig 1 is configured to interrupt a fault current upon occurrence of a fault 17 on the right side of the interrupter, but it is of course within the scope of the invention to modify the apparatus so as to instead be able to take care of a fault occurring on the left side of the interrupter and also so as to be able to take care of faults occurring on both sides of the apparatus, which for example may be obtained by connecting a further parallel connection of an arrester and a semiconductor device of turn-off type in series with the parallel connection shown in Fig 1 and with that semiconductor device having opposite conducting direction. Another option would be to have a breaker configuration in an adjacent switch gear preventing current in more than one direction.

During normal operation a current, such as in the order of 2000 A, will flow in the DC conductor 1 through the semiconductor device 3 and the mechanical interrupter 2 then closed. The energy transfer loss will be comparatively low in the semiconductor device 3, since this has only to be rated for a value somewhat higher than the protective voltage level of the arrester 5, which means that the at least one semiconductor device does not have to be a high number of semiconductor devices connected in series.

When a fault 17 occurs on the DC line, which may be a line-to-line fault or a line-to-ground fault, this is detected by the means 11 and information thereabout is sent to the control unit 12. This occurs at the time $t_1$ shown in Figs 2 and 3. After the fault has occurred the fault current through the interrupter rises at a rate given by the ratio between the system voltage of the DC conductor and the fault current derivative limiting reactor 16, which takes place to the time $t_2$, which may occur 2 ms after $t_1$. After this protection time $t_p$ the mechanical interrupter 2 is controlled

by the control unit 12 to be tripped, which means that the mechanical contacts thereof starts to separate, so that an arc is formed therebetween. At the same time the control unit starts to switch the semiconductor device 3 at a frequency close to the eigenfrequency of the LC-circuit 6, so that the capacitance 8 will be charged by the fault current through the interrupter 2. This fault current will by said switching oscillate with an increasing amplitude as shown in Fig 2, and the voltage across the capacitance 8 will increase by each firing pulse sent to the semiconductor device 3 until current zero 0 is reached by the fault current through the interrupter 2. This is done when the current changes direction, so that the current derivative is zero, which then facilitates proper interruption of the current through the interrupter, which will then withstand the rising recovery voltage then further limited by the further arrester 9 in parallel with the LC-circuit 6.

The presence of the measuring means 14 and 15 for providing feedback, which presence, however, is not necessary, makes it possible to adapt the switching of the semiconductor device 3 to reach zero-crossing of the fault current through the interrupter in the most favourable way (at a zero current derivative) and at exactly the instant desired. This happens in the embodiment shown in Figs 2 and 3 about 5.6 ms after tripping of the interrupter.

Although it is shown in Figs 2 and 3 how the switching of the semiconductor device 3 is started at the same time as the interrupter is tripped the tripping of the interrupter may be delayed by a determined period of time with respect to the start of the switching of the semiconductor device for possibly refraining from opening the interrupter should said control unit receive information about a disappearance of the fault within this period of time.

Parameters influencing the interrupter procedure are: the protective voltage level of the arrester 5, a higher such level means that the capacitance will be charged more rapidly. Higher values of the inductance and the capacitance will result in a lower eigenfrequency of the LC-circuit and a lower suitable frequency of the switching of the semiconductor device. The values of L and C should be chosen for obtaining an interruption situation to be managed by the mechanical interrupter, such as with respect to recovery voltage across the interrupter. It also has to be considered which frequency the semiconductor device may operate at, and the semiconductor device also has to be able to break the current therethrough when being turned off in said switching.

The invention is of course not in any way restricted to the embodiments described above, but many possibilities to modifications thereof will be apparent to a person with ordinary skill in the art without departing from the scope of the invention as defined in the appended claims.

It would be possible to cascade several interrupters so as to obtain higher voltages, i.e. to connect a plurality of modules comprising the elements 2-9 and 13-15 shown in Fig 1 in series.

CLAIMS

1. A high voltage DC breaker apparatus configured to interrupt a fault current occurring in a high voltage DC conductor (1), said apparatus comprising

- at least one mechanical interrupter (2) configured to be connected in series with said DC conductor,
- an arrangement (10) configured to obtain zero-crossing of a fault current through said interrupter upon occurrence of a fault in said conductor,
- means (11) configured to detect occurrence of a fault current in said DC conductor, and
- a unit (12) configured to control said arrangement and mechanical interrupter upon occurrence of a said fault for obtaining interruption of a said fault current through the interrupter upon zero-crossing of the fault current,

**characterized** in that said arrangement comprises

- at least one semiconductor device (3) of turn-off type configured to be connected in series with said mechanical interrupter (2) and to conduct in the direction towards the interrupter,
- an arrester (5) connected in parallel with said semiconductor device for defining a maximum voltage across said device, and
- an LC-circuit (6) in the form of a series connection of an inductance (7) and a capacitance (8) connected in parallel with the series connection of said semiconductor device (3) and the mechanical interrupter (2),

and that said control unit (12) is configured, upon detection of a said fault current by said means, to control switching of said semiconductor device (3) at a frequency adapted to the values of said inductance (7) and capacitance (8) for charging said capacitance by the fault current while making this current oscillatethrough the mechanical interrupter (2) with an increasing amplitude and that said at least one mechanical inter-

rupter is configured to open for having the mechanical contacts thereof separated when said current zero-crossing is reached for obtaining interruption of the fault current through the mechanical interrupter.

2. An apparatus according to claim 1, **characterized** in that the control unit (12) is configured to carry out said switching of the semiconductor device (3) at a frequency being 90%-110% of the eigenfrequency of said LC-circuit (6).

3. An apparatus according to claim 1 or 2, **characterized** in that it further comprises measuring means (14, 15) configured to measure at least one parameter relating to the operation of said arrangement (10) upon occurrence of a said fault and send the result of this measurement to said control unit (12) configured to adapt said switching to this measurement result.

4. An apparatus according to claim 3, **characterized** in that said measuring means (14) is configured to measure the current through said semiconductor device (3).

5. An apparatus according to claim 3 or 4, **characterized** in that said measuring means (15) is configured to measure the voltage across said capacitance (8).

6. An apparatus according to any of the preceding claims, **characterized** in that said control unit (12) is configured to delay initiation of separation of the mechanical contacts of the interrupter (2) by a determined period of time with respect to the start of the switching of said semiconductor device (3) for possibly refraining from opening the interrupter should said control unit receive information about a disappearance of said fault within this period of time.

7. An apparatus according to any of the preceding claims, **characterized** in that it comprises a further arrester (9) connected in parallel with said LC-circuit (6).

8. An apparatus according to claim 7, **characterized** in that the protective voltage level of said further arrester (9) connected in parallel with the LC-circuit (6) is at least 120% or 130%-200% of the DC voltage intended for a said DC conductor (1) with respect to ground.

9. An apparatus according to any of the preceding claims, **characterized** in that it comprises a current derivative limiting reactor (16) configured to be connected in series with said parallel connection of the LC-circuit (6) and the series connection of the semiconductor device (3) and the mechanical interrupter (2) in said DC conductor upstream this parallel connection as seen in the conducting direction of said semiconductor device (3).

10. An apparatus according to any of the preceding claims, **characterized** in that said control unit (12) is configured to carry out said switching of the semiconductor device with a frequency of 100 Hz – 10 kHz or 500 Hz – 5 kHz.

11. An apparatus according to any of the preceding claims, **characterized** in that said inductance (7) has a value of 0.1 mH – 10 mH.

12. An apparatus according to any of the preceding claims, **characterized** in that said capacitance (8) has a value of 10 nF – 100 µF or 0.5 µF – 5 µF.

13. An apparatus according to any of the preceding claims, **characterized** in that said semiconductor device (3) is an IGBT, a GTO or an IGCT.

14. An apparatus according to any of the preceding claims, **characterized** in that it is configured to interrupt a fault current occurring in a high voltage DC conductor (1) intended to be on a voltage level of ≥ 10 kV, 10 kV – 1000 kV, 100 kV – 1000 kV or 300 kV – 1000 kV with respect to ground.

15. An apparatus according to any of the preceding claims, **characterized** in that the protective level of said arrester (5) connected in parallel with said semiconductor device (3) is less than 50% or less than 10% of the voltage level intended for said high voltage DC conductor (1) with respect to ground.

16. An apparatus according to any of the preceding claims, **characterized** in that it is configured to be connected to a said high voltage DC conductor (1) in an AC/DC converter station.

17. An apparatus according to any of the preceding claims, **characterized** in that it is configured to be arranged in a DC grid for protecting equipment connected thereto.

18. A plant for transmitting electric power through High Voltage Direct Current, **characterized** in that it is provided with a DC breaker apparatus according to any of the preceding claims.

19. A method for controlling a high voltage DC breaker apparatus according to any of claims 1-17 so as to interrupt a fault current detected in said high voltage DC conductor, **characterized** in that it comprises the steps:

a) switching said semiconductor device (3) is switched at a frequency adapted to the values of said inductance (7) and capacitance (8) for charging said capacitance by the fault current while making this current through the mechanical interrupter (2) oscillating with an increasing amplitude, and

b) switching the mechanical interrupter (2) is controlled to open for having the mechanical contacts thereof separated when said

current zero-crossing is reached for obtaining interruption of a fault current through the mechanical interrupter.

20. A computer program product storable on a computer usable medium containing instructions for a processor to evaluate the method according to claim 19.

21. Computer program product according to claim 20 provided at least partially through a network, such as the Internet.

22. Computer readable medium, **characterized** in that it contains a computer program product according to claim 20.

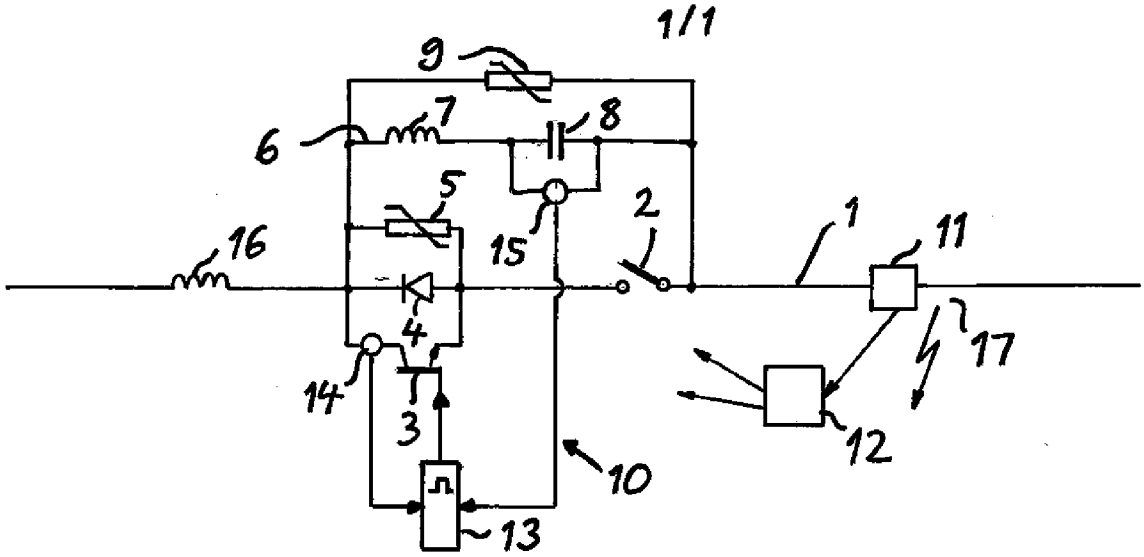



Fig 1

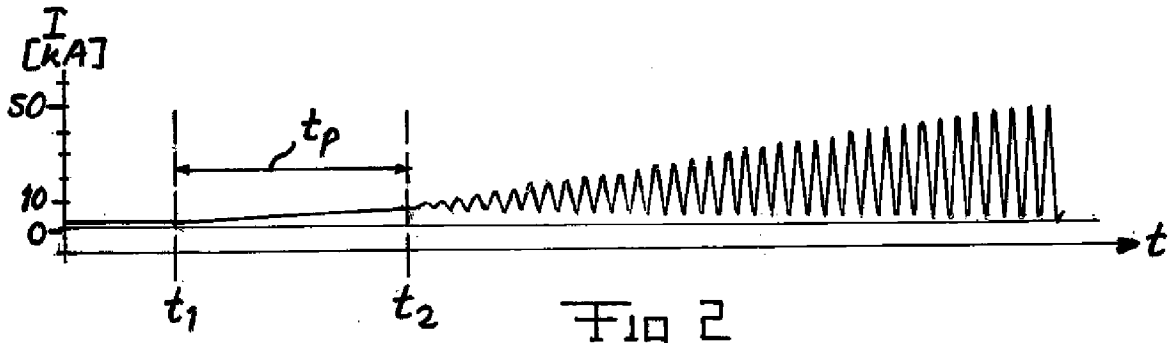



Fig 2

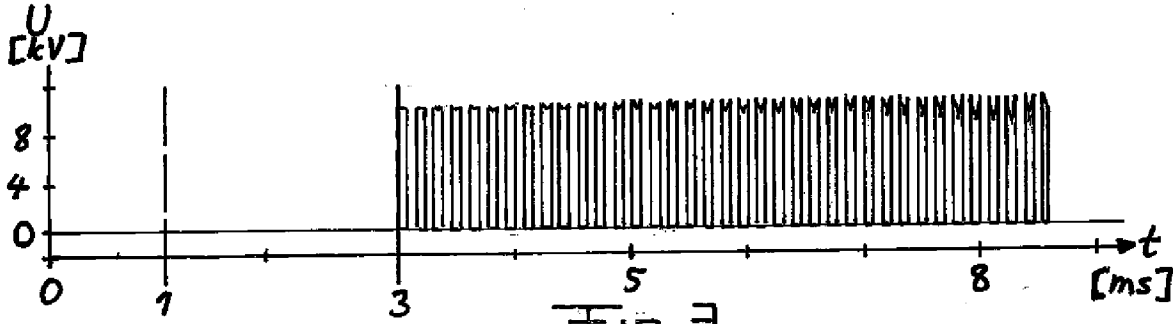



Fig 3

# INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/056474

**A. CLASSIFICATION OF SUBJECT MATTER**
INV. H01H33/59
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H01H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5 517 378 A (ASPLUND GUNNAR [SE] ET AL) 14 May 1996 (1996-05-14) cited in the application | 19-22 |
| A | column 6, line 62 - column 8, line 33; figures 3a-3d | 1 |
| A | DE 43 04 863 A1 (HITACHI LTD [JP]) 26 August 1993 (1993-08-26) the whole document | 1 |
| A | WO 2009/149749 A1 (ABB TECHNOLOGY AG [CH]; AASTROEM URBAN [SE]; LILJESTRAND LARS [SE]; LE) 17 December 2009 (2009-12-17) the whole document | 1 |
| A | EP 0 740 320 A2 (MITSUBISHI ELECTRIC CORP [JP]; KANSAI ELECTRIC POWER CO [JP]; SHIKOKU) 30 October 1996 (1996-10-30) the whole document | 1 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 19 November 2010 | 29/11/2010 |

| Name and mailing address of the ISA/ | Authorized officer |
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