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(12) **United States Design Patent**
Soyano et al.

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(54) **SEMICONDUCTOR MODULE**

H05K 1/141; H05K 1/142; H05K 1/144;
H05K 1/18; H05K 1/181; H05K 1/182;
H05K 1/026

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See application file for complete search history.

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(73) Assignee: **FUJI ELECTRIC CO., LTD.**,
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(Continued)

(**) Term: **15 Years**

(21) Appl. No.: **29/705,163**

Primary Examiner — Elizabeth J Oswecki

(22) Filed: **Sep. 10, 2019**

(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

(30) **Foreign Application Priority Data**

Mar. 26, 2019 (JP) 2019-006409

(51) **LOC (12) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**

USPC D13/182; 257/678, 684, 690, 691;
361/679.01, 713, 728, 736, 760, 761, 772,
361/775, 783, 820; 174/250, 253;
438/15, 25, 26, 51, 55, 63, 64, 106
CPC . H01L 21/00; H01L 2224/42; H01L 2224/43;
H01L 2021/00; H01L 2021/02; H01L
2021/04; H01L 21/4814; H01L 21/4846;
H01L 21/4871; H01L 21/67144; H01L
23/02; H01L 23/13; H01L 23/14; H01L
23/147; H01L 2924/171; H01L
2924/1711; H01L 2924/1715; H01L
2924/17151; H01L 2924/181; H01L
2924/1811; H01L 2924/1815; H01L
2924/19042; H01L 2924/1905; H01L
2224/08054; H01L 23/58; H05B 41/14;
H02B 6/4201; G02B 6/4256; G02B
6/4257; G02B 6/4261; G02B 6/4262;
G02B 6/428; G02B 6/4281; H05K 1/14;

DESCRIPTION

FIG. 1 is a front view of a semiconductor module showing our new design;

FIG. 2 is a rear view of the semiconductor module of FIG. 1;

FIG. 3 is a left side view of the semiconductor module of FIG. 1;

FIG. 4 is a right side view of the semiconductor module of FIG. 1;

FIG. 5 is a top view of the semiconductor module of FIG. 1;

FIG. 6 is a bottom view of the semiconductor module of FIG. 1;

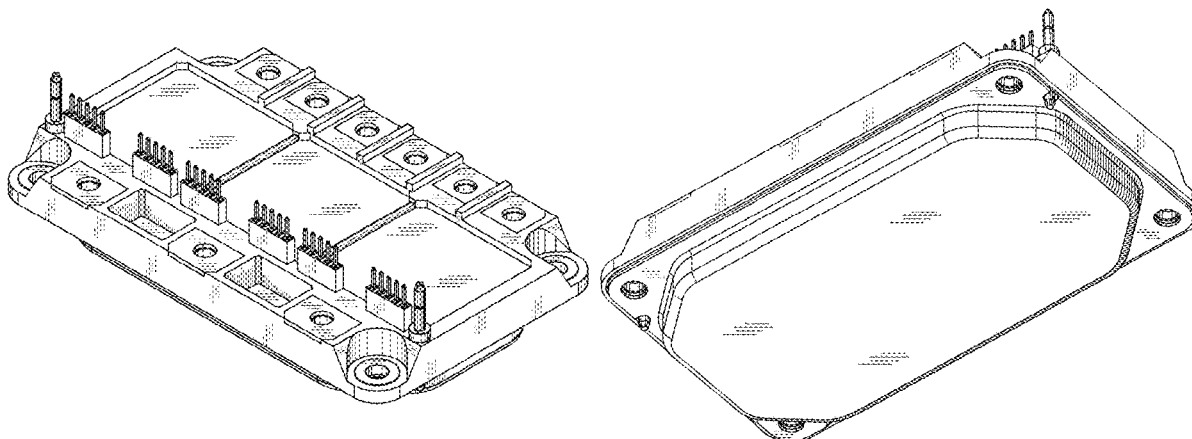
FIG. 7 is a front, top and left side perspective view of the semiconductor module of FIG. 1;

FIG. 8 is a front, bottom and right side perspective view of the semiconductor module of FIG. 1;

FIG. 9 is a rear, top and left side perspective view of the semiconductor module of FIG. 1; and,

FIG. 10 is a rear, bottom and right side perspective view of the semiconductor module of FIG. 1.

1 Claim, 10 Drawing Sheets



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FIG.1

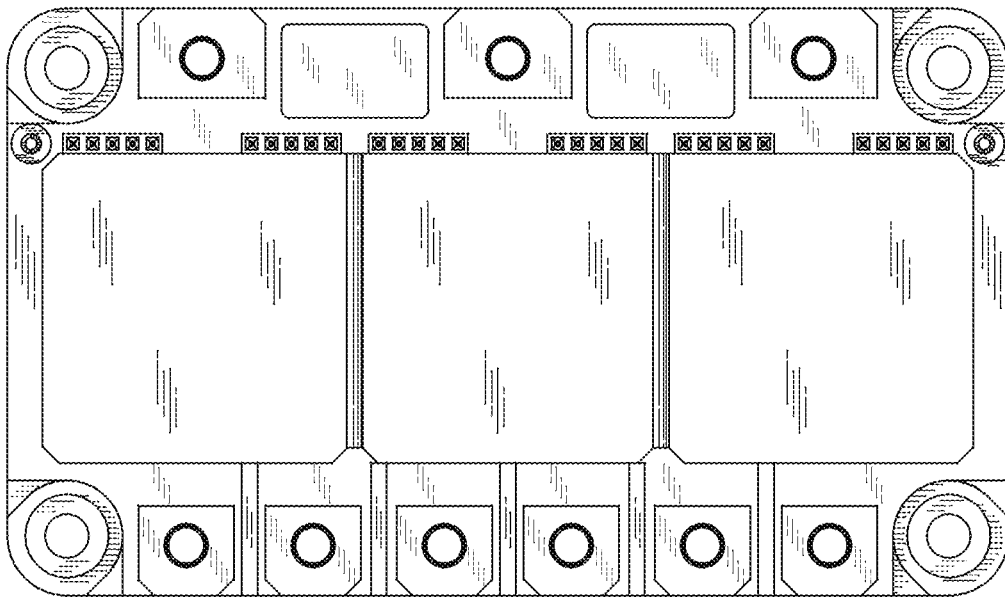


FIG.2

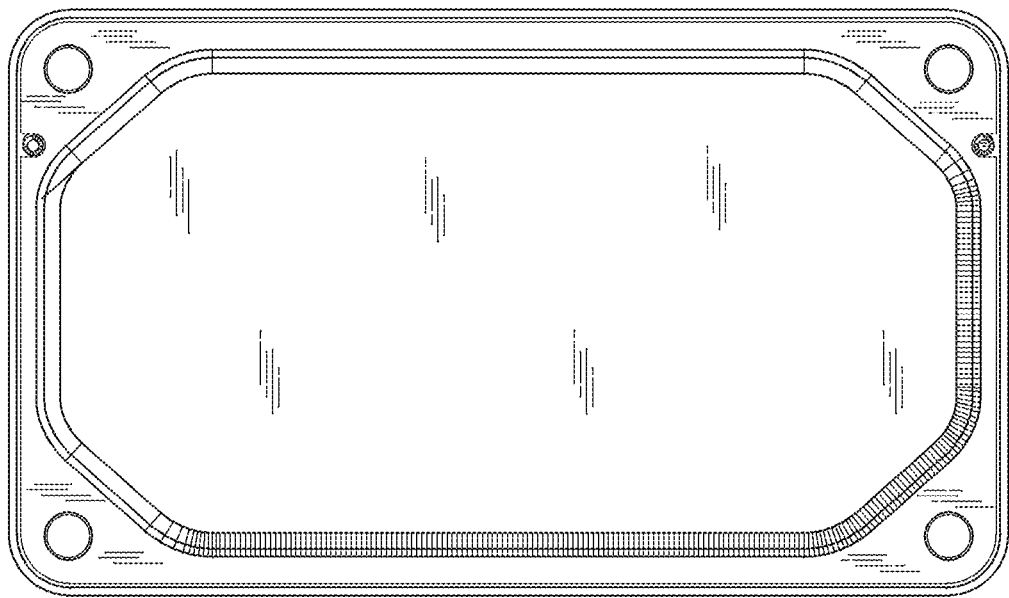


FIG.3

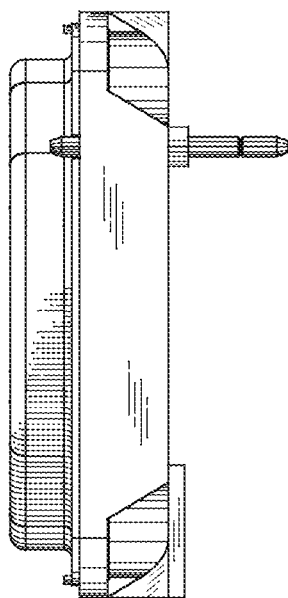


FIG.4

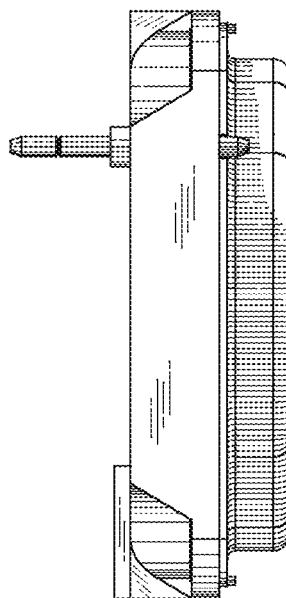


FIG.5

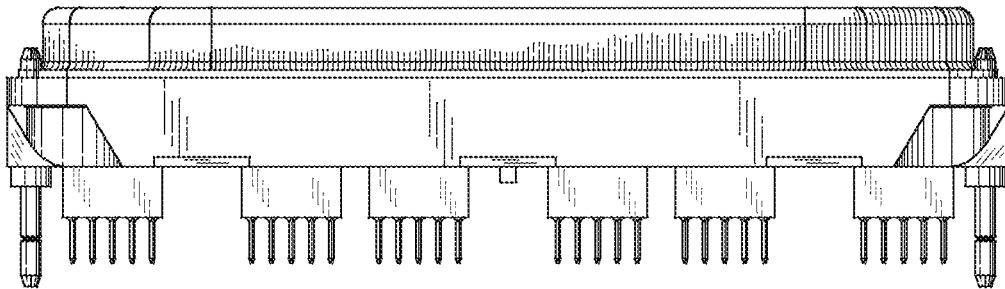


FIG.6

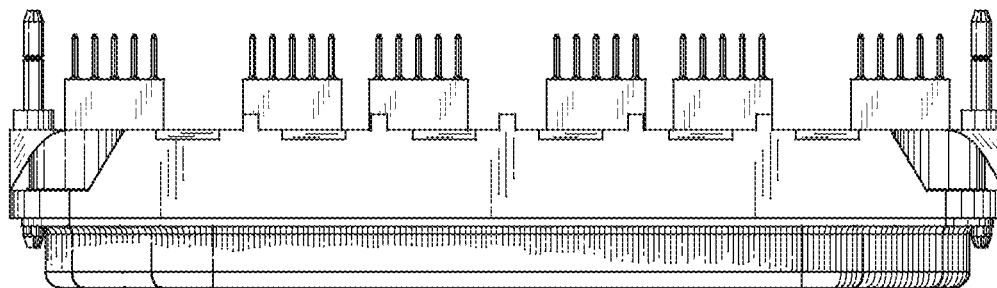


FIG.7

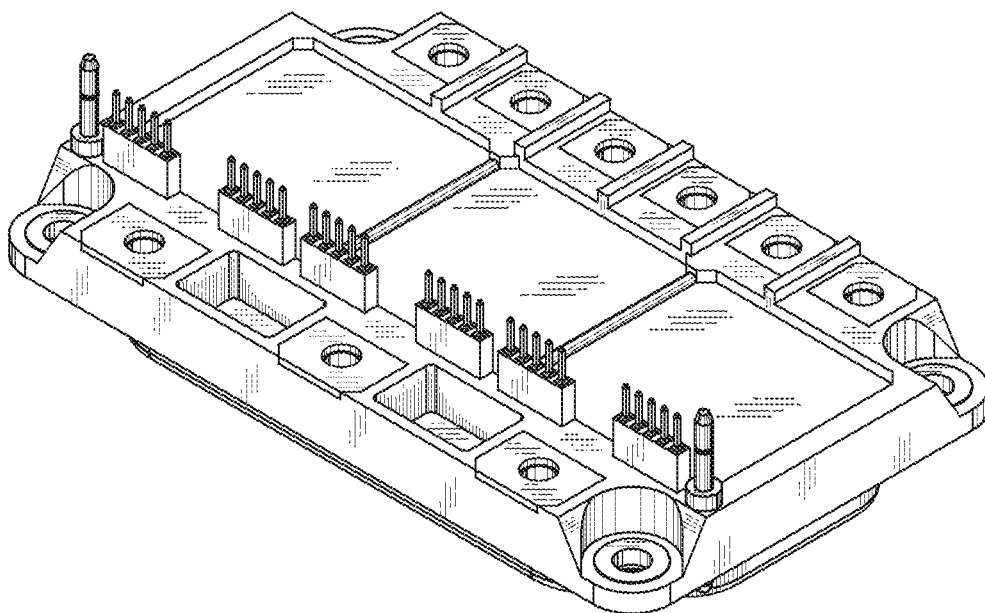


FIG.8

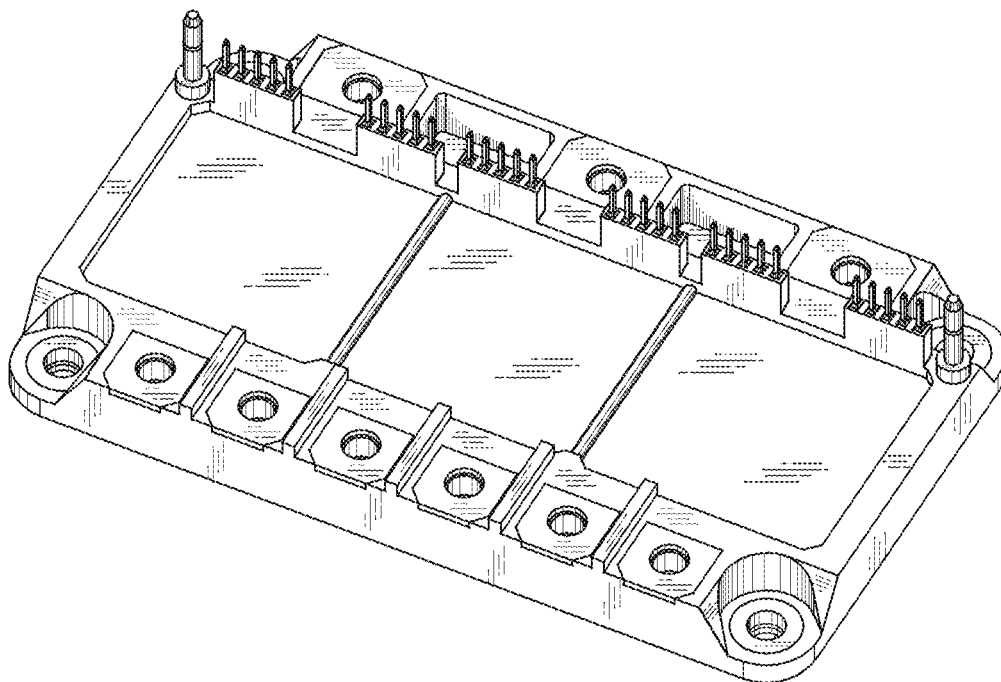


FIG.9

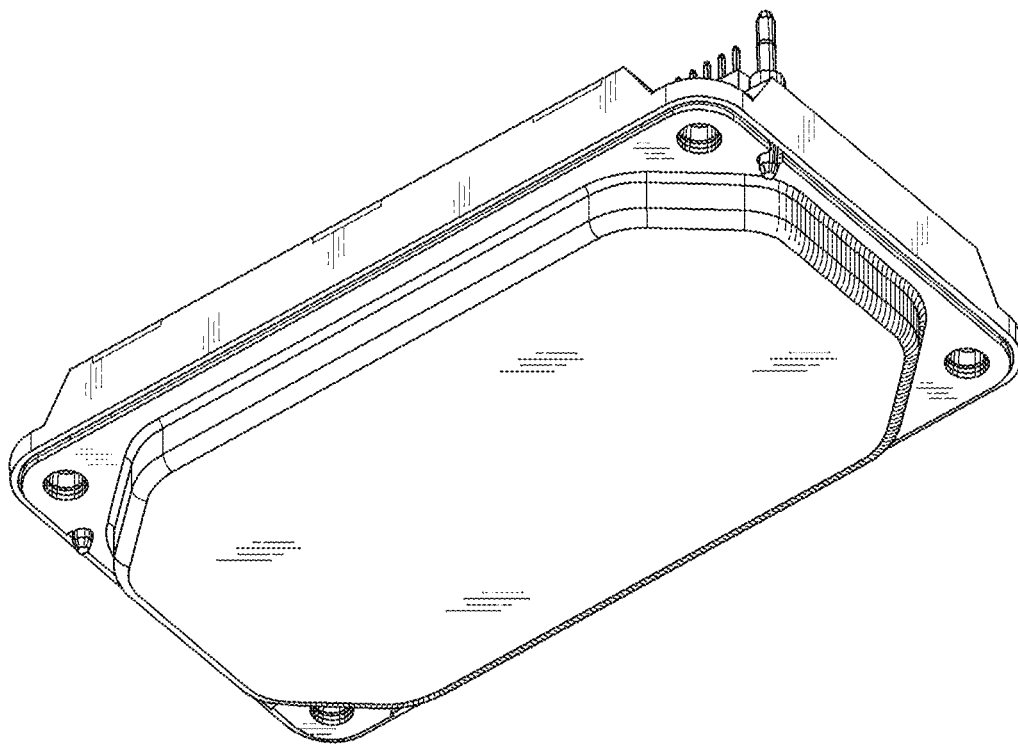


FIG.10

