



(51) International Patent Classification:

G01R 27/06 (2006.01)

G01R 31/3193 (2006.01)

G01R 31/319 (2006.01)

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(21) International Application Number:

PCT/EP2018/086419

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(22) International Filing Date:

20 December 2018 (20.12.2018)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(25) Filing Language:

English

(26) Publication Language:

English

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(54) Title: APPARATUS AND METHOD FOR TESTING A DEVICE-UNDER-TEST

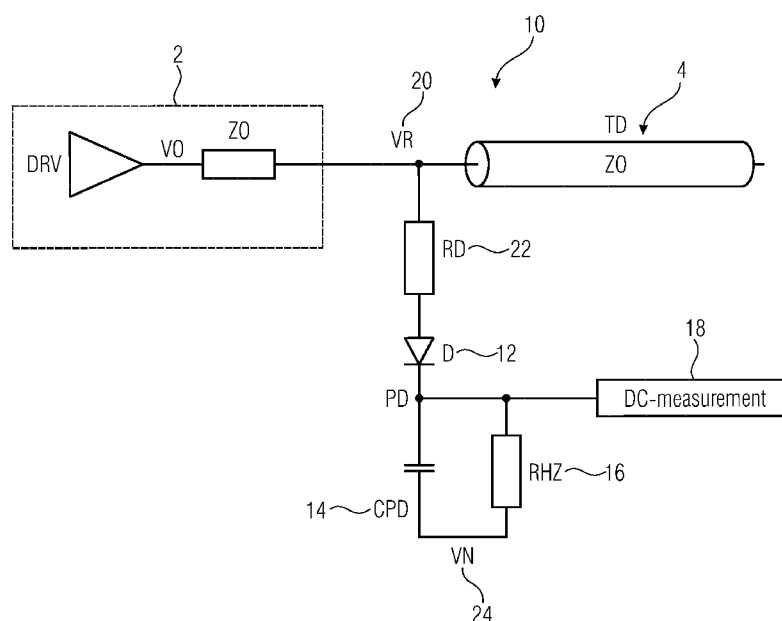


Fig. 2

(57) **Abstract:** The invention concerns devices and methods for calibration an Automated Test Equipment (ATE) for automated testing of a Device Under Test (DUT). According to an aspect of the invention, the apparatus (10) comprises a signal provider configured to generate a signal and to apply the signal to a signal path (4) which provides a reflection, and a circuit arrangement configured to determine a signal characteristic value of a result signal which is caused at a signal provider side of the signal path (4); wherein the apparatus (10) is configured to vary a period of the generated signal; and wherein the apparatus (10) is configured to obtain information about an electrical length (TD) of the signal path (4) in dependence on signal characteristic values determined for different period of the generated signal.



(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

Apparatus and Method for Testing a Device-Under-Test

Description

5

The present invention relates to testing of integrated circuits (ICs) and semiconductor devices by means of automated test equipment (ATE).

10 During a typical semiconductor manufacturing process, ICs are tested to ensure their proper operation. The ATEs perform necessary tests to ensure functionality and quality, with the ICs being devices under test (DUT). In general, a test to be performed on a DUT consists of a set of digital pattern vectors that translate to stimulus voltage levels to be applied to input signal pins of the DUT according to a pre-specified timing. Signals
15 captures from output signal pins of the DUT are translated into corresponding response vectors that may be analyzed to determine whether the DUT is operating according to its specification. The ATE generally provides a number of signal generating resources that may generate configurable signal level with configurable timing. The tester also provides signal processing resources capable of converting signals generated by the DUT (e.g. in
20 analog form) into a format (e.g. in digital form) readable by the tester. The signal processing resources may also be configurable.

A typical automated tester for integrated circuits includes a set of so-called test channels, each connected to separate pin of an IC or DUT. In an ATE System with digital
25 drive/receive channels, it is important to calibrate the timing of every channel in order to make sure that all channels generate/receive the signals at a predetermined time value, relative to the DUT. This calibration is called skew calibration.

There are various ways to calibrate the timing directly at the input/output of the pin-
30 electronics but this is only part of the problem. Since the pin-electronics usually is located on some board within the automated tester and the DUT is connected with some kind of transmission lines, either cables or pc-board traces or a combination of both. This adds some unknown timing difference, especially also due to the fact that some of this difference is in the domain of the ATE user and not in the domain of the ATE
35 manufacturer.

This poses the challenge for a timing calibration to do a measurement of this total time difference and take the result into account when doing the final time programming of each digital channel. The measurement is called TDR (time domain reflectometer) -Calibration.

5 Most digital ATE channels with moderate signal speeds are built up of a driver circuit and a receiver or comparator circuit. It is well known in the art how to do a TDR calibration with these two circuits. Fig. 1a shows a conventional driver circuit with a conventional comparator circuit to implement the TDR calibration. Fundamentally, the TDR measures the reflections that result from a signal travelling through a transmission environment of
10 some kind – a circuit board trace, a cable, a connector and so on. The TDR instrument sends a signal, for example, a pulse through the medium and compares the reflections from the unknown transmission environment to those produced by a standard impedance. The sample point of the comparator is swept at two different thresholds in order to measure the time between transmitted and reflected signal as shown in Fig. 1b.

15

However, ATE channels with very high signal speeds only consist of a dedicated driver or a dedicated receiver, mainly caused by the DUT's requirement (very high speed signals tend to be uni-directional), but also by the fact that combining both circuits on the board inside the ATE would have a significant negative effect on bandwidth, besides adding cost
20 for components which are not needed in normal operation.

25

Hence, it is an object of the present invention to provide a solution of the TDR measurement problem at a uni-directional ATE drive channel, i.e., to avoid the significant negative effect on bandwidth with minimum cost.

This object is solved by an apparatus for testing a device-under-test according to claim 1 and a method for testing a device-under-test according to claim 16.

Some embodiments of the present invention also provide a computer program for carrying
30 out steps of the invention method.

According to a first aspect of the present invention, an apparatus for testing a device-under-test may comprises a signal provider configured to generate a signal and to apply the signal to a signal path which provides a reflection, and a circuit arrangement
35 configured to determine a signal characteristic value of a result signal which is caused at a signal provider side of the signal path; wherein the apparatus is configured to vary a

period of the generated signal ,e.g., the signal is periodically generated, i.e., the period of the signal is swept; and wherein the apparatus is configured to obtain information about an electrical length of the signal path in dependence on signal characteristic values determined for different period of the generated signal. The generated signal may be one
5 of sine wave, pulses with constant pulse width, and pulses with pulse width of half of the period. The signal characteristic value may be one of root mean square voltage, power, i.e., average power, and detected peak voltage over one or more period, i.e., positive and negative.

10 According to an embodiment of the present invention, the apparatus is configured to determine the electrical length in dependence on a variation of the signal characteristic value over the period. The electrical length may be determined in dependence on a period for which the signal characteristic value fulfills a predetermined criterion, wherein the
15 predetermined criteria is one of: local minimum, local maximum, global minimum, global maximum and predetermined shape of variation over period. The circuit arrangement may comprise a peak detector configured to determine a peak signal level at the signal provider side of the signal path as the signal characteristic value.

According to an embodiment of the present invention, the circuit arrangement may
20 comprise a diode, wherein a first terminal of the diode is connected to the signal provider side, i.e., signal provider end, of the signal path, a capacitor connected between a second terminal of the diode and a voltage node, e.g., fixed voltage node, a discharge element configured to discharge the capacitor, e.g., connected in parallel to the capacitor; and DC measurement unit configured to measure a voltage at a terminal of the capacitor, for
25 example, the measured voltage represents a peak level at the signal provider side of the signal path and is the signal characteristic value. The diode may be connected with an anode to the signal provider side of the signal path and with a cathode to the capacitor, or the diode may be connected with a cathode to the signal provider side of the signal path and with an anode to the capacitor. The circuit arrangement may comprise a resistor,
30 wherein the diode is connected to the signal path via the resistor.

According to an embodiment of the present invention, one end of the signal path may be connected to the signal provider and the other end of the signal path may be terminated
35 by an impedance having a different value to a characteristic impedance of the signal path, or terminated in an open circuit, i.e., having an open end, or terminated in a short circuit. The signal provider may have a source impedance which has an equivalent value, i.e., the

difference is for example +/- 5% to a characteristic impedance of the signal path or different value from the characteristic impedance.

According to an embodiment of the present invention, the apparatus may be configured to
5 set the voltage at the voltage node to a first value in a normal mode operation, such that the diode is permanently reverse biased in the normal mode operation, and to set the voltage at the voltage node to a second value in a test mode operation, such that the diode is forward biased when a signal peak occurs in the test mode operation.

10 According to an embodiment of the present invention, the apparatus may be configured to detect one or more extrema of the measured voltage, and to determine the electrical length on the bases of the one or more detected extrema. In addition, the apparatus may be configured to detect plurality of extrema of the measured voltage, and to determine the electrical length using a ratio between periods, e.g., period duration, for which the extrema
15 occurs.

According to a second aspect of the present invention, a method for testing a device-under-test comprise generating a signal and applying the signal to a signal path which provides a reflection, and determining a signal characteristic value of a result signal which
20 is caused at a signal provider side of the signal path; wherein a period of the generated signal is varied; and wherein obtaining information about an electrical length of the signal path in dependence on signal characteristic values determined for different period of the generated signal.

25 According to a third aspect of the present invention, computer programs are provided, wherein each of the computer programs is configured to implement the above-described method, when being executed on a computer or signal processor, so that the above-described method is implemented by one of the computer programs.

30 In the followings, embodiments of the present invention are described in more detail with reference to the figures, in which

Fig. 1a shows a conventional schematic block diagram of a circuit for implementing a time domain reflection (TDR) calibration;

Fig. 1b shows a schematic detected result of the conventional circuit according to Fig. 1a;

Fig. 2 shows a schematic block diagram of a circuit for a TDR calibration
5 according to an embodiment of the present invention;

Fig. 3a to 3c shows a schematic diagram illustrating the time domain signals according to an embodiment of the present invention;

10 Fig. 4 shows a schematic diagram illustrating the detected result of the circuit according to an embodiment of the present invention; and

Fig. 5a and 5b shows a diagram illustrating a sample result of the circuit according to the present invention.

15

The following description sets forth specific details such as particular embodiments, procedure, techniques, end etc. for purposes of explanation and not limitation. It will be appreciated by those skilled in the art that other embodiments may be employed apart from these specific details. For example, although the following description is facilitated
20 using non-limiting example applications, the technology may be employed to any type of ATE. In some instances, detailed description of well-known methods, interfaces, circuits and devices are omitted so as to not obscure the description with unnecessary detail.

Equal or equivalent elements with equal or equivalent functionality are denoted in the
25 following description by equal or equivalent reference signs.

Fig. 2 schematically shows a block diagram of an apparatus 10 for testing a device-under-test (DUT) according to an embodiment of the present invention.

30 The apparatus 10 may comprise a uni-drive channel 2 including a driver circuit DRV which includes a signal provider (which is not illustrated in Fig. 2), a circuit arrangement comprising a diode D 12, a capacitor CPD 14, a discharge element, e.g., a resistor RHZ 16 and DC measurement unit 18, and a signal path 4. In the circuit arrangement, the diode D 12 having a small parasitic capacitance is connected with it's a first terminal, e.g.,
35 anode to the signal at some point in the signal chain. That is, the anode of the diode D 12 is connected to a node VR 20 via an optional low-parasitic damping resistor DR 22, where

the transmission into the unknown electrical length TD (e.g., signal path 4) starts, e.g., at the output of the driver circuit DRV of the uni-drive channel 2. The other end of the signal path 4 is not terminated, i.e., the other end of the signal path 4 is terminated at an open circuit. The characteristic impedance of the signal path 4 is Z_0 and a source impedance of the driver circuit DRV, i.e., the signal provider has the same value as the characteristic impedance. The same value means that the value of the source impedance of the signal provider could have an equivalent value, i.e., $\pm 5\%$ value of the characteristic impedance of the signal path 4. It is also possible that the value of the source impedance may have a different value from the value of the characteristic impedance. A second terminal of the diode D 12, e.g., cathode of the diode D 12 is connected to one end of the capacitor CPD 14 for effectively creating a peak detector circuit. The other end of the capacitor CPD 14 is connected to a voltage node VN 24. The voltage node VN 24 may be a fixed voltage source. The resistor RHZ 16 may be a high-impedance resistor and the resistor RHZ 16 is connected in parallel to the capacitor CPD 14. The DC measurement unit 18 is configured to measure a voltage of at a terminal of the capacitor CPD 14. The node at the peak detector (the capacitor CPD 14) is monitored by the DC measurement unit 18. The DC measurement unit 18 may be a digital volt-meter DVM or an analog-to-digital-converter ADC. The measured voltage by the DC measurement unit 18 represents a peak level at the signal provider side of the signal path 4 and is the signal characteristic value.

In a normal mode operation, i.e., the operation mode not calibrating, the voltage value at the node VN 24 is pulled above the voltage at the signal path 4 so that the diode D 12 is reverse biased and does not disturb the normal high speed drive signal. In a calibrating mode operation (a test operation mode operation), the voltage value at the node VN 24 is pulled to a value at least one diode drop, e.g., 0.7 V, below the level of the generated signal thus it is possible to detect the peak. When calibrating (in the test mode operation), the signal at the anode of the diode D 12 changes in dependence on the applied period of the generated signal. Along with the signal change at the anode of the diode D 12, the signal at the cathode of the diode D 12 also changes in dependence on the applied period of the generated signal. The generated signal V0 may be pulses with pulse width 50% of the period or sine wave or pulses with constant pulse width.

Each Fig. 3a to 3c shows time domain signals associated to an embodiment according to the present invention. If the period of the generated signal is significantly larger than 4 times the electrical length TD ($4 \times TD$), then there is a typical TDR waveform at the line and the settled peak detector shown its maximum (shown as Fig. 3a). In case the period

of the generated signal is exactly $4xTD$ ($3/4xTD$ or $4/5xTD$ or $4/7xTD$ or etc.) then the reflection occurs exactly at the provided pulse yielding a DC signal at the node VR 20 when assuming a lossless transmission line (shown as Fig. 3b). This results in a minimum voltage at the monitored peak detector, when it settled. In case the far end of the signal path 4 is shorted, i.e., the signal path is terminated at short circuit, and then there are minima when the reflections cancel the transmitted pulses. This occurs at periods of the generated signal $2xTD$ (or $2/3xTD$ or etc.) as shown in Fig 3c.

Fig. 4 shows the DC (peaked) value at node PD vs. the signal period, with very sharp minima at the distinctive periods. As indicated in Fig. 4, the reflection is occurred at the period $4/5xTD$, $4/3xTD$ and $4xTD$. This corresponds to the case indicated in Fig. 3b.

As explained above, it is possible to implement the TDR-calibration with the uni-drive channel, i.e., with the circuit without having a comparator circuit or a receiver circuit, and hence, it is possible to avoid negative effect of bandwidth with minimum cost. Furthermore, by reducing the circuit on the printed board, the accuracy of the test result is also improved.

The same approach works when using the diode D 12 connected the other way round, i.e., the diode D 12 is connected with the cathode to the signal provider side of the signal path 4 and with an anode to the capacitor CPD 14. In this case, the respective terms in the above explanation "below" and "above" for the node VN 24 and "minimum" and "maximum" at the peak detector have to be interchanged.

Fig. 5a and 5b show a sample result of a real measurement according to the present invention. The measurement environment is:

$V_0=1200m\ V_{pp}$

80 cm real coaxial cable, $TD \sim 4.4ns$

$RD=0$, $CPD=10nF$, $RHZ=100k\ ohm$

Fig. 5b is a zoom of Fig. 5a. Figs. 5a and 5b show that x-axis normalized to the minima at $4xTD$ and $4/3xTD$ (offset) and TD itself (scale). The non-ideal behavior comes from the fact that the cable has a frequency-dependent loss and therefore the reflected signal is not able to fully 'fill' the gaps in the transmitted pulses. This is however well known for the skilled person. Therefore, it should be recognized that the accuracy of the test is improved.

Although some aspects have been described in the context of an apparatus, it is clear that these aspects also represent a description of the corresponding method, where a block or device corresponds to a method step or a feature of a method step. Analogously, aspects described in the context of a method step also represent a description of a corresponding block or item or feature of a corresponding apparatus. Some or all of the method steps may be executed by (or using) a hardware apparatus, like for example, a microprocessor, a programmable computer or an electronic circuit. In some embodiments, one or more of the most important method steps may be executed by such an apparatus.

The inventive data stream can be stored on a digital storage medium or can be transmitted on a transmission medium such as a wireless transmission medium or a wired transmission medium such as the Internet.

Depending on certain implementation requirements, embodiments of the invention can be implemented in hardware or in software. The implementation can be performed using a digital storage medium, for example a floppy disk, a DVD, a Blu-Ray, a CD, a ROM, a PROM, an EPROM, an EEPROM or a FLASH memory, having electronically readable control signals stored thereon, which cooperate (or are capable of cooperating) with a programmable computer system such that the respective method is performed. Therefore, the digital storage medium may be computer readable.

Some embodiments according to the invention comprise a data carrier having electronically readable control signals, which are capable of cooperating with a programmable computer system, such that one of the methods described herein is performed.

Generally, embodiments of the present invention can be implemented as a computer program product with a program code, the program code being operative for performing one of the methods when the computer program product runs on a computer. The program code may for example be stored on a machine readable carrier.

Other embodiments comprise the computer program for performing one of the methods described herein, stored on a machine readable carrier.

In other words, an embodiment of the inventive method is, therefore, a computer program having a program code for performing one of the methods described herein, when the computer program runs on a computer.

5 A further embodiment of the inventive methods is, therefore, a data carrier (or a digital storage medium, or a computer-readable medium) comprising, recorded thereon, the computer program for performing one of the methods described herein. The data carrier, the digital storage medium or the recorded medium are typically tangible and/or non-transitionary.

10 A further embodiment of the inventive method is, therefore, a data stream or a sequence of signals representing the computer program for performing one of the methods described herein. The data stream or the sequence of signals may for example be configured to be transferred via a data communication connection, for example via the
15 Internet.

A further embodiment comprises a processing means, for example a computer, or a programmable logic device, configured to or adapted to perform one of the methods described herein.

20 A further embodiment comprises a computer having installed thereon the computer program for performing one of the methods described herein.

A further embodiment according to the invention comprises an apparatus or a system
25 configured to transfer (for example, electronically or optically) a computer program for performing one of the methods described herein to a receiver. The receiver may, for example, be a computer, a mobile device, a memory device or the like. The apparatus or system may, for example, comprise a file server for transferring the computer program to the receiver.

30 In some embodiments, a programmable logic device (for example a field programmable gate array) may be used to perform some or all of the functionalities of the methods described herein. In some embodiments, a field programmable gate array may cooperate with a microprocessor in order to perform one of the methods described herein. Generally,
35 the methods are preferably performed by any hardware apparatus.

The apparatus described herein may be implemented using a hardware apparatus, or using a computer, or using a combination of a hardware apparatus and a computer.

5 The apparatus described herein, or any components of the apparatus described herein, may be implemented at least partially in hardware and/or in software.

The methods described herein may be performed using a hardware apparatus, or using a computer, or using a combination of a hardware apparatus and a computer.

10 The methods described herein, or any components of the apparatus described herein, may be performed at least partially by hardware and/or by software.

15 The above described embodiments are merely illustrative for the principles of the present invention. It is understood that modifications and variations of the arrangements and the details described herein will be apparent to others skilled in the art. It is the intent, therefore, to be limited only by the scope of the impending patent claims and not by the specific details presented by way of description and explanation of the embodiments herein.

Claims

1. An apparatus (10) for testing a device-under-test comprising:

5 a signal provider configured to generate a signal and to apply the signal to a signal path (4) which provides a reflection, and

a circuit arrangement configured to determine a signal characteristic value of a result signal which is caused at a signal provider side of the signal path (4);

10

wherein the apparatus (10) is configured to vary a period of the generated signal; and

wherein the apparatus (10) is configured to obtain information about an electrical length (TD) of the signal path (4) in dependence on signal characteristic values determined for
15 different period of the generated signal.

2. The apparatus (10) according to claim 1, wherein the generated signal is one of sine wave, pulses with constant pulse width, and pulses with pulse width of half of the period.

20 3. The apparatus (10) according to claim 1 or 2, wherein the generated signal characteristic value is one of root mean square voltage, power, and detected peak voltage over one or more period.

4. The apparatus according to any one of claims 1 to 3, wherein the apparatus is
25 configured to determine the electrical length (TD) in dependent on a variation of the signal characteristic value over the period.

5. The apparatus (10) according to any one of claims 1 to 4, wherein the apparatus (10) is configured to determine the electrical length (TD) in dependence on a period for which the
30 signal characteristic value fulfills a predetermined criterion,
wherein the predetermined criteria is one of:
local minimum, local maximum, global minimum, global maximum and predetermined shape of variation over period.

35 6. The apparatus (10) according to any one of claims 1 to 5, wherein the circuit arrangement comprises:

a peak detector configured to determine a peak signal level at the signal provider side of the signal path (4) as the signal characteristic value.

7. The apparatus (10) according to any one of claims 1 to 6, wherein the circuit arrangement comprises:

a diode (12), wherein a first terminal of the diode (12) is connected to the signal provider side of the signal path (4),

a capacitor (14) connected between a second terminal of the diode and a voltage node (24),

10 a discharge element (16) configured to discharge the capacitor; and

DC measurement unit (18) configured to measure a voltage of at a terminal of the capacitor (14).

8. The apparatus (10) according to claim 7, wherein the diode (12) is connected with an anode to the signal provider side of the signal path and with a cathode to the capacitor (14).

9. The apparatus (10) according to claim 7, wherein the diode (12) is connected with a cathode to the signal provider side of the signal path and with an anode to the capacitor (14).

10. The apparatus (10) according to any one of claims 7 to 9, the circuit arrangement comprises a resistor (22), wherein the diode is connected to the signal path (4) via the resistor (22).

11. The apparatus (10) according to any one of claims 7 to 10, wherein one end of the signal path (4) is connected to the signal provider and the other end of the signal path (4) is terminated by or in one of:

an impedance having a different value to a characteristic impedance of the signal path,

30 an open circuit, and

a short circuit.

12. The apparatus (10) according to any one of claims 7 to 11, wherein the signal provider has a source impedance which has an equivalent $[+/- 5\%]$ value to a characteristic impedance of the signal path (4) or different value from the characteristic impedance.

13. The apparatus (10) according to any one of claims 7 to 12, wherein the apparatus (10) is configured to set the voltage at the voltage node to a first value in a normal mode operation, such that the diode is permanently reverse biased in the normal mode operation, and to set the voltage at the voltage node (24) to a second value in a test mode operation, such that the diode (12) is forward biased when a signal peak occurs in the test mode operation.

14. The apparatus (10) according to any one of claims 7 to 13, wherein the apparatus (10) is configured to detect one or more extrema of the measured voltage, and to determine the electrical length (TD) on the bases of the one or more detected extrema.

15. The apparatus (10) according to claim 14, wherein the apparatus (10) is configured to detect plurality of extrema of the measured voltage, and to determine the electrical length (TD) using a ratio between periods for which the extrema occurs.

16. A method for testing a device-under-test, the method comprising:
generating a signal and applying the signal to a signal path (4) which provides a reflection, and
determining a signal characteristic value of a result signal which is caused at a signal provider side of the signal path (4);
wherein a period of the generated signal is varied; and
wherein obtaining information about an electrical length (TD) of the signal path (4) in dependence on signal characteristic values determined for different period of the generated signal.

17. A computer program for performing the method according to claim 16, when the computer program is running on a computer or a processor of an apparatus.

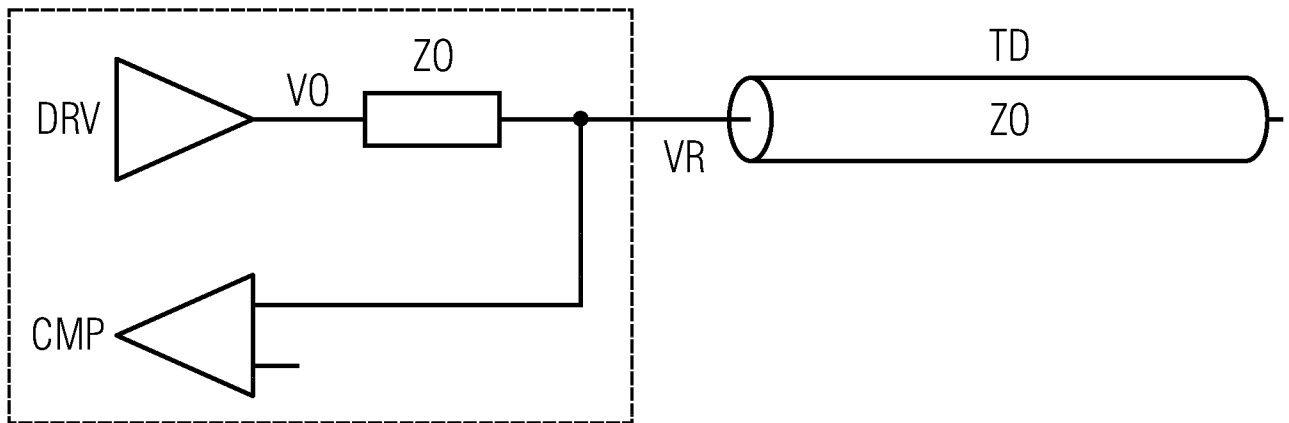


Fig. 1a
(PRIOR ART)

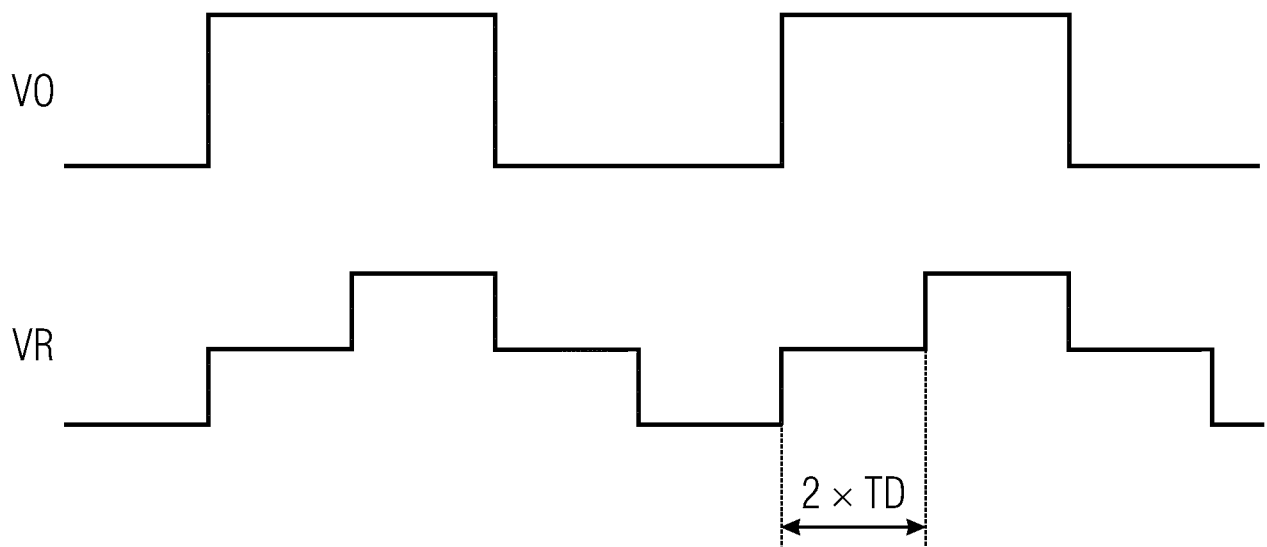


Fig. 1b

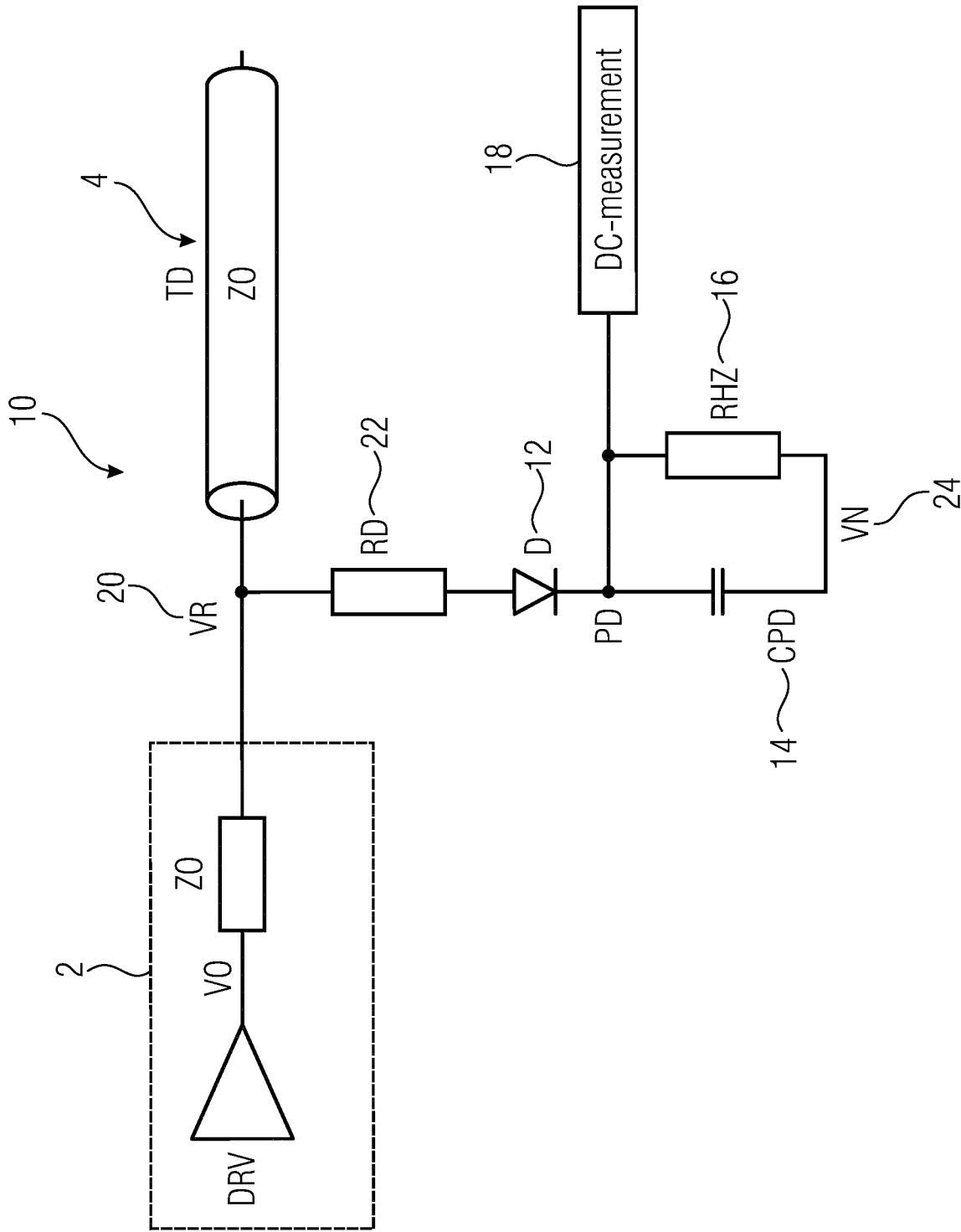


Fig. 2

3/6

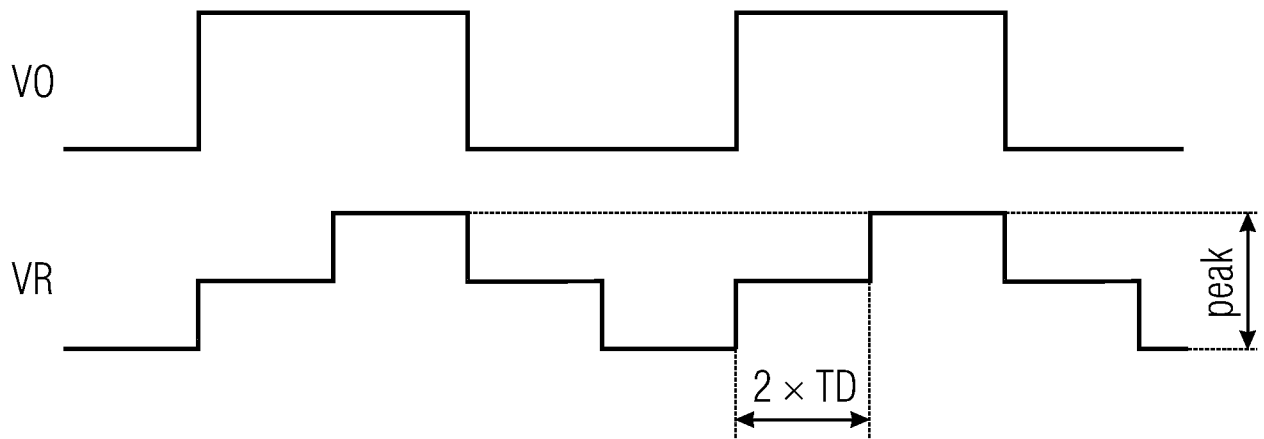
period $> 4 \times TD$ 

Fig. 3a

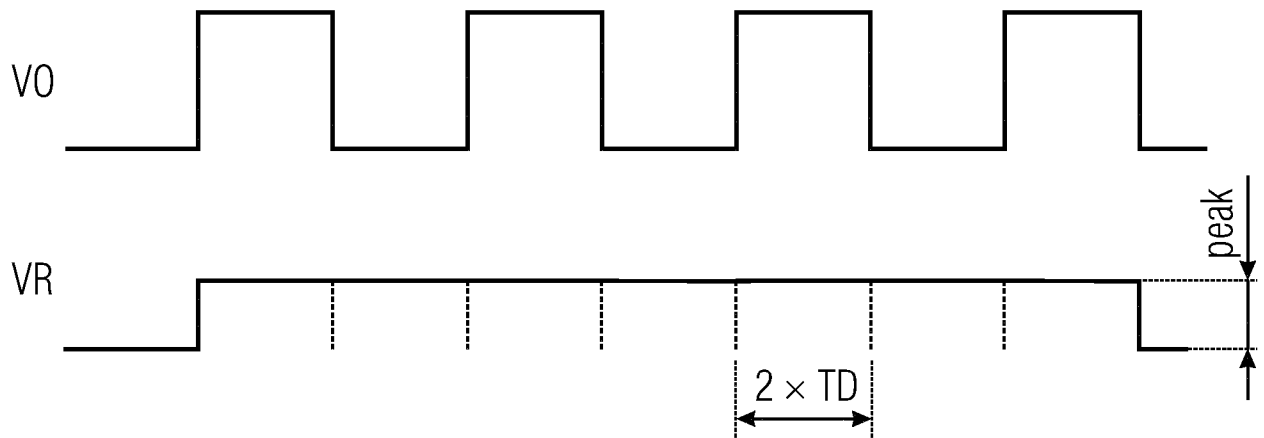
period $= 4 \times TD$ 

Fig. 3b

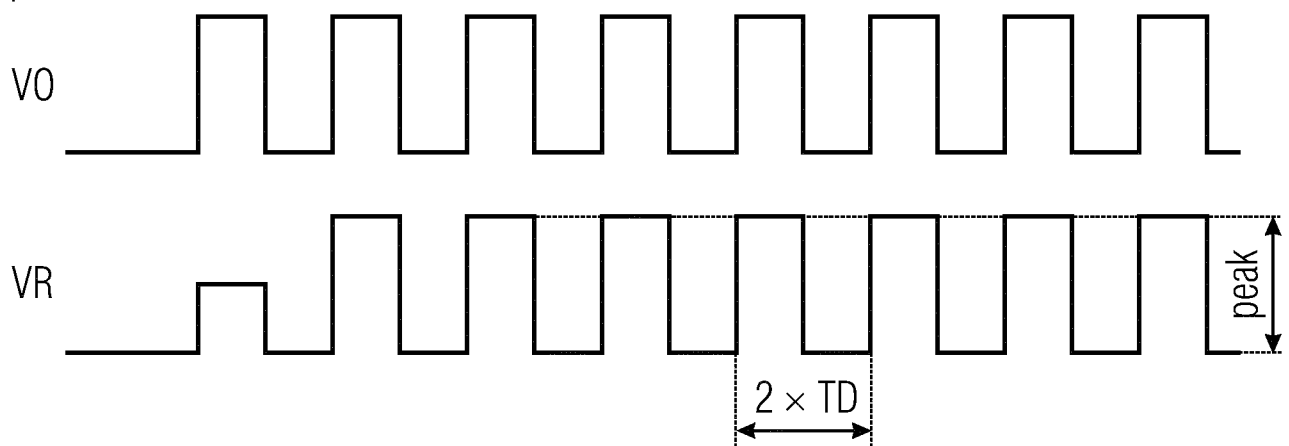
period $= 2 \times TD$ 

Fig. 3c

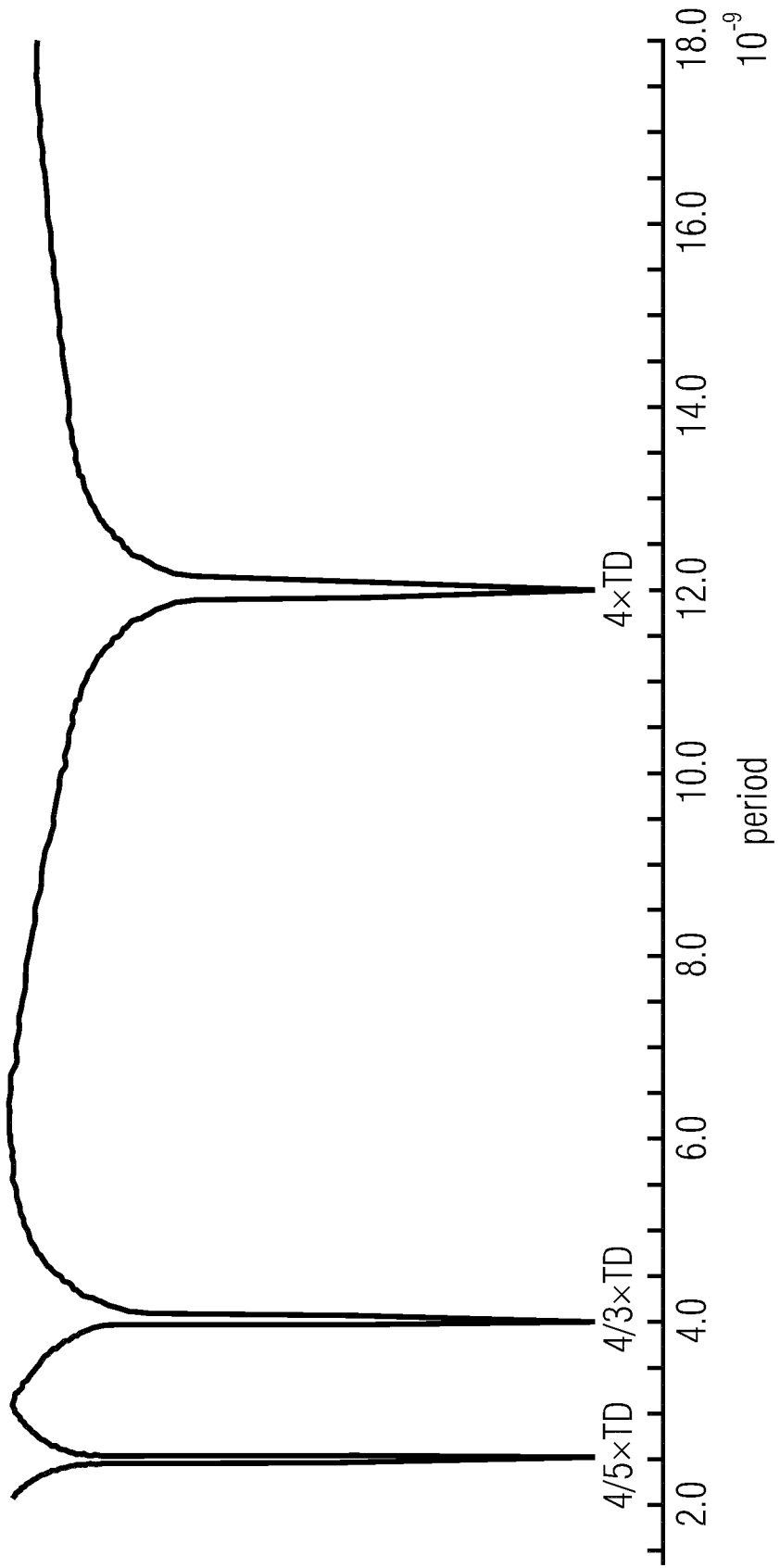


Fig. 4

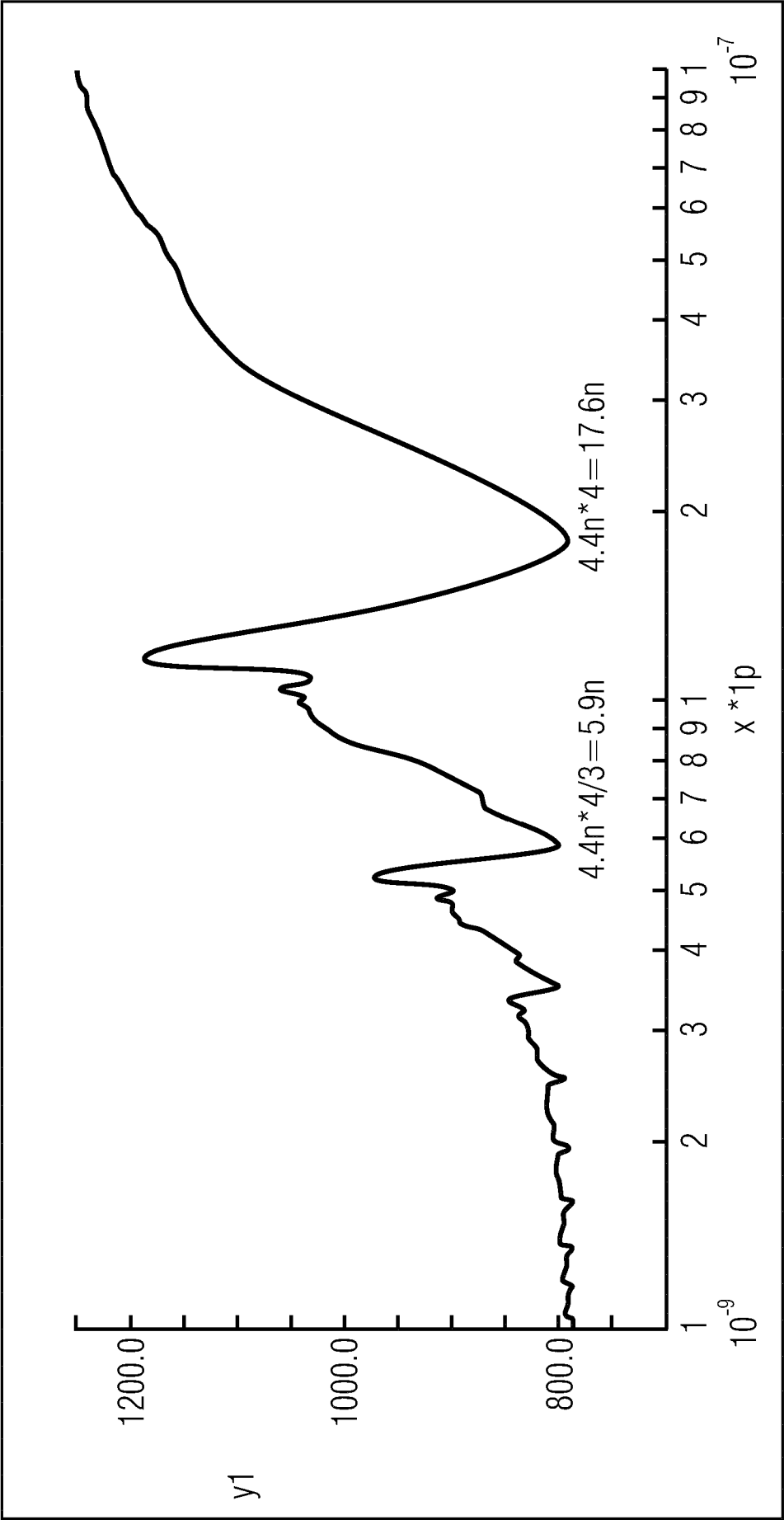


Fig. 5a

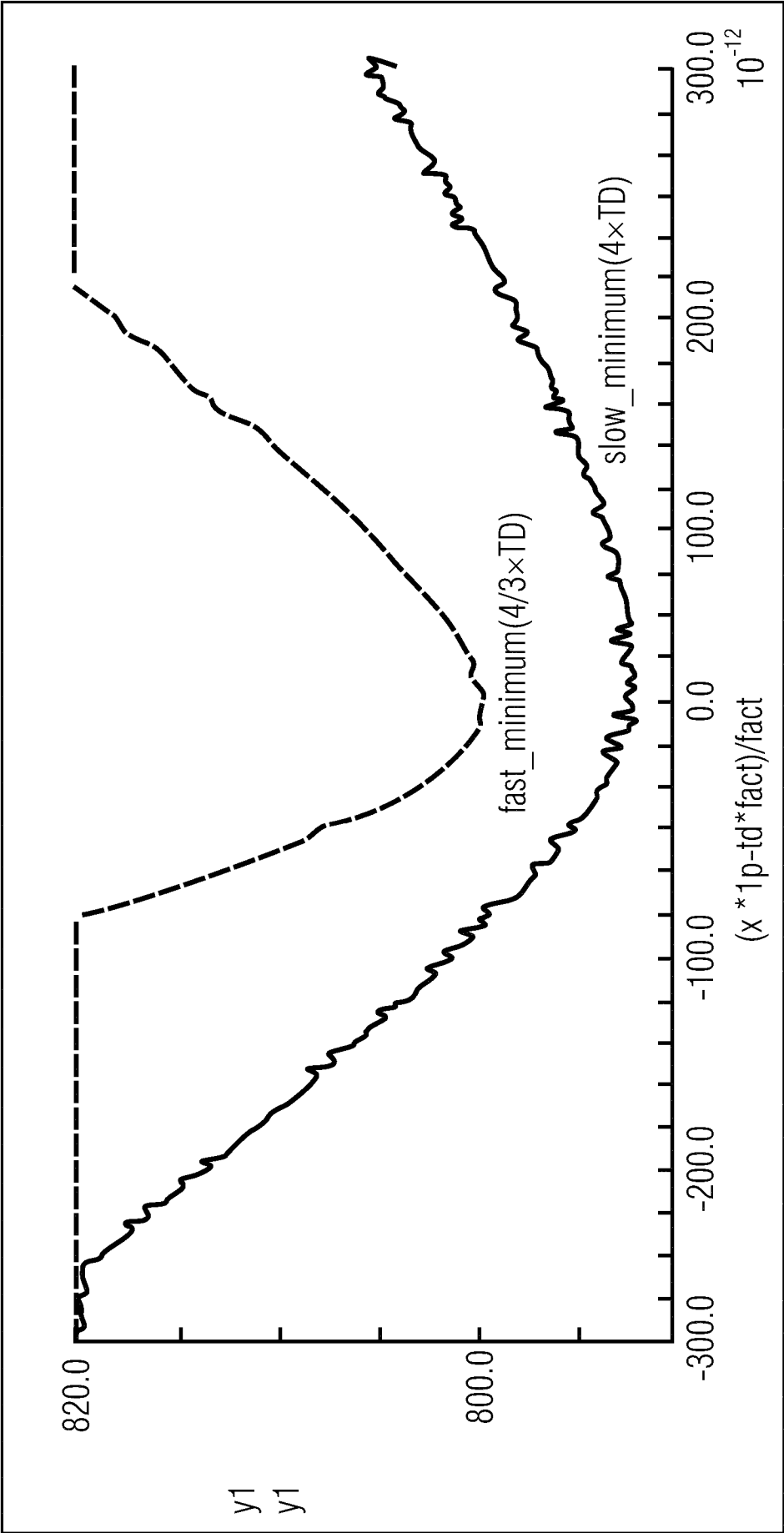


Fig. 5b

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2018/086419

A. CLASSIFICATION OF SUBJECT MATTER

INV. G01R27/06 G01R31/319 G01R31/3193
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 630 228 A (TARCZY-HORNOCH ZOLTAN [US] ET AL) 16 December 1986 (1986-12-16) figures 1-3 -----	1-5, 16, 17
A	US 6 609 077 B1 (BROWN BENJAMIN [US] ET AL) 19 August 2003 (2003-08-19) figures 1, 4, 6 -----	1
A	US 2012/081129 A1 (NEGISHI TOSHIYUKI [JP]) 5 April 2012 (2012-04-05) figures 1, 2 -----	1
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26 August 2019

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18/09/2019

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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