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(54) Title: METHOD AND DEVICE FOR DETERMINING THE GAIN DISTRIBUTION BETWEEN THE ANALOG AND THE DIGITAL STAGES OF A RADIO RECEIVER

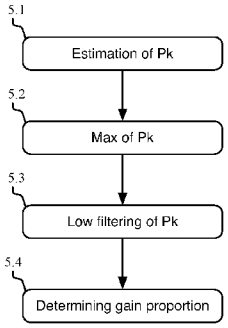


Fig. 5

(57) Abstract: Determining the gain distribution between the analog and the digital stages of a radio receiving device by estimating for each automated gain control period the instantaneous blocker power level, said device implementing an automated gain control mechanism to adjust the level of the received signal, the global gain to be applied being distributed between an analog stage and a digital one separated by an analog to digital converter, the gains being applied by automated gain control commands triggered regularly, the time between two consecutive automated gain control commands defining the automated gain control period; calculating the maximum of the estimated instantaneous blocker power level over a number of automated gain control periods to obtain a slow-varying value of the blocker power level and distributing the automated gain control command between the analog and the digital stage according to this slow- varying value of the blocker power level.

Method and device for determining the gain distribution between the analog and the digital stages of a radio receiver

The present invention generally relates to automatic gain control in a mixed analogue and digital wireless receiver in the presence of intermittent blockers.

Automatic gain control or AGC systems are known and widely used. The purpose of the AGC system is to adjust the level of a received signal in the receiver at an input of an analogue to digital converter (ADC). The AGC system controls the receiver gain in order to keep the signal level at the ADC input as close as possible to a reference level, in order to avoid saturation of the ADC, whilst ensuring that the full range of the ADC is utilized to thereby provide the required signal to noise ratio (SNR) in the sampled signal. A further purpose of the AGC is to maintain the level of the receiver baseband (BB) output signal as close as possible to a reference level.

The general principle of AGC systems comprises measuring the received signal and using that measurement in computing and setting a required gain for the receiver. Generally, an average power may be measured over a given duration of time and the measured average power then used in the AGC system. The duration of time over

which the average power measurement is taken determines the rate at which the AGC system updates the receiver gain. It is called the AGC period.

Fig. 1 illustrates the general architecture of a mixed analog and digital wireless receiver. The signal received from the antenna is affected by a first gain in the analog part of the receiver. This analog gain can be modeled as an analog amplifier 1.1. The signal is also affected by a first analog filter 1.2 in an attempt to keep only signals within the useful band and to discard all signals outside this useful band. Ideally this filter would be perfectly rectangular. In the real world, signals close to the useful band are likely to be kept while attenuated.

The signal is then converted to digital by the ADC 1.3. While converted, a digital filter 1.4 is applied to the signal to complete the elimination of the out of band signal. A digital amplifier 1.5 is then used to bring the signal in the proper dynamic range for subsequent processing by the receiver baseband.

A blocker refers to an interfering signal that occupies a frequency band that is close to the one of the useful signal. As such, it is likely to be only partially attenuated by the analog filter. If the power of this blocker is greater than the power of the useful signal, it should be taken into account to adapt the analog gain in order to avoid saturation at the ADC.

If the analog gain is lowered to tolerate a strong blocker in the analog stage, an increase of the digital gain should compensate this in the digital stage in order to achieve a same power level of the output signal.

Therefore it is advantageous to take into account the possible presence of such blocker in the signal in order to adapt the sharing out of the gain appropriately between the analog and the digital stage.

To that end, the present invention concerns a method for determining the gain distribution between the analog and the digital stages of a radio receiving device, said method causing the device to perform:

- estimating for each automated gain control period the instantaneous blocker power level, said device implementing an automated gain control mechanism to adjust the level of the received signal, the global gain to be applied being distributed between an analog stage and a digital one separated by an analog to digital converter, the gains being applied by automated gain control commands triggered regularly, the time between two consecutive automated gain control commands defining the automated gain control period;

- calculating the maximum of the estimated instantaneous blocker power level over a number of automated gain control periods to obtain a slow-varying value of the blocker power level;

- distributing the automated gain control command between the analog and the digital stage according to this slow-varying value of the blocker power level.

Therefore, in presence of an intermittent blocker, the power of this blocker is taken into account even for the AGC period where it is not present.

The present invention also concerns a device for determining the gain distribution between the analog and the digital stages of a radio receiving device, the device comprising circuitry causing the device to implement:

- means for estimating for each automated gain control period the instantaneous blocker power level, said device implementing an automated gain control mechanism to adjust the level of the received signal, the global gain to be applied being distributed between an analog stage and a digital one separated by an analog to digital converter, the gains being applied by automated gain control commands triggered regularly, the time between two consecutive automated gain control commands defining the automated gain control period;

- means for calculating the maximum of the estimated instantaneous blocker power level over a number of automated gain control period to obtain a slow-varying value of the blocker power level;

- means for distributing the automated gain control command between the analog and the digital stage according to this slow-varying value of the blocker power level.

The present invention also concerns, in at least one embodiment, a computer program that can be downloaded from a communication network and/or stored on a medium that can be read by a computer or processing device. This computer program comprises instructions for causing implementation of the aforementioned method, or any of its embodiments, when said program is run by a processor.

The present invention also concerns an information storage means, storing a computer program comprising a set of instructions causing implementation of the aforementioned method, or any of its embodiments, when the stored information is read from said information storage means and run by a processor.

The characteristics of the invention will emerge more clearly from a reading of the following description of an example embodiment, the said description being produced with reference to the accompanying drawings, among which:

Fig. 1 illustrates the general architecture of a mixed analog and digital wireless receiver.

Fig. 2 illustrates the evolution of power of the signal throughout the receiving chain.

Fig. 3 illustrates the amplification scheme in presence of a blocker.

Fig. 4 illustrates the case where the blocker appears and disappears at a pace comparable to the AGC rate.

Fig. 5 illustrates the general method steps used to determine the AGC gain distribution between the analog and the digital stage.

Fig. 6 illustrates the determination of the instantaneous power level P_k between two AGC commands according to certain embodiment.

Fig. 7 illustrates the measurement of the elementary power according to certain embodiment.

Fig. 8 illustrates the further step to obtain a slow-varying value of the blocker power level.

Fig. 9 schematically represents an architecture of a receiver device in which the present invention may be implemented.

Fig. 1 is to be considered as a model of the receiver. In a real receiver, the respective placement of the analog amplifier and filter on one hand, and the digital amplifier and filter on another hand, could differ. It should be understood that the amplification and filter could consist of several amplifiers and filters throughout the analog or digital stage. This reality is modeled in this generic example as one amplifier and one filter in each stage, analog and digital.

Fig. 2 illustrates the evolution of power of the signal throughout the receiving chain. Fig. 2a illustrates the input signal when no blocker occurs. We have a useful signal 2.1 and thermal in band noise 2.2. The figure shows their respective power level. Power level 2.3 represents the target level at the ADC input and power level 2.4 represents the target level at the receiver output.

Fig. 2b illustrates the signal at the output of the ADC. The signal has been amplified in order to have the useful signal power level 2.1 approaching the target

level at the ADC input 2.3. Due to the conversion, a quantization noise 2.5 appears in the signal. Its level is low enough to be neglected.

Fig. 2c illustrates the signal after the digital amplification. The useful signal 2.1 is amplified to match the output target level 2.4. Noise is amplified accordingly while remaining in an acceptable range.

We can notice that, with no blocker present, it is the power level of the useful signal that proportions the level of gain to be applied in the analog stage to match the ADC input target level. This level of analog gain can hence be set quite high if the signal is weak. It is also to be noted that the noise introduced by the amplifier itself is not much increased compared to the signal thanks to LNA (Low Noise Amplifier) components which feature a low noise figure (NF) when applying a large gain. This leads to a good signal to noise ratio (SNR). On the figure, the SNR can be visualized by the difference between the power level of the useful signal 2.1 and the power level of the in band thermal noise 2.2, the power level of the quantization noise 2.5 being neglected, at the output on Fig. 2c.

Fig. 3 illustrates the amplification scheme in presence of a blocker. Fig. 3a corresponds to Fig. 2a with the useful signal 3.1, the in band thermal noise 3.2. It shows the power level 3.3 that represents the ADC input target level and the power level 3.4 that represents the receiver output target level. The power level of the blocker is illustrated by the bar 3.6. It is typically greater than the useful signal power level. As the band of the blocker is very close to the one of the useful signal, the analog filtering fails to suppress it efficiently.

If we apply the same analog gain value as before, the useful signal is correctly amplified but the blocker whose power level is greater will be amplified beyond the ADC dynamic. This results in saturation in the ADC and likely a loss of the signal.

In that case we have to distribute the analog gain relatively to the power level of the blocker and not the useful signal.

Fig. 3b illustrates the analog gain application. A low gain is applied in order to bring the power level of the blocker in the dynamic of the ADC. The increase of the noise power level 3.2 is comparatively greater than the amplification applied to the useful signal. This is due to a greater NF due to the use of the LNA with a lower gain. In this range of gain value, typically, these components are less efficient regarding to the noise amplification. Some quantization noise 3.5 appears after conversion.

The digital filtering is then applied resulting in a strong attenuation of the blocker 3.6 as can be noticed on Fig. 3c. A digital amplification is then applied to bring the useful signal to the expected output level. The SNR, visualized by the difference between the power level of the useful signal 3.1 and the power level of the in band thermal noise 3.2, the power levels of the quantization noise 3.5 and of the blocker 3.6 being neglected, is lower than previously due to the greater noise figure for a low level of analog gain.

As can be noticed, in absence of a blocker, we should apply a relatively great value of analog gain in order to make the useful signal level reach its target at the ADC input. This results in a low noise figure and a good SNR. On the contrary, in presence of a strong blocker, one should apply a smaller analog gain compensated by a stronger digital gain to make the total power level reach its target at the ADC input.

We also notice that, on the one hand, using the value of analog gain dedicated to a signal without blocker in presence of such blocker will lead to saturation of the ADC and likely to a loss of signal. On the other hand, using a low analog gain in absence of a blocker leads to a lower SNR while not leading to a loss of signal.

AGC is in charge of applying a global gain to the received signal in order to set its power at the RF output to a predefined level. This global gain must be split over several stages throughout the receiver, some being located before the ADC, others being located after it (analog and digital gains respectively). If an adjacent blocker is present and if it cannot be sufficiently attenuated by the receiver's analog filters, then the signal quality can be dramatically degraded due to saturation/clipping effects in the analog chain up to the ADC. This can be avoided by adapting the gain mapping strategy depending on whether a blocker has been detected or not.

The presence of an adjacent blocker can be detected, and its power estimated, by performing two different power measurements. The first one is taken before the digital filters, where the blocker has only been slightly attenuated by the analog filters. It is often referred to as wide-band power measurement. The second one is taken after the digital filters, where it is assumed that the blocker power has been rejected far below the one of the useful signal itself.

Once a good estimate of the blocker power is obtained, gain mapping can be done optimally by either decreasing the analog gains if a powerful blocker is present and compensating with higher digital gains afterwards to set the useful signal power to

its target level, or by increasing the analog gains if possible to optimize the SNR if no blocker is interfering.

A problem arises though when the blocker is not continuously present, as is the case with signals that have an inherent intermittent nature, transmitting in bursts, or hopping from a frequency band to another for instance. Since gains are switched when AGC commands are issued, which occurs with a given periodicity, based on power measurements that are made in between, it may happen that the adaptive gain mapping reacts too late. Indeed, the gains that are applied throughout a given time frame actually depend on what occurred during the previous time frame, and they may not be appropriate if the blocker appears and disappears at a pace comparable to the AGC rate. This issue is illustrated in Fig. 4.

Fig. 4 illustrates 5 successive AGC periods called P1 to P5. Boundaries of periods, namely 4.1 and 4.2 are the moments when AGC commands are applied. Fig. 4 illustrates the useful signal 4.3 and an intermittent blocker 4.4 and 4.5. We suppose the preceding period before P1 does not include a blocker. Therefore the analog gain value has been determined as high by the command 4.1 at the beginning of AGC period P1. The line 4.11 shows the analog gain level. We can notice that it is high during period P1 illustrated by reference 4.6. When the blocker 4.4 appears, this high analog gain value leads to saturation during period 4.7.

During the AGC period P1, some power measurement is done and leads to the detection of the blocker 4.4. Consequently, the analog gain is set to low value during the next period 4.8, namely P2. But during P2 the blocker has disappeared. Therefore, during P2 a low analogue gain level is applied as the system would have benefited from a high level of analogue gain level.

Due to the measurement during P2, the absence of the blocker is detected and the level is set to a high level for P3. This time, as there are no blockers during P3, this is correct.

Accordingly, a high analog gain level is determined for P4 leading to a saturation during 4.9 when the blocker 4.5 reappears. The detection of the blocker 4.5 during P4 leads to a low level of analogue gain determined for P5, which is not necessary.

Analog gains are high when the blocker appears, which causes saturation/clipping. They are set low in reaction to that but it is now useless as the blocker is already gone. When the blocker reappears the analog gains will have been

set high again, and the same problem will occur again. Also, in addition to saturation issues, switching analog gains too often can also degrade SNR because of transient effects it induces. It would be better in such a situation to keep the analog gains to a low value all the time so that no saturation occurs when the blocker reappears.

Fig. 9 schematically represents an architecture of a receiver device in which the present invention may be implemented.

According to the shown architecture, the receiver 9.1 device comprises the following components interconnected by a communications bus 9.7: a processor, microprocessor, microcontroller or CPU (*Central Processing Unit*) 9.2; a RAM (*Random-Access Memory*) 9.3; a ROM (*Read-Only Memory*) 9.4; an SD (*Secure Digital*) card reader 9.5, or any other device adapted to read information stored on storage means; a communication interface 9.6.

The communication interface 9.6 allows the receiver device to wirelessly communicate with a transmitter device.

CPU 9.2 is capable of executing instructions loaded into RAM 9.3 from ROM 9.4 or from an external memory, such as an SD card. After the receiver device has been powered on, CPU 9.2 is capable of reading instructions from RAM 9.3 and executing these instructions. The instructions form one computer program that causes CPU 9.2 to perform some or all of the steps of the algorithms described hereafter with regard to Figs. 5.

Any and all steps of the algorithms described hereafter with regard to Figs. 5 may be implemented in software by execution of a set of instructions or program by a programmable computing machine, such as a PC (*Personal Computer*), a DSP (*Digital Signal Processor*) or a microcontroller; or else implemented in hardware by a machine or a dedicated component, such as an FPGA (*Field-Programmable Gate Array*) or an ASIC (*Application-Specific Integrated Circuit*).

In other words, the receiver device includes circuitry, or a device including circuitry, causing the receiver device to perform the steps of the algorithms described hereafter with regard to Figs. 5. Such a device including circuitry causing the receiver device to perform the steps of the algorithms described hereafter with regard to Figs. 5 may be an external device connectable to the receiver device. Such receiver device may also be installed as part of another device. In example, this kind of installation would be useful when the receiver device is in form of a chip, a chipset, or a module. Alternatively, instead of being installed in or connected to a dedicated communication

device, the receiver device according to the invention may provide communication capability to any suitable device, such as a computer device, a machine, in example, a vending machine, or a vehicle like a car or truck, where the device may be installed in or connected to for this purpose. The term circuitry refers either to hardware implementation, consisting in analogue and/or digital processing, or to a combination of hardware and software implementation, including instructions of computer program associated with memories and processor causing the processor to perform any and all steps of the algorithms described hereafter with regard to Figs. 5.

Fig. 5 illustrates the general method steps used to determine the AGC gain distribution between the analog and the digital stages.

In a first step 5.1, we determine for each AGC period an estimation of the "instantaneous" blocker power level, denoted P_k.

Once we have this estimated power level for each AGC command, we calculate in a step 5.2 a new value called P_{kmax}. This value is the maximum of the P_k values over a number N_k of AGC periods, keeping the maximum P_k value observed over a programmable number N_k of AGC periods. The N_k value to use should be determined based on the AGC period and on the maximum expected time between two consecutive appearances of the blocker.

Optionally, a low-pass filter is applied to the results to smooth the blocker power level estimate over time in a step 5.3 resulting in a new value P_{blk}. If the low-pass filter is not applied, then P_{blk} is equal to P_{kmax}.

Finally, the distribution of the AGC command between the analog and the digital stage is determined according to this slow-varying value of the blocker power level in a step 5.4.

Advantageously, the step of determining the distribution of the gain also comprises a step to enable an immediate decrease of the analog gain in case of a sudden detection of a blocker. This is to face the apparition of a new blocker. As we have already seen, the application of a high level of analog gain in case of the presence of a blocker leads to signal loss. To avoid this, it is profitable to immediately decrease the analog gain level when a new blocker is detected.

One important aspect lies in the fact that the useful signal power and the blocker power are separated and processed on two different time scales. This enables the gain mapping mechanism to be as reactive as needed when AGC commands are issued in

order to follow the signal power variations, while preventing it from switching analog gains uselessly when a powerful intermittent blocker is present.

According to a certain embodiment, the instantaneous power level P_k between two AGC commands is determined according to Fig. 6. The considered AGC period is the period between a first AGC command 6.1 and a second one 6.2. The power of the signal is computed over a time window 6.3 shorter than the AGC period. In some embodiments, the power is measured on a sliding window. In that case, successive elementary power measurements are performed, one for each window, the window being slightly shifted in time. These elementary power measures are illustrated by the hairpins on the bottom line. The maximum value 6.4 over the AGC period is retained as the instantaneous power level P_k for this AGC period.

Advantageously, the power measurements must reflect the peak power observed during an AGC period and not the average power. Hence, the window size may be chosen according to the shortest expected power variation time frame, which could be imposed by either the signal or the blocker, depending on their respective characteristics. For example: the power of an LTE signal can change every symbol (~71µs) whereas the power of a GSM blocker can change every GSM slot (577µs). In that case the window duration should be, for example, close to 71µs.

The elementary power measurement could be done according to the method illustrated Fig. 7, while other methods could also be adopted.

The two power measurements *M1* and *M2* are taken before and after the digital filters 7.1. They are expressed in dB scale to facilitate computations (the exact way the conversion from linear scale to dB scale is done is not described here as it is out of the scope of the invention). Note that *M1* and *M2* are only relative power levels: the total gain G_{tot} applied up the receiver chain must also be taken into account to obtain the absolute signal power P_{in} referred at the antenna output, $P_{in} = M1 - G_{tot}$.

It is recommended that *M1* be taken just before the digital filters that suppress the blocker and *M2* just after them, other filters that would have no effect on the useful signal power and blocker power do not count here. Other options are possible though: *M1* taken somewhere up the analog part of the receiver, which requires an additional ADC; *M2* taken after the digital gains 7.2, which requires taking the digital gains into account in the subsequent calculations.

The variable $P_{diff} = M1 - M2$ gives a rough estimation of the total power that has been suppressed by the digital filters. As those filters are supposed to be adapted

to the useful signal, any loss of power can be attributed to an adjacent blocker. Since *M1* and *M2* are in dB scale P_{diff} does not exactly reflect the lost power, however the instantaneous blocker power P_k can easily be estimated by examining its value:

- $P_{diff} \gg 0$ means that a strong blocker is present and that its contribution to *M1* is prominent. P_k can be set equal to *Pin* without much loss of accuracy.
- $P_{diff} \approx 0$ means that the useful signal is prominent in *M1:* the blocker is either weak or not there at all. P_k can be set equal to the minimal possible value that the digital system can represent. It is to be noted here, that P_{diff} is a log and would be minus infinity theorically.
- When P_{diff} falls between those two extreme cases a programmable threshold THP_{diff} can be used to select which case to follow: $P_k = P_{in}$; if $P_{diff} > THP_{diff}$, P_k set to the minimum otherwise. A small error is then made in estimating P_k that has no significant effect on performance if the threshold is rightly chosen.

Alternatively, a more sophisticated mechanism can be used to yield a more accurate value of P_k, involving more conversions from linear to dB scale and vice versa. Alternatively, a look-up table could be used to get the difference $(M1 - P_k)$ based on P_{diff}, then compute P_k from *M1*.

Fig. 8 illustrates the further step to obtain P_{kmax}. This value 8.3 is obtained by keeping the maximum of P_k values 8.2 over N_k AGC period 8.1. N_k should be programmable and its value is determined based on the AGC period 8.1 and on the maximum expected time between two consecutive appearances of the blocker. That way, P_{kmax} is ensured to remain quite steady over time, its variations being tightly correlated with the long-time fluctuations of the blocker power but not affected by its intermittent properties.

Then, the optional step of low-pass filtering of the P_{kmax} value could be done, for example, by a first order IIR (Infinite Impulse Response) filter. As an example, the filter having the following transfer function can be used:

$$H(z^{-1}) = \frac{\alpha}{1 - (1 - \alpha)z^{-1}}$$

Where $\alpha < 1$ determines the cut-off frequency.

The low-pass filtered power value obtained is called P_{blk}. If no filter is used, $P_{blk} = P_{kmax}$.

Gain mapping is performed each time an AGC command is issued. An AGC command may comprise an estimate of the useful signal power P_{sig}, or directly the total gain G_{tot} to apply. In the latter case it is always possible to obtain P_{sig} based on G_{tot}.

The exact way the gains are spread across the receiver is out of the scope of the invention as it may be specific to every system. It should however take into account both the instantaneous P_{sig} gotten from the AGC command and the long-term estimate of the blocker power P_{blk}.

We remind here that the goal of the analog gain is to bring the signal into the right dynamic to be treated optimally by the ADC. If the gain is too high, the signal will saturate the ADC. On the contrary, if the gain is too small the conversion lacks precision as the dynamic of the ADC is underused.

The preceding steps aim at estimating the power of the blocker resulting in P_{blk}, even between the periods where it is present if it is an intermittent blocker. Therefore the analog gain should take into account the power of the useful signal P_{sig} if P_{sig} is significantly greater than P_{blk}. On the contrary, it should take into account P_{blk} if P_{blk} is significantly greater than P_{sig}. In between, one can choose either case according to the comparison of the difference between P_{sig} and P_{blk}.

Alternatively, a more sophisticated mechanism can be used to perform a more accurate comparison in linear scale, involving conversions from linear to dB scale and vice versa. Alternatively, a look-up table could be used to compute the total power in dB scale of the signal and the blocker based on a look-up table addressed by the difference $(P_{sig} - P_{blk})$. Finally, the digital gains are set to achieve the total gain G_{tot} once the analog gains have been determined.

This method results in the introduction of some latency to cope with change in the power of the blocker, which is fine in most cases. But, advantageously, a special care is taken to face the sudden raise, or apparition, of the power of the blocker. When a strong blocker appears or when the power of an existing blocker raises suddenly, there is a risk of ADC saturation if adjustment of the analog gain is not done fast enough.

Therefore a special mechanism may be advantageously added to ensure P_{blk} gets updated immediately if a powerful blocker appears suddenly while P_{blk} is low. This can be done by comparing the instantaneous blocker power P_k to the long-term estimate P_{blk}. If $P_k - P_{blk}$ becomes greater than a programmable threshold *THPBLK*

then P_{blk} must be updated immediately: $P_{blk} = P_k$. This event should also update P_{kmax}: $P_{kmax} = P_k$, and reset the N_k counter so that a new set of N_k values are used to obtain P_{kmax} afterwards; at the same time the internal state of the low-pass filter should be modified so that its subsequent outputs remain consistent with the new P_{blk} value.

CLAIMS

1/ A method for determining the gain distribution between the analog and the digital stages of a radio receiving device, said method causing the device to perform:

- estimating for each automated gain control period the instantaneous blocker power level, said device implementing an automated gain control mechanism to adjust the level of the received signal, the global gain to be applied being distributed between an analog stage and a digital one separated by an analog to digital converter, the gains being applied by automated gain control commands triggered regularly, the time between two consecutive automated gain control commands defining the automated gain control period;
- calculating the maximum of the estimated instantaneous blocker power level over a number of automated gain control periods to obtain a slow-varying value of the blocker power level;
- distributing the automated gain control command between the analog and the digital stage according to this slow-varying value of the blocker power level.

2/ The method according to claim 1, characterized in that it further causes the device to perform:

- smoothing the calculated maximum of the estimated instantaneous blocker power level over time by applying a low-pass filter.

3/ The method according to any one of claims 1 to 2, characterized in that the step of determining the distribution of the gain also comprises a step to enable an immediate decrease of the analog gain in case of a sudden detection of a blocker.

4/ The method according to any one of claims 1 to 3, characterized in that the instantaneous power level between two AGC commands is determined by:

- measuring on a sliding window successive elementary power measurements for each window slightly shifted in time;
- retaining the maximum value of these elementary power measurements over the AGC period as the instantaneous power level for this AGC period.

5/ The method according to claim 4, characterized in that the size of the sliding window is chosen according to the shortest expected power variation time frame.

6/ The method according to any one of claims 1 to 5, characterized in that the elementary power measurements are done by:

- calculating a difference value between a first power measurement before the digital filter and a second power measurement after the digital filter, both being expressed in dB scale;
- calculating the absolute signal power at the antenna by subtracting the total gain up to the measurement point;
- if the calculated difference value is greater than a given threshold, the elementary power measurement is set to the calculated absolute signal power at the antenna;
- if the calculated difference value is below the given threshold, the elementary power measurement is set to this calculated difference value.

7/ A computer program characterized in that it comprises program code instructions which can be loaded in a programmable device for causing the device to perform, when the program code instructions are run by the programmable device:

- estimating for each automated gain control period the instantaneous blocker power level, said device implementing an automated gain control mechanism to adjust the level of the received signal, the global gain to be applied being distributed between an analog stage and a digital one separated by an analog to digital converter, the gains being applied by automated gain control commands triggered regularly, the time between two consecutive automated gain control commands defining the automated gain control period;
- calculating the maximum of the estimated instantaneous blocker power level over a number of automated gain control periods to obtain a slow-varying value of the blocker power level;
- distributing the automated gain control command between the analog and the digital stage according to this slow-varying value of the blocker power level.

8/ The computer program according to claim 7, characterized in that it further causes the device to perform:

- smoothing the calculated maximum of the estimated instantaneous blocker power level over time by applying a low-pass filter.

9/ The computer program according to any one of claims 7 to 8, characterized in that the step of determining the distribution of the gain also comprises a step to enable an immediate decrease of the analog gain in case of a sudden detection of a blocker.

10/ The computer program according to any one of claims 7 to 9, characterized in that the instantaneous power level between two AGC commands is determined by:

- measuring on a sliding window successive elementary power measurements for each window slightly shifted in time;

- retaining the maximum value of these elementary power measurements over the AGC period as the instantaneous power level for this AGC period.

11/ The computer program according to claim 10, characterized in that the size of the sliding window is chosen according to the shortest expected power variation time frame.

12/ The computer program according to any one of claims 7 to 11, characterized in that the elementary power measurements are done by:

- calculating a difference value between a first power measurement before the digital filter and a second power measurement after the digital filter, both being expressed in dB scale;

- calculating the absolute signal power at the antenna by subtracting the total gain up to the measurement point;

- if the calculated difference value is greater than a given threshold, the elementary power measurement is set to the calculated absolute signal power at the antenna;

- if the calculated difference value is below the given threshold, the elementary power measurement is set to this calculated difference value.

13/ Information storage means, characterized in that they store a computer program comprising program code instructions which can be loaded in a

programmable device for implementing the method according to any one of claims 1 to 6, when the program code instructions are run by the programmable device.

14/ A device for determining the gain distribution between the analog and the digital stages of a radio receiving device, the device comprising circuitry causing the device to implement:

- means for estimating for each automated gain control period the instantaneous blocker power level, said device implementing an automated gain control mechanism to adjust the level of the received signal, the global gain to be applied being distributed between an analog stage and a digital one separated by an analog to digital converter, the gains being applied by automated gain control commands triggered regularly, the time between two consecutive automated gain control commands defining the automated gain control period;

- means for calculating the maximum of the estimated instantaneous blocker power level over a number of automated gain control period to obtain a slow-varying value of the blocker power level;

- means for distributing the automated gain control command between the analog and the digital stage according to this slow-varying value of the blocker power level.

15/ The device according to claim 14, characterized in that it further comprises circuitry causing the device to implement:

- means for smoothing the calculated maximum of the estimated instantaneous blocker power level over time by applying a low-pass filter.

16/ The device according to any one of claims 14 to 15, characterized in that the means for determining the distribution of the gain also comprise means for enabling an immediate decrease of the analog gain in case of a sudden detection of a blocker.

17/ The device according to any one of claims 14 to 16, characterized in that the instantaneous power level between two AGC commands is determined by:

- means for measuring on a sliding window successive elementary power measurements for each window slightly shifted in time ;

- means for retaining the maximum value of these elementary power measurements over the AGC period as the instantaneous power level for this AGC period.

18/ The device according to claim 17, characterized in that the size of the sliding window is chosen according to the shortest expected power variation time frame.

19/ The device according to any one of claims 14 to 18, characterized in that the means for measuring the elementary power measurements comprise:

- means for calculating a difference value between a first power measurement before the digital filter and a second power measurement after the digital filter, both being expressed in dB scale;
- means for calculating the absolute signal power at the antenna by subtracting the total gain up to the measurement point;
- means for setting the elementary power measurement value to the calculated absolute signal power at the antenna if the calculated difference value is greater than a given threshold;
- means for setting the elementary power measurement value to the calculated difference value if this calculated difference value is below the given threshold.

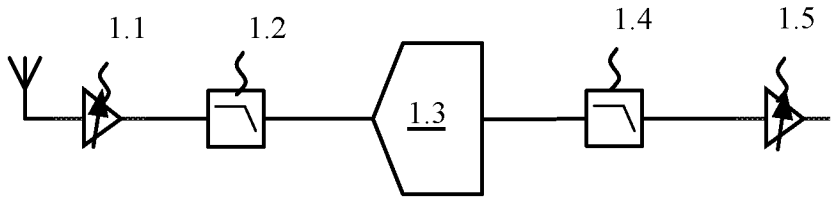


Fig. 1

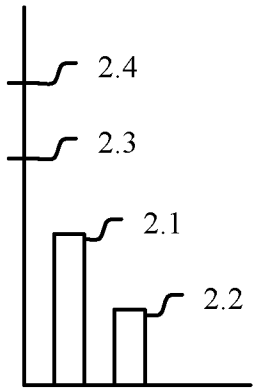


Fig. 2a

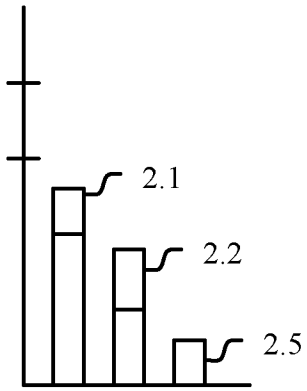


Fig. 2b

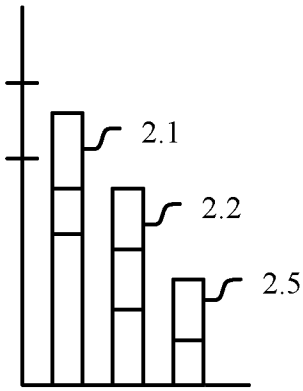


Fig. 2c

Fig. 2

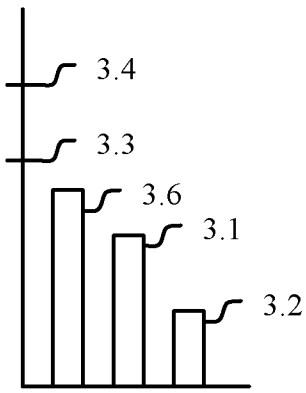


Fig. 3a

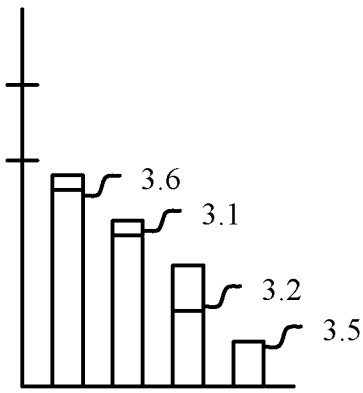


Fig. 3b

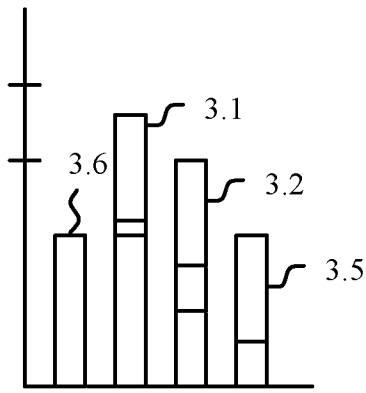


Fig. 3c

Fig. 3

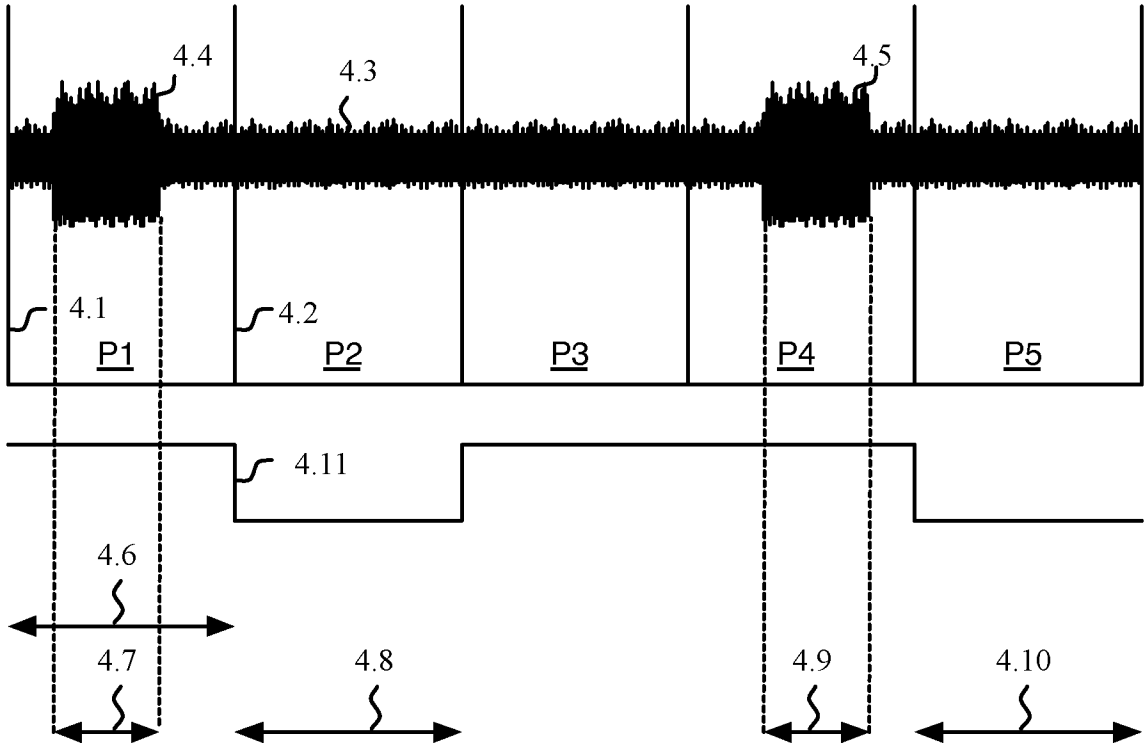

4.4
4.3
4.5
4.1
4.2
P1
P2
P3
P4
P5
4.11
4.6
4.7
4.8
4.9
4.10

Fig. 4

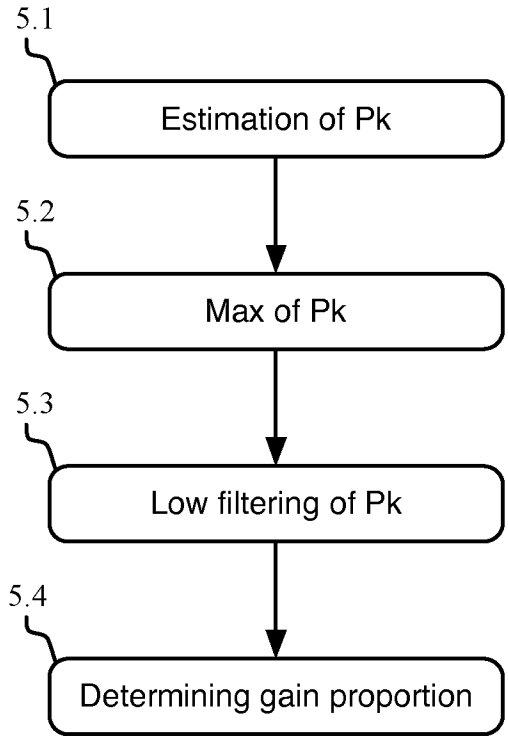

5.1
Estimation of Pk
5.2
Max of Pk
5.3
Low filtering of Pk
5.4
Determining gain proportion

Fig. 5

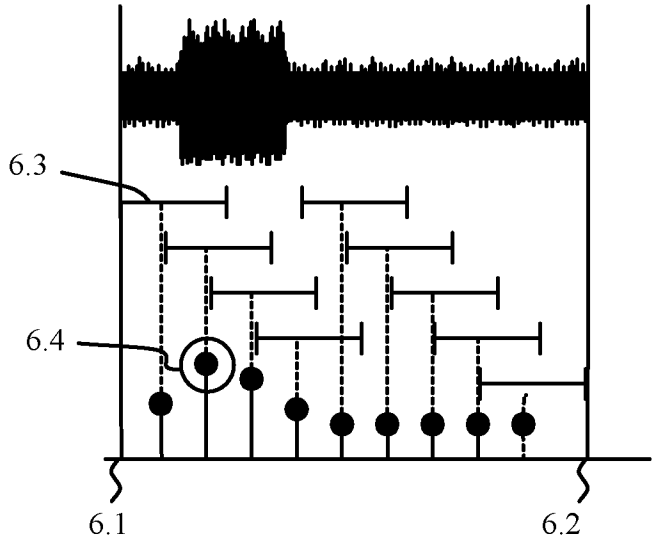


Fig. 6

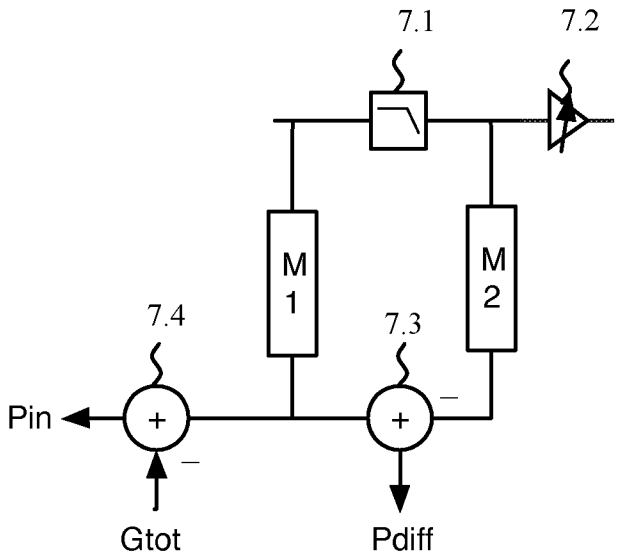


Fig. 7

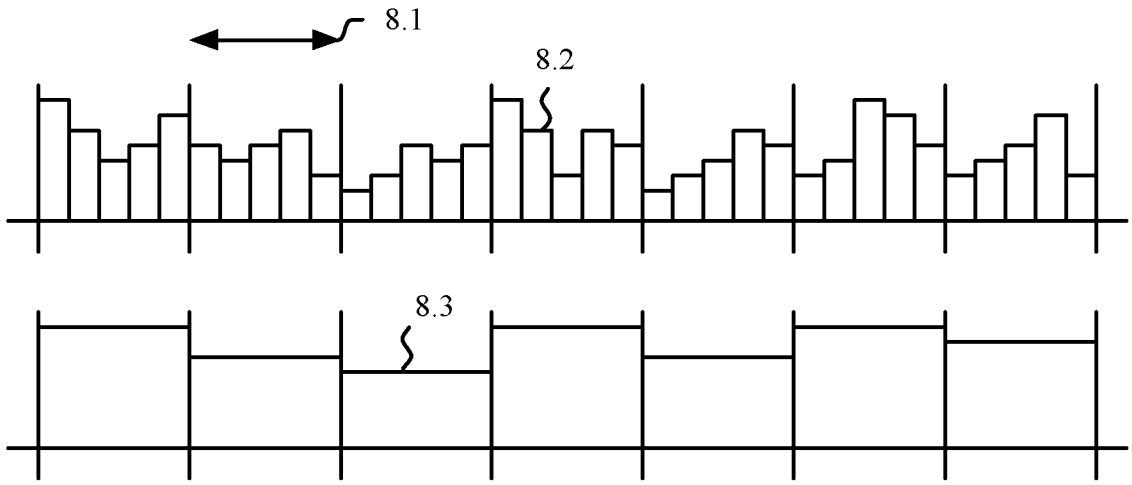


Fig. 8

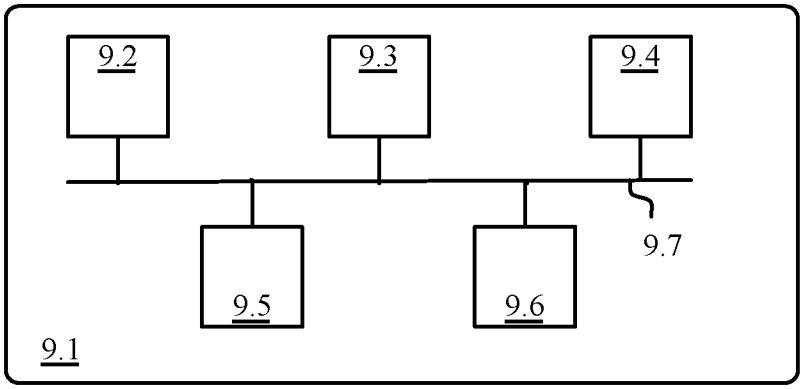


Fig. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/000757

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03G3/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/046679 A1 (KAJAKINE NIKOLAI [FI] ET AL) 25 February 2010 (2010-02-25) paragraphs [0002], [0020] - [0035], [0051] - [0108]; figure 4	1-19
X	US 2007/081615 A1 (KHOINI-POORFARD RAMIN [US] ET AL) 12 April 2007 (2007-04-12) paragraphs [0001], [0006] - [0008], [0016] - [0041]; figure 1	1-19
A	US 2011/235758 A1 (KHOINI-POORFARD RAMIN [US] ET AL) 29 September 2011 (2011-09-29) paragraphs [0002], [0017] - [0033]; figure 1	1-19

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 May 2012	06/06/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Goethals, Filip

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2012/000757

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010046679 A1	25-02-2010	GB 2458542 A	30-09-2009
		US 2010046679 A1	25-02-2010
US 2007081615 A1	12-04-2007	NONE	
US 2011235758 A1	29-09-2011	NONE	