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(71) **Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).**

(72) **Inventors:** **GRANT, John, M.**; 5812 Lomita Verde Circle, Austin, TX 78749 (US). **ADETUTU, Olubunmi, O.**; 12919 Partridge Bend, Austin, TX 78729 (US). **MUSGROVE, Yolanda, S.**; 903 West Noton Street, Pflugerville, TX 78660 (US).

(74) Agents: KOCH, William, E.; Motorola, Inc., Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 et al. (US).

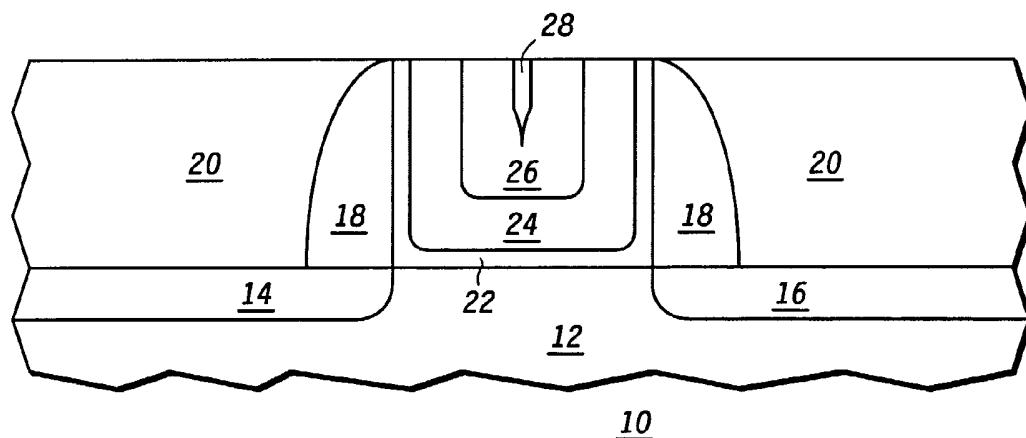
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(54) Title: TRANSISTOR METAL GATE STRUCTURE THAT MINIMIZES NON-PLANARITY EFFECTS AND METHOD OF FORMATION



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(57) Abstract: A metal gate structure (10) is formed by depositing a gate dielectric (22), a gate electrode (24), a stop layer (26), and a metal layer (28) within a gate trench (19) and removing the portions of the layers that lie outside the gate trench (19). A first polish or etch process is used to remove a portion of the metal layer (28) selective to the stop layer (26). A second polish or etch process is used to remove portions of the gate dielectric (22), the gate electrode (24), the stop layer (26) and the metal layer (28) which lie outside the gate trench (19) after the first polish or etch process. The resulting structure increases the uniformity and non-planarity of the top surface of the metal gate structure (10).

TRANSISTOR METAL GATE STRUCTURE THAT MINIMIZES NON-PLANARITY EFFECTS AND METHOD OF FORMATION

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Field of the Invention

The present invention is related to semiconductor devices and, more specifically, to a transistor metal gate structure that minimizes non-planarity effects.

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Background

As used herein, the term “high-k material” or “high dielectric constant material” refers to any material with a dielectric constant that is greater than silicon dioxide. The dielectric constant of silicon dioxide is approximately 3.9.

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As the industry moves to high dielectric constant materials due to electrical problems of using a thin silicon dioxide layer, using polysilicon as a gate electrode can result in the depletion of carriers in the polysilicon gate. To alleviate the polysilicon depletion problem, metal gate structures can be used.

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One method used to form transistor metal gate structures includes depositing metal layers within a gate trench, meaning a trench where a gate will subsequently be formed, and along the top surface of insulating materials surrounding the gate trench. An etch back or polishing process is used to remove the portions of the metal layers lying outside the gate trench.

When removing the metal layers using chemical mechanical polishing (CMP), dishing can occur across the semiconductor wafer and when using etch back the insulating materials around

the gate trench can erode. This results in non-functional devices, which decreases yield. Therefore, there is a need for a semiconductor process that minimizes non-planarity effects when removing the metal layers outside the gate trench.

Brief Description of the Drawings

The present invention is illustrated by way of example and
5 not limited by the accompanying figures, in which like references
indicate similar elements, and in which:

FIG. 1 illustrates a cross-sectional view of a semiconductor
device after removing the dummy gate in a replacement gate
integration in accordance with an embodiment of the present
10 invention;

FIG. 2 illustrates the semiconductor device in FIG. 1 after
depositing a gate dielectric and a gate electrode in accordance
with an embodiment of the present invention;

FIG. 3 illustrates the semiconductor device in FIG. 2 after
15 depositing a stop layer in accordance with an embodiment of the
present invention;

FIG. 4 illustrates the semiconductor device in FIG. 3 after
depositing a metal layer in accordance with an embodiment of the
present invention;

20 FIG. 5 illustrates the semiconductor device in FIG. 4 after
removing portions of the metal layer in accordance with an
embodiment of the present invention; and

FIG. 6 illustrates the semiconductor device in FIG. 5 after
removing portions of the metal layer, the stop layer, the gate
25 electrode layer and the gate dielectric in accordance with an
embodiment of the present invention.

Skilled artisans appreciate that elements in the figures are
illustrated for simplicity and clarity and have not necessarily been

drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description of the Drawings

A control electrode dielectric layer is formed adjoining all surfaces of a control electrode trench and extending beyond the 5 control electrode trench. A control electrode layer is formed adjoining the control electrode dielectric layer in the control electrode trench. A stop layer is formed within the control electrode trench over the control electrode dielectric layer. Both the control electrode layer and the stop layer fill less than all of the 10 control electrode trench. A conductive layer is formed adjoining all exposed surfaces of the stop layer and extending beyond the gate trench and substantially filling all the remaining volume of the control electrode trench. The control electrode dielectric layer, the control electrode layer, the stop layer and the conductive layer 15 form a control electrode stack overlying a channel area in a substrate and having a lateral dimension and a height defining the control electrode trench that is determined by a sidewall spacer.

Portions of the conductive layer above the stop layer are removed using the stop layer to substantially retard the removing. 20 The stop layer is a conductive material that has a slower removal rate than the overlying materials during removal of the overlying materials. All portions of the conductive layer, the stop layer, the control electrode layer, and the control electrode dielectric above a predetermined height are also removed. The invention is better 25 understood by turning to the figures and is defined by the claims.

FIG. 1 illustrates a cross-section of a semiconductor device or integrated circuit 10 including a semiconductor substrate 12, a source region 14, a drain region 16, sidewall spacers 18 and an

interlevel dielectric layer (ILD) 20 after removing a dummy gate stack to form a gate trench 19 in a replacement gate integration, as known to a skilled artisan. The semiconductor substrate 12 can be any semiconductor material such as silicon, gallium arsenide, 5 silicon germanium and the like. In addition the semiconductor substrate 12 can be the silicon layer of a silicon-on-insulator (SOI) substrate. The source region 14 and the drain region 16 are doped a conductivity that is opposite that of the semiconductor substrate 12, if doped, and are separated from each other to 10 define a channel area in the semiconductor substrate 12. The sidewall spacers 18 are insulating and, preferably, include a nitride or oxide material. In one embodiment, the sidewall spacers 18 are a stack of insulating materials. The ILD layer 20 is an insulating material, such as silicon dioxide, and can also include a stack of 15 insulating materials. The ILD layer 20 adjoins an outer perimeter of the sidewall spacers and will insulate the subsequently formed transistor structure.

As shown in FIG. 2, a gate dielectric or control electrode dielectric 22 and a gate electrode 24 are formed in the gate trench 19 and along the upper surface of the ILD LAYER 20 by CVD (chemical vapor deposition), PVD (physical vapor deposition), ALD (atomic layer deposition), MBE (molecular beam epitaxy), plating, combinations of the above or the like. However, it is not necessary that the gate dielectric layer 22 and the gate electrode 24 be 25 formed by the same process. The gate dielectric layer 22 can be any dielectric material, such as silicon dioxide, a high-k material, a metal-oxy-nitride, a metal oxide, a metal silicate, or a metal aluminate. For example, the gate dielectric layer 22 can be silicon

nitride, silicon dioxide, HfO_2 , ZrO_2 , HfSi_xO_y , SiO_xN_y , and the like.

Typically, the gate dielectric layer 22 is approximately 10 Angstroms to 60 Angstroms.

The gate electrode or current electrode 24 can be a metal 5 nitride (such as TiN, TaN, TiSiN, TaSiN), a conductive metal oxide (such as IrO, RuO, or a metal aluminum nitride (such as $\text{Ti}_x\text{Al}_y\text{N}_z$), a metal silicide, a metal-silicon-nitride, or any other material that has a suitable work function. A suitable work function is a material 10 property that determines the desired threshold voltage value for the transistor. In one embodiment, the gate electrode 24 will be a thickness that is less than half of the gate length of the transistor and greater than 10 Angstroms.

After forming the gate dielectric layer 22 and the gate electrode 24, a stop layer 26 is formed, by CVD, PVD, ALD, MBE, 15 plating, the like, or combinations of the above, as shown in FIG. 3. The stop layer 26 is conductive and can be a pure metal (such as Ti, Ta, Ag, Au, Ir or Ru), a metal silicide (such as cobalt silicide or titanium silicide), or silicon. The stop layer 26 can serve as an etch stop layer and/or a polish stop layer for the subsequently 20 formed overlying layers. The stop layer 26 can be a polish stop layer for a chemical mechanical polish (CMP) or a physical mechanical polish of the overlying materials. In an embodiment where the stop layer 26 is a polish stop layer, a thickness of 50 Angstroms has shown to be sufficient using conventional CMP 25 equipment. When serving as an etch stop layer, the stop layer 26 can be a stop layer for a chemical etch back of the overlying materials

As shown in FIG. 4, after forming the stop layer 26, a conductive layer 28 is formed over the semiconductor device 10 by CVD, PVD, ALD, MBE, plating, the like or combinations of the above. The conductive layer 28 is a conductive material with a low 5 resistivity and can be a metal (such as W, Al, Au, Cu, Ag, Pt), a metal silicide or silicon, the like, or combinations of metals. The conductive layer 28 should be able to be polished or etched selectively to the stop layer 26 material. The conductive layer 28 is thicker than the sum total of the thicknesses of the stop layer 26, 10 the gate electrode layer 24 and the gate dielectric layer 22.

Therefore, the stop layer 26, the gate electrode layer 24, and the gate dielectric layer 22 are thinner than the conductive layer 28. In one embodiment, the thickness of the conductive layer 28 is approximately twice the depth of the gate trench 19.

15 After forming the conductive layer 28, a portion of the conductive layer 28 is polished or etched until the stop layer 26 is exposed as shown in FIG. 5. This is performed by using a process that is selective to the material chosen for the stop layer 26. For example, if the conductive layer 28 is tungsten and the stop layer 20 26 is titanium a CMP chemistry using FeNO_3 can be used. The chemistry used to remove materials suitable for the conductive layer 28 tends to not be selective to metal nitrides or other gate electrode type materials, however, the chemistry is selective to materials disclosed for the stop layer 26.

25 Shown in FIG. 6, after removing the portion of the conductive layer 28 that lies over the etch stop layer 28, a different polish or etch process is performed to remove the stop layer 26, the gate electrode layer 24 and the gate dielectric layer 22. The ILD

LAYER 20 will serve as a second stop material for the selective layer removal of overlying materials. For example, if the conductive layer 28 is removed by CMP, the semiconductor device 10 can be switched to a different platen in the CMP tool with a

5 different slurry and pad to remove the stop layer 26, the gate electrode layer 24 and the gate dielectric layer 22 selective to the ILD LAYER 20. For example, a chemistry using ammonium hydroxide can be used to CMP the three layers 26, 24, and 22. However, it is not necessary that the stop layer 26, the gate

10 electrode layer 24 and the gate dielectric layer 22 be removed using the same chemistry or during the same process step. Therefore, more than one process chemistry and step can be performed to remove the layers 26, 24 and 22.

The resulting structure after removing the portions of the

15 gate electrode stack or control electrode stack - which includes the conductive layer 28, the stop layer 26, the gate electrode layer 24, and the gate dielectric layer 22 - that are over the ILD LAYER 20 is a transistor metal gate structure with a minimum dishing or recessing of the gate or control electrode stack. The dishing of the

20 ILD LAYER 20 is also minimized in other areas of the semiconductor substrate 12 (not shown). Advantageously, yield is increased due to the decrease in dishing. The presence of the stop layer 26 allows for at least a two-step polish or etch process to be performed. Since it is generally more difficult to polish or

25 etch a thicker layer than a thinner layer with good uniformity across a die or a wafer, the ability to remove the thicker layer selective to underlying thinner layers by stopping on a stop layer and

subsequently removing the thinner layers using a separate process increases planarity control.

Another advantage of the invention is that it allows for the selection of the gate electrode material independently of its 5 polishing or etching characteristics. Therefore, the present invention provides for a wider range of choices for the gate electrode material than if the stop layer 26 is not used.

After forming a transistor metal gate with minimized non-planarity, traditional additional processing (not shown) known to 10 one skilled in the art is performed. For example, a second ILD material is deposited over the structure shown in FIG. 6 and metal interconnects are subsequently formed.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one 15 of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, additional layers may be incorporated into the gate electrode stack, such as diffusion or barrier layers. Accordingly, the 20 specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have 25 been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the

claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements

5 but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A transistor structure (10) comprising:
 - 5 a substrate (12) having first (14) and second (16) current electrodes formed therein and separated to define a channel area in the substrate;
 - 10 a control electrode stack overlying the channel area in the substrate, the control electrode stack having a lateral dimension determined by a sidewall spacer (18) and having a height to define a control electrode trench, the control electrode stack further comprising:
 - 15 a control electrode dielectric (22) directly adjoining the sidewall spacer (18) and a region above the channel area, the control electrode dielectric filling a first portion of the control electrode trench;
 - 20 a control electrode layer (24) directly adjoining the control electrode dielectric, the control electrode layer filling a second portion of the control electrode trench and having a material property that determines a threshold voltage value of the transistor structure;
 - 25 a conductive stop layer (26) directly adjoining the control electrode layer, the conductive stop layer filling a third portion of the control

electrode trench and providing a stop material that is used for selective layer removal of overlying materials during formation of the transistor structure; and

5 a conductive layer (28) directly adjoining the conductive stop layer, the conductive layer filling a fourth portion of the control electrode trench, the first portion, second portion, third portion and fourth portion substantially filling the control electrode

10 trench.

2. The transistor structure of claim 1 wherein the conductive stop layer (26) is a polish stop layer for a chemical mechanical

15 polish of the overlying materials.

3. The transistor structure of claim 1 wherein the conductive stop layer (26) is a polish stop layer for a physical mechanical polish of the overlying materials.

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4. The transistor structure of claim 1 wherein the conductive stop layer (26) is an etch stop layer for chemical etch back of the overlying materials.

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5. The transistor structure of claim 1 wherein the control electrode dielectric (22) comprises one of a material selected from a group consisting of silicon dioxide, silicon-oxy-nitride, silicon

nitride, metal silicates, metal aluminates, metal oxides and metal-oxy-nitrides.

6. The transistor structure of claim 1 wherein the conductive stop layer (26) comprises a conductive material that has a slower removal rate than the overlying materials during removal of the overlying materials.
7. A method for providing a transistor (10), comprising:
 - 10 providing a substrate (12);
forming first (14) and second (16) current electrodes in the substrate, the first and second current electrodes being separated to define a channel area in the substrate;
 - 15 forming a control electrode trench that determines location of a control electrode; and
forming a control electrode stack within the control electrode trench, the forming of the control electrode stack further comprising:
 - 20 forming a control electrode dielectric (22) within and beyond the control electrode trench and directly adjoining walls of the control electrode trench, the control electrode dielectric filling a first portion of the control electrode trench;
 - 25 forming a control electrode layer (24) directly adjoining the control electrode dielectric, the control electrode layer filling a second

portion of the control electrode trench and having a material property that determines a threshold voltage value of the transistor; forming a conductive stop layer (26) directly adjoining the control electrode layer, the conductive stop layer filling a third portion of the control electrode trench and providing a stop material that is used for selective layer removal of overlying materials during formation of the transistor; forming a conductive layer (28) directly adjoining the conductive stop layer, the conductive layer filling a fourth portion of the control electrode trench, the first portion, second portion, third portion and fourth portion substantially filling the control electrode trench opening; removing a first initial part (above the top surface of 26) of the conductive layer to form a first upper surface by using the conductive stop layer to stop the removing; and removing a second initial part (above the top surface of 20) of the conductive layer and part of the conductive stop layer, the control electrode layer and the control electrode dielectric to form a control electrode stack of the transistor that has a substantially planar upper surface.

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8. The method of claim 7 further comprising:

5 forming an interlevel dielectric (20) adjoining an outer perimeter of the control electrode trench, the interlevel dielectric electrically insulating the transistor; and

10 using the interlevel dielectric as a second stop material to remove the second initial part of the conductive layer and part of the conductive stop layer, the control electrode layer and the control electrode dielectric.

9. The method of claim 7 further comprising:

15 forming the conductive stop layer (26) with a conductive material that has a slower removal rate than the overlying materials during removal of the first initial part of the conductive layer.

20 10. A method of forming within a gate trench a metal gate structure (10) that minimizes non-planarity effects comprising:

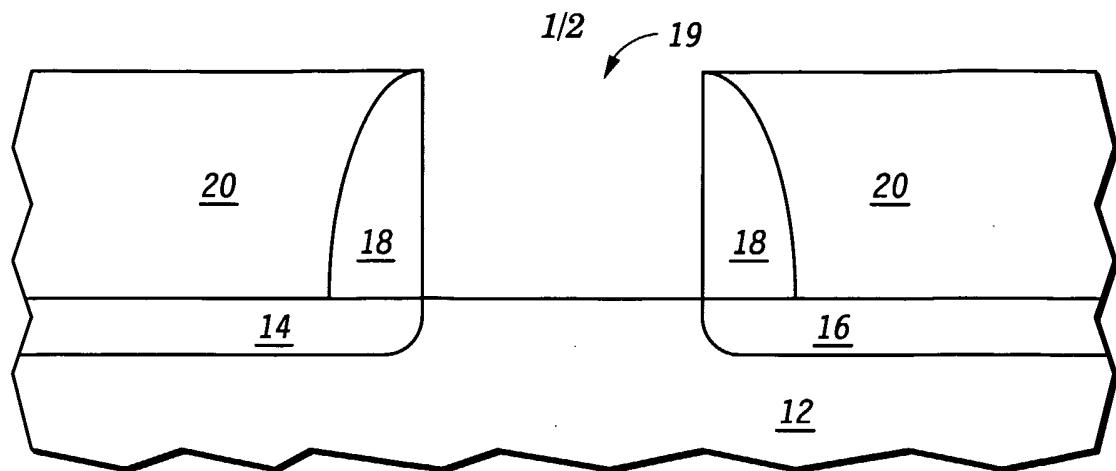
25 forming a gate dielectric (22) adjoining all surfaces of the gate trench and extending beyond the gate trench; forming a gate electrode layer (24) of a first metal adjoining the gate dielectric and extending beyond the gate trench, the gate electrode layer filling less than all of the gate trench;

forming a stop layer (26) adjoining all exposed surfaces of the gate electrode layer and extending beyond the gate trench, the stop layer also filling less than all of the gate trench;

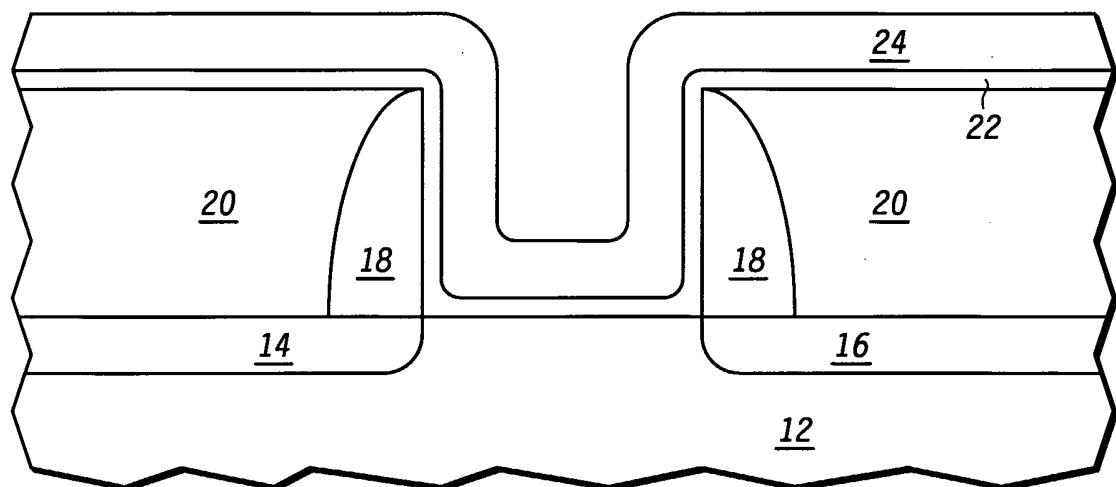
5 forming a conductive layer (28) of a second metal adjoining all exposed surfaces of the stop layer and extending beyond the gate trench, the conductive layer substantially filling the gate trench;

10 removing all portions of the conductive layer (28) above the stop layer (26) by using the stop layer to substantially retard the removing; and removing all portions of the conductive layer (28), the stop layer (26), the gate electrode layer (24) and the gate dielectric (22) above a predetermined height (the height of the sidewall spacer).

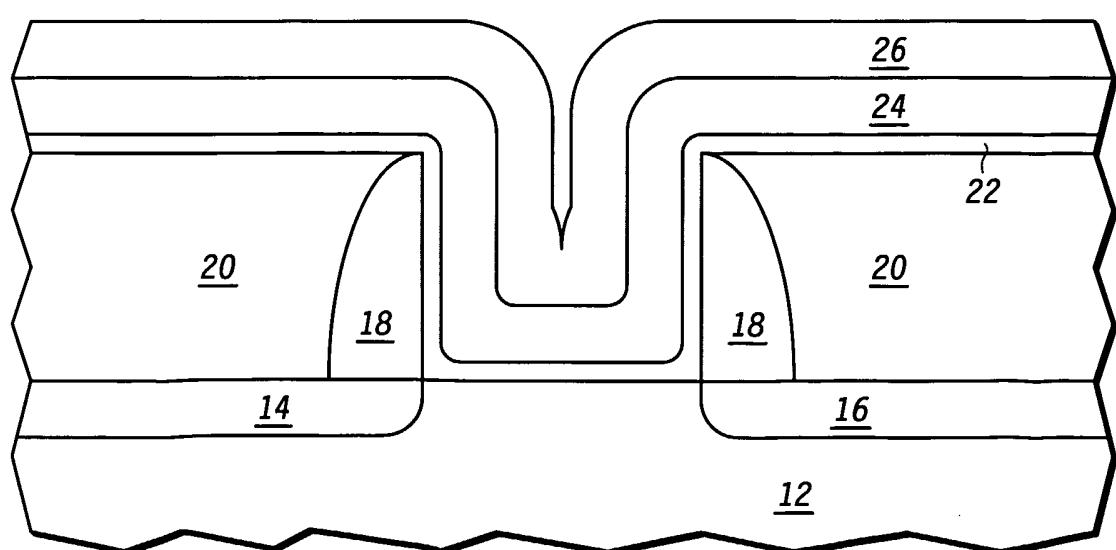
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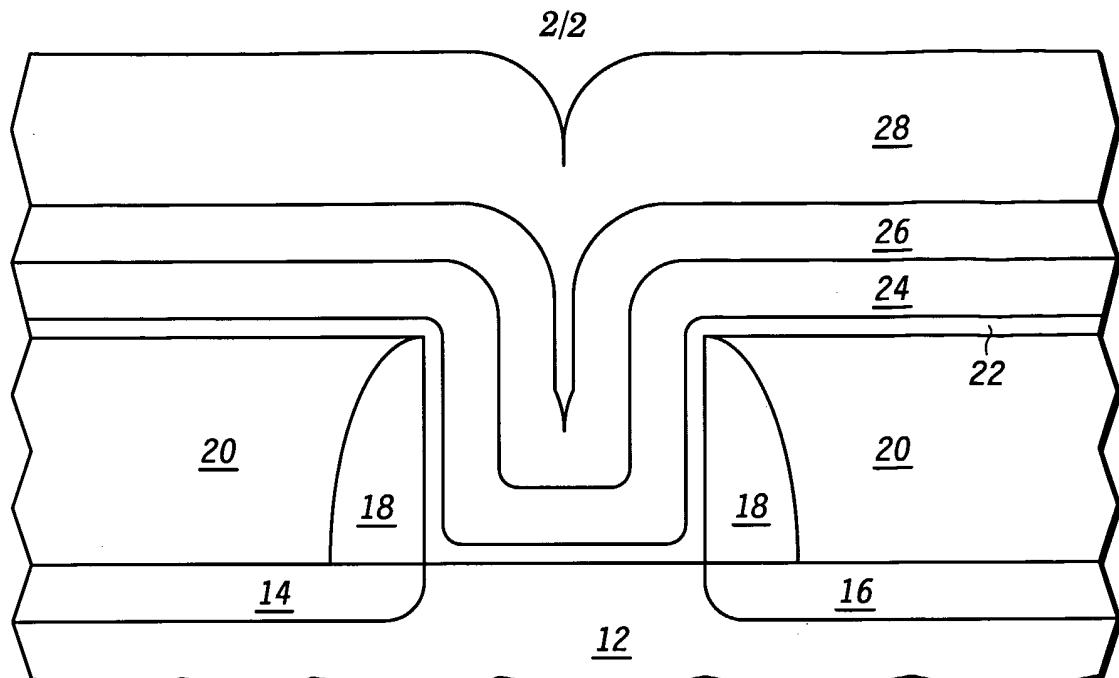


FIG. 4 10

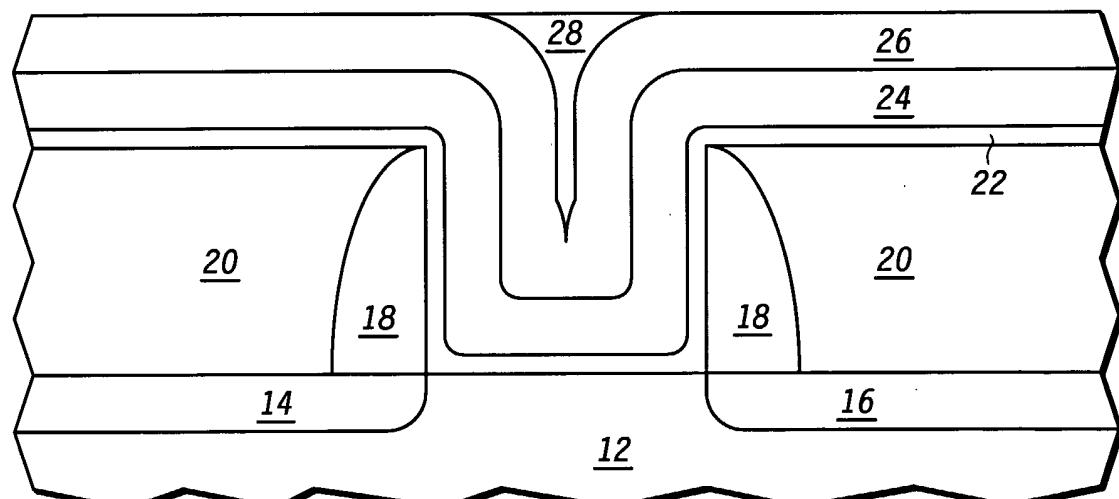


FIG. 5 10

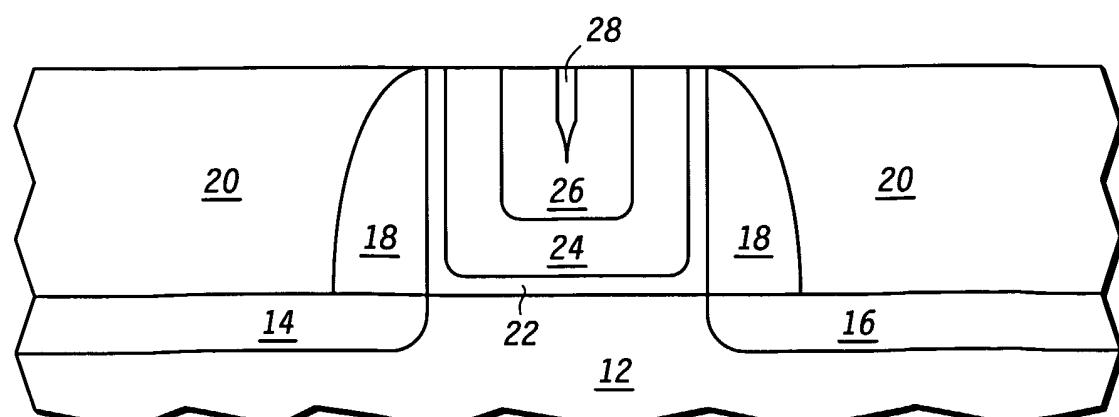


FIG. 6 10