(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 March 2015 (05.03.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/030787 A1

(51) International Patent Classification:
H01L 21/336 (2006.01)

(21) International Application Number:
PCT/US2013/057482

(22) International Filing Date:
30 August 2013 (30.08.2013)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** [US/US]; Hewlett-Packard Company, 11445 Compaq Center Drive W., Houston, Texas 77070 (US).

(72) Inventors: **GE, Ning**; Depot Road Plant 1150 Depot Rd, Singapore 109673 (SG). **CHIA, Leong Yap**; Depot Road Plant 1150 Depot Rd, Singapore 109673 (SG). **LEE, Pin Chin**; Depot Road Plant 1150 Depot Rd, Singapore 109673 (SG). **RANDO, Jose Jehrome**; 8 Venlo Court, Salisbury Downs, South Australia 5108 (AU).

(74) Agents: **BRUSH, Robert M** et al.; Hewlett-Packard Company, IP Administration - MS35, 3404 E. Harmony Road, Fort Collins, Colorado 80528 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME

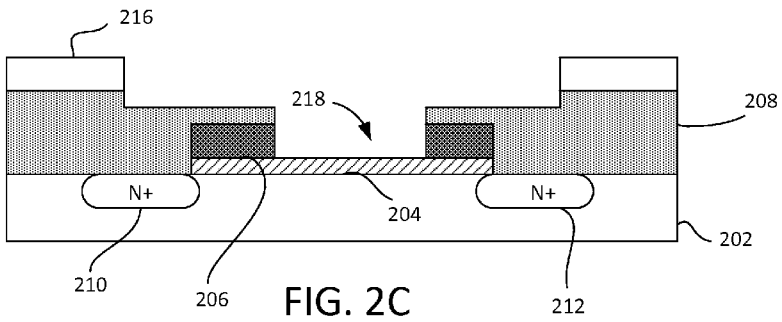


FIG. 2C

(57) Abstract: A semiconductor device and method of forming the same is described. In an example, a polysilicon layer is deposited on a substrate having at least one polysilicon ring. The substrate is doped using the polysilicon layer as a mask to form doped regions in the substrate. A dielectric layer is deposited over the polysilicon layer and the substrate. The dielectric layer is etched to expose portions of the polysilicon layer. A metal layer is deposited on the dielectric layer. The metal layer, the dielectric layer, and the exposed portions of the polysilicon layer are etched such that at least a portion of each polysilicon ring is removed.

WO 2015/030787 A1

SEMICONDUCTOR DEVICE AND METHOD OF MAKING SAME

Background

[0001] Inkjet technology is widely used for precisely and rapidly dispensing small quantities of fluid. Inkjets eject droplets of fluid out of a nozzle by creating a short pulse of high pressure within a firing chamber. During printing, this ejection process can repeat thousands of times per second. Inkjet printing devices are implemented using semiconductor devices, such as thermal inkjet (TIJ) devices or piezoelectric inkjet (PIJ) devices. For example, a TIJ device is a semiconductor device including a heating element (e.g., resistor) in the firing chamber along with other integrated circuitry. To eject a droplet, an electrical current is passed through the heating element. As the heating element generates heat, a small portion of the fluid within the firing chamber is vaporized. The vapor rapidly expands, forcing a small droplet out of the firing chamber and nozzle. The electrical current is then turned off and the heating element cools. The vapor bubble rapidly collapses, drawing more fluid into the firing chamber.

Brief Description Of The Drawings

[0002] Some embodiments of the invention are described with respect to the following figures:

Fig. 1 is a block diagram of an ink jet printer according to an example implementation.

Figs. 2A through 2C illustrate cross-sections of a semiconductor device according to an example implementation.

Figs. 3A and 3B show a top view and cross-section view respectively of a semiconductor device according to an example implementation prior to partial gate etching.

Figs. 4A and 4B show a top view and cross-section view respectively of a semiconductor device according to an example implementation after partial gate etching.

Fig. 5A is a schematic showing a circuit of transistors according to an example implementation.

Fig. 5B is a top view of the circuit of Fig. 5 as formed on a substrate prior to partial gate etching according to an example implementation.

Fig. 6 is a flow diagram of a method of forming a semiconductor device according to an example implementation.

Fig. 7 is a flow diagram of a method of forming transistors in a substrate according to an example implementation.

Detailed Description

[0003] Fig. 1 is a block diagram of an ink jet printer 102 according to an example implementation. The ink jet printer 102 includes a print controller 106 and a printhead 108. The print controller 106 is coupled to the printhead 108. The print controller 106 receives printing data representing an image to be printed to media (media not shown for clarity). The print controller 106 generates signals for activating drop ejectors on the printhead 108 to eject ink onto the media and produce the image. The print controller 106 provides the signals to the printhead 108 based on the printing data.

[0004] The print controller 106 includes a processor 120, a memory 122, input/output (IO) circuits 116, and various support circuits 118. The processor 120 can include any type of microprocessor known in the art. The support circuits 118 can include cache, power supplies, clock circuits, data registers, and the like. The memory 122 can include random access memory, read only

memory, cache memory, magnetic read/write memory, or the like or any combination of such memory devices. The IO circuits 116 can by coupled to the printhead 108. The IO circuits 116 can also be coupled to external devices, such as a computer 104. For example, the IO circuits 116 can receive printing data from an external device (e.g., the computer 104), and provide signals to the printhead 108 using the IO circuits 116.

[0005] The printhead 108 includes a plurality of drop ejectors 110 and associated integrated circuitry 111. The drop ejectors 110 are in fluidic communication with an ink supply (not shown) for receiving ink. For example, ink can be provided from a container. In an example, the printhead 108 is a thermal ink jet (TIJ) device. The drop ejectors 110 generally include a heating element, a firing chamber, and a nozzle. Ink from the ink supply fills the firing chambers. To eject a droplet, an electrical current generated by the circuits 111 is passed through the heater element placed adjacent to the firing chamber. The heating element generated heat, which vaporizes a small portion of the fluid within the firing chamber. The vapor rapidly expands, forcing a small droplet out of the firing chamber and nozzle. The electrical current is then turned off and the resistor cools. The vapor bubble rapidly collapses, drawing more fluid into the firing chamber from the ink supply.

[0006] The circuits 111 include various circuit elements and conductors formed as part of an integrated circuitry on the printhead 108. In particular, the circuits 111 include transistors 112 used for various purposes, such as providing signals to the drop ejectors or implementing higher-level circuits, such as logic gates, shift registers, address generators, multiplexers/demultiplexers, on-chip memory, and the like. In some circuits, multiple transistors are laid out in proximity to one another (e.g., a cascade arrangement of transistors). In a standard complementary metal oxide semiconductor (CMOS) process, transistors are isolated from one another using a field oxide (FOX), shallow trench isolation (STI), deep trench isolation (DTI), or the like. Some printheads, however, are manufactured using a no-field oxide process for cost reduction.

Since there is no field oxide (or similar feature) isolating individual transistors, the transistors must be laid out with an enclosed gate structure.

[0007] For example, in an N-type metal oxide semiconductor (NMOS) no-field oxide process, a gate is formed as a ring on a semiconductor substrate. An inner doped region is formed in the substrate inside the ring and an outer doped region is formed outside the ring separated from the inner doped region by a channel. The inner and outer doped regions act as drain and source of the transistor. If two or more transistors are cascaded and share a common source/drain, additional gate ring(s) must be concentrically arranged on the substrate. This transistor layout is not efficient in terms of area as compared to industry CMOS design having FOX or the like. Further, layout becomes more complicated, requires more semiconductor area, and increases cost. Examples discussed below improve the efficiency of transistor layout in a no-field oxide process by forming transistors using a partially etched gate NMOS transistor process, which requires less semiconductor area for higher packing density and for reduces manufacturing cost. Also, due to the smaller size capacitance, the resulting device exhibits increase electrical speed.

[0008] Figs. 2A through 2C illustrate cross-sections of a semiconductor device according to an example implementation. The cross-sections show the device after different steps of a NMOS transistor process. As shown in Fig. 2A, the device includes a substrate 202 having a gate oxide (GOX) 204 deposited thereon. A polysilicon layer 206 is deposited on the GOX layer 204. The polysilicon layer 206 acts as a hard mask to produce N+ doped regions 210 and 212 in the substrate 202 and the polysilicon layer 206 will be in-situ doped for lower resistance. A dielectric layer 208 is deposited over the polysilicon layer 206. The dielectric layer 208 can be any type of insulator material, such as phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG).

[0009] As shown in step Fig. 2B, the dielectric layer 208 is masked using a photolithographic technique, such as use of a contact mask, and etched to produce an exposed portion 214 of the polysilicon layer 206. The etch can be

designed to stop at the polysilicon layer 206 using etch control and selectivity techniques.

[0010] As shown in Fig. 2C, a metal layer 216 is deposited on the dielectric layer using a mask that covers at least the exposed portion 214 of the polysilicon layer 206. Thus, no metal is deposited on the exposed portion 214 of the polysilicon layer 206. The metal layer 216 is etched to form a conductor pattern. The etching process of the metal layer 216 will also remove the exposed portion 214 of the polysilicon layer 206 and some of the dielectric layer 208 to produce a break 218 in the polysilicon layer 206. This general process, referred to as a partially etched gate NMOS transistor process, can be used to remove unwanted gate portions after doping, as discussed below.

[0011] Figs. 3A and 3B show a top view and cross-section view respectively of a semiconductor device according to an example implementation. The semiconductor device includes a substrate 308 having a GOX layer 310 deposited thereon. A polysilicon layer is formed on the GOX layer 310 having a polysilicon ring 302. The polysilicon ring 302 has a section 302A and a section 302B. Doped regions 304 and 306 are formed in the substrate 308 to provide drain and source for a transistor. In particular, the doped region 306 includes a section 306A and 306B. After the doped regions 304 and 306 are formed, the section 302B can be removed using the process partial-etch process described above in Fig. 2. The resulting transistor structure is shown in Figs. 4A and 4B.

[0012] As shown in Fig. 4, the section 302B is removed. A transistor is formed from the doped region 306A, the section 302A of polysilicon, and the doped region 304 (e.g., source, gate, and drain, respectively). The doped region 304 is isolated from the doped region 306B because the section 302B of polysilicon has been removed (i.e., there is no gate spanning the channel between doped region 304 and doped region 306B). Thus, the gate ring 302 is used to form the doped regions for the transistor (source and drain) and the unwanted portion (e.g., the section 302B) of the polysilicon ring is removed thereafter using the partial-etch process described above. Thus, transistor

layouts can be provided to conserve silicon area and cost. When two or more transistors are cascaded, there is no need to build a ring in ring design, as shown below.

[0013] Fig. 5A is a schematic showing a circuit 500 of transistors according to an example implementation. The circuit 500 includes three transistors Q1, Q2, and Q3 in a cascade arrangement. Fig. 5B is a top view of the circuit 500 as formed on a substrate prior to partial gate etching according to an example implementation. The layout includes polysilicon gate segments 502 and doped regions 506. A polysilicon ring 504, used when forming the doped regions 506, is removed using the partial etching process described above. In this manner, a ring-in-ring structure is not required to produce a layout of cascaded transistors, saving silicon area and cost.

[0014] Fig. 6 is a flow diagram of a method 600 of forming a semiconductor device according to an example implementation. The method 600 begins at step 602, where a polysilicon layer is deposited on a substrate having at least one polysilicon ring. At 604, the substrate is doped using the polysilicon layer as a mask to form doped regions in the substrate. At step 606, a dielectric layer is deposited over the polysilicon layer and the substrate. At step 608, the dielectric layer is etched to expose portions of the polysilicon layer. At step 610, a metal layer is deposited over the dielectric layer. In examples, the metal layer is not deposited over at least the exposed portions of the polysilicon layer. At step 612, the metal layer, dielectric layer, and the exposed portions of the polysilicon layer such that at least a portion of the polysilicon ring is removed.

[0015] Fig. 7 is a flow diagram of a method 700 of forming transistors in a substrate according to an example implementation. The method 700 begins at step 702, where a gate layer is formed on the substrate having at least one gate ring. At step 704, the substrate is doped to form source and drain regions. At step 706, a dielectric layer is formed over the gate layer and the substrate. At step 708, the dielectric layer is etched to expose portions of the gate layer. At step 710, a metal layer is deposited on the dielectric layer. In examples, the

metal layer is not deposited over at least the exposed gate portions. At step 712, the metal layer, dielectric layer, and the exposed gate portions are etched such that at least a portion of the gate ring is removed.

[0016] In the foregoing description, numerous details are set forth to provide an understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these details. While the invention has been disclosed with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the invention.

What is claimed is:

1. A method of forming a semiconductor device, comprising:

depositing a polysilicon layer on a substrate having at least one polysilicon ring;

doping the substrate using the polysilicon layer as a mask to form doped regions in the substrate;

depositing a dielectric layer over the polysilicon layer and the substrate;

etching the dielectric layer to expose portions of the polysilicon layer;

depositing a metal layer on the dielectric layer; and

etching the metal layer, the dielectric layer, and the exposed portions of the polysilicon layer such that at least a portion of each polysilicon ring is removed.

2. The method of claim 1, wherein the at least one polysilicon ring includes a first polysilicon ring, and wherein the step of doping includes forming a first doped region surrounded by a second doped region and spaced apart from the second doped region.

3. The method of claim 2, wherein after the step of etching, the first polysilicon ring spans only a portion of space between the first doped region and the second doped region.

4. The method of claim 1, wherein the substrate is a P-type substrate and the doped regions are N+ doped regions.

5. A method of forming transistors in a substrate, comprising:

forming a gate layer having at least one gate ring on the substrate;

doping the substrate to form doped source and drain regions in the substrate;

forming a dielectric layer over the gate layer and the substrate;

etching the dielectric layer to expose portions of the gate layer;

depositing a metal layer on the dielectric layer; and

etching the metal layer, the dielectric layer, and the exposed portions of the gate layer such that at least a portion of each gate ring is removed.

6. The method of claim 5, wherein the at least one gate ring includes a first gate ring, and wherein the step of doping includes forming a drain region surrounded by a source region with a channel therebetween.

7. The method of claim 6, wherein after the step of etching, the first gate ring spans only a portion of the channel between the source and the drain regions.

8. The method of claim 5, wherein the substrate is a P-type substrate and the source and drain regions are N+ doped regions.

9. A semiconductor device, comprising:

a substrate;

a drain region formed in the substrate;

a source region formed around the drain region with a channel therebetween formed using a gate ring on the substrate as a mask; and

a gate formed over only a portion of the channel, the gate being a portion of the gate ring.

10. The semiconductor device of claim 9, wherein the substrate is P-type substrate and the source and drain regions are N+ doped regions.

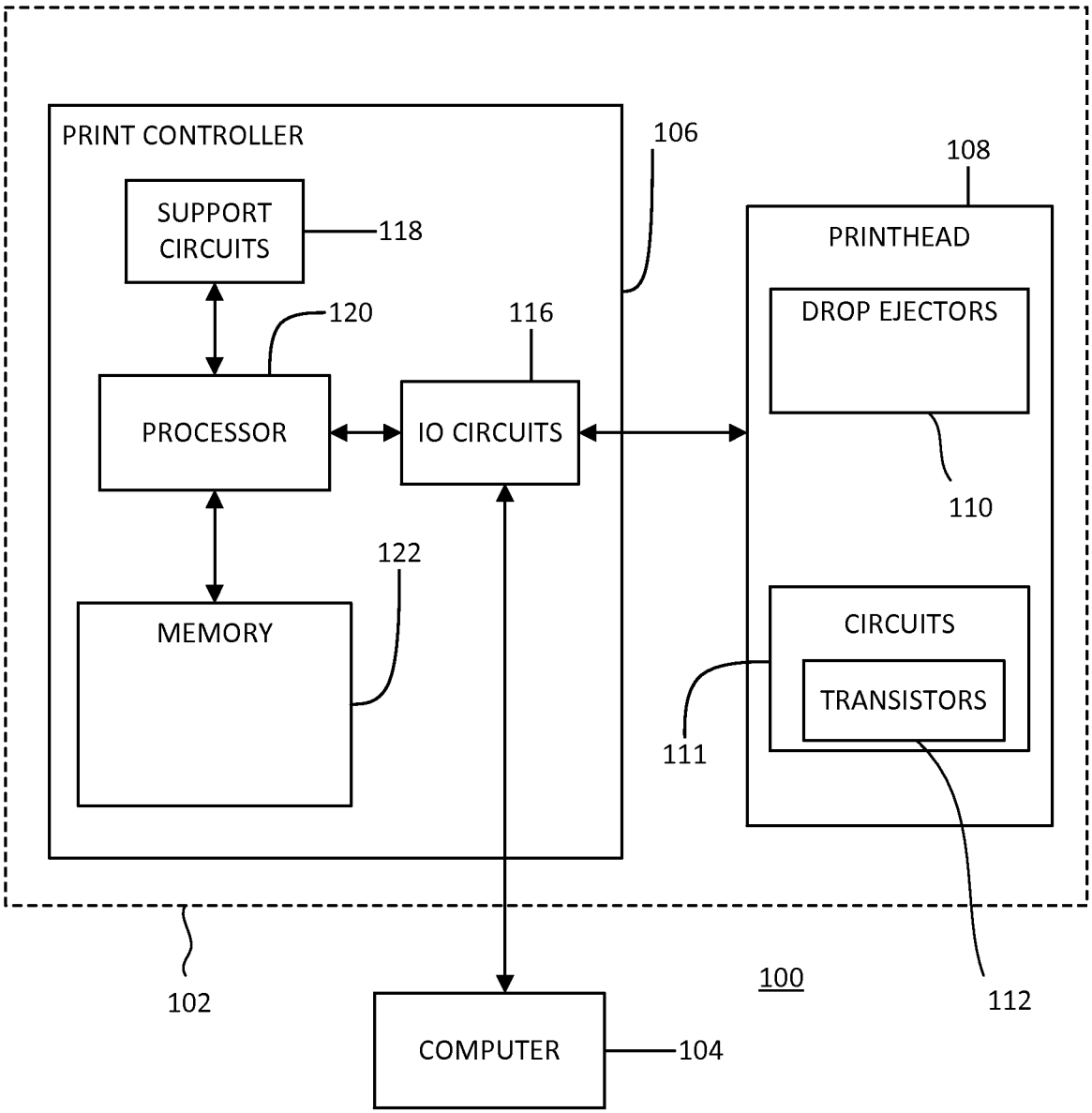

PRINT CONTROLLER
106
108
SUPPORT CIRCUITS
118
PRINTHEAD
DROP EJECTORS
120
116
PROCESSOR
IO CIRCUITS
110
122
MEMORY
CIRCUITS
TRANSISTORS
111
102
100
112
COMPUTER
104

FIG.1

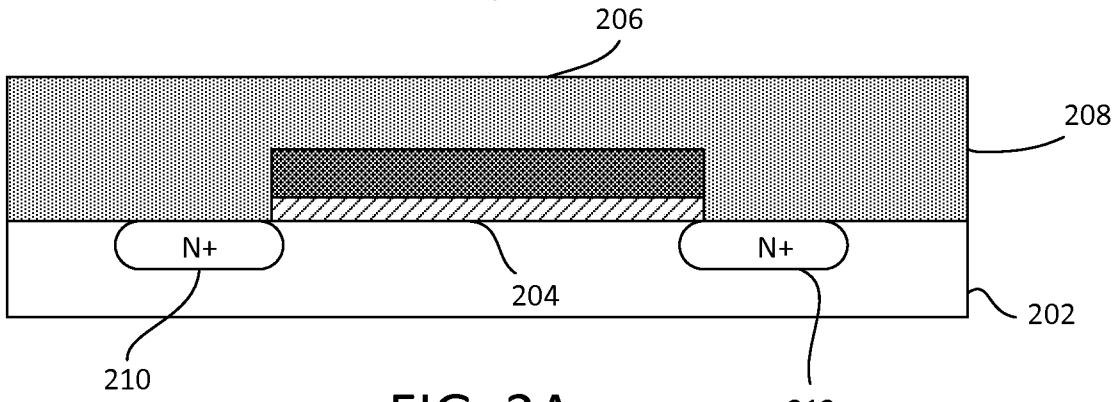


FIG. 2A

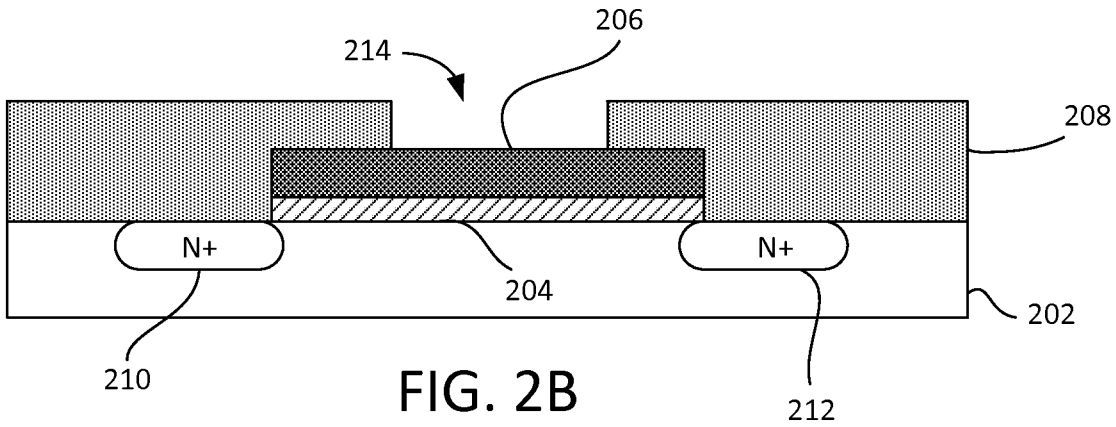


FIG. 2B

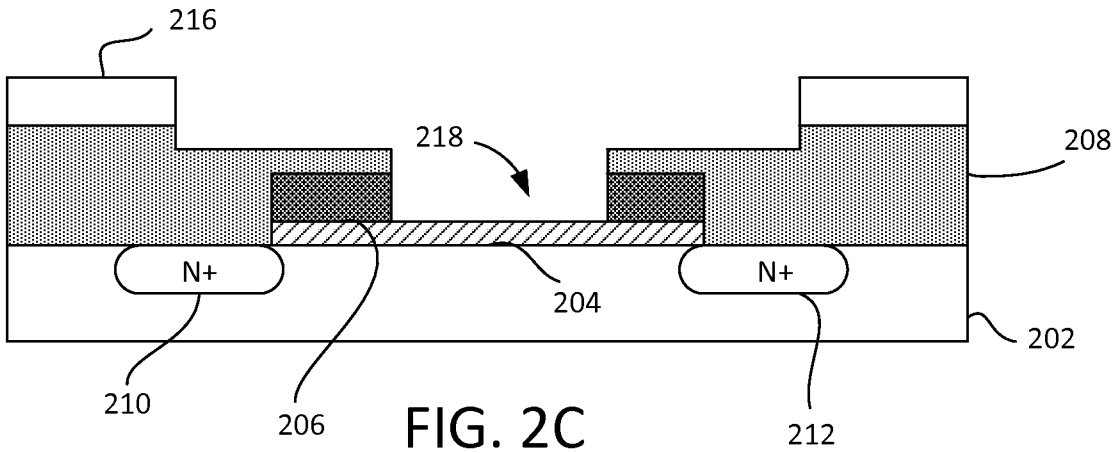


FIG. 2C

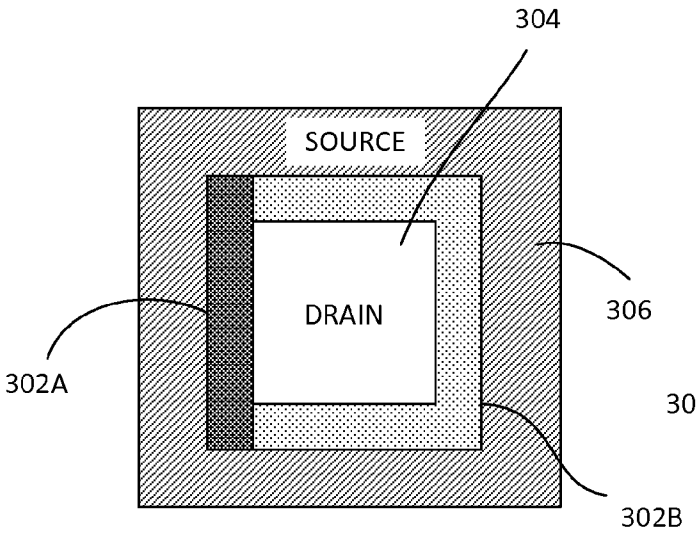


FIG. 3A

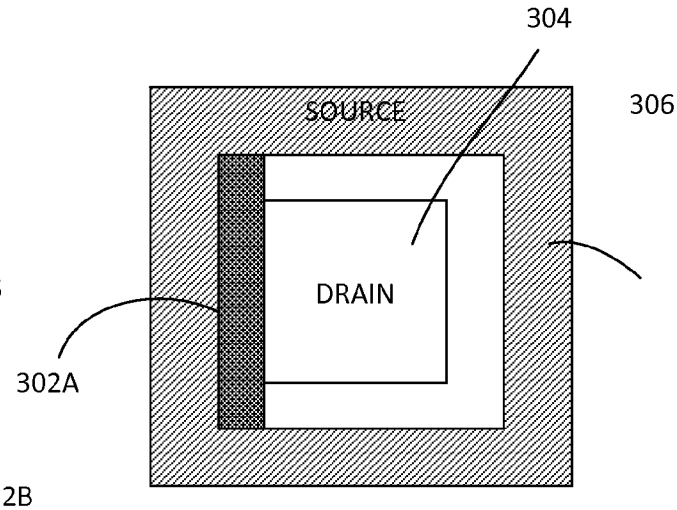


FIG. 4A

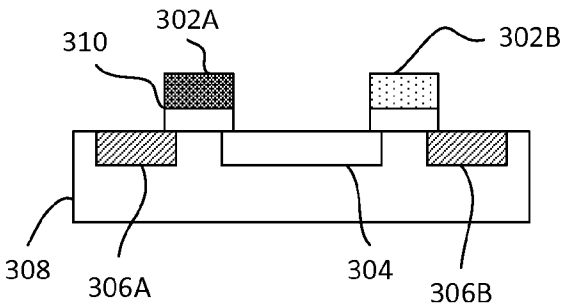


FIG. 3B

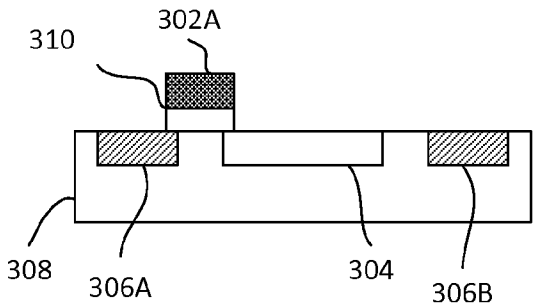


FIG. 4B

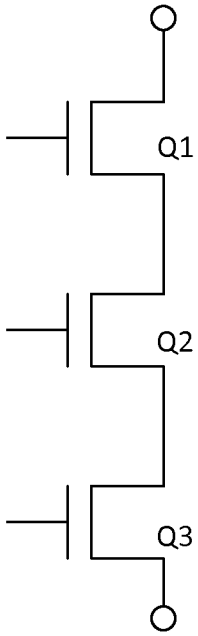


FIG. 5A

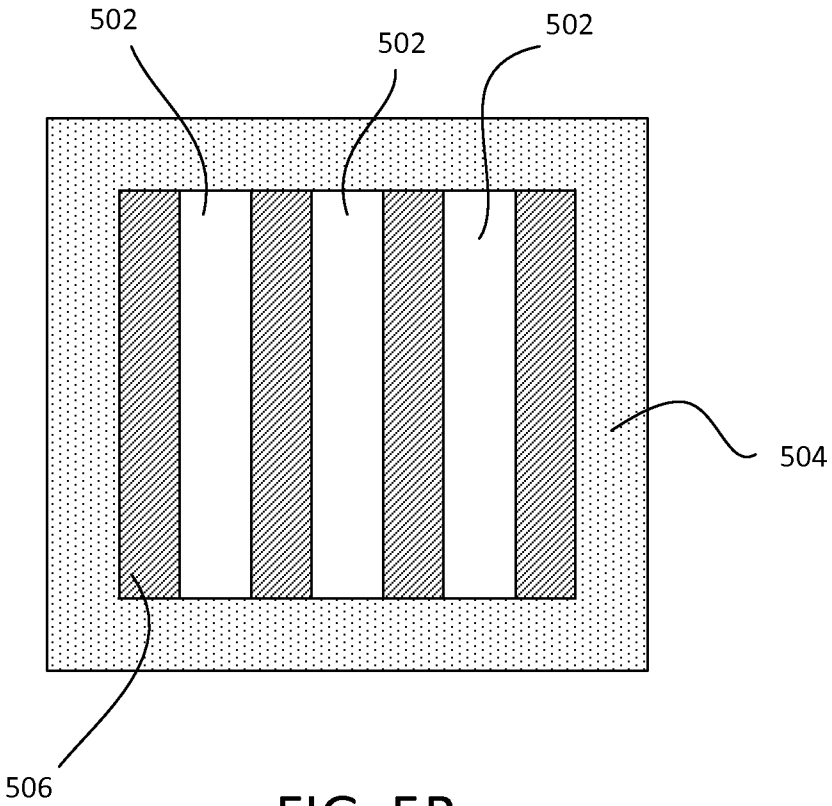


FIG. 5B

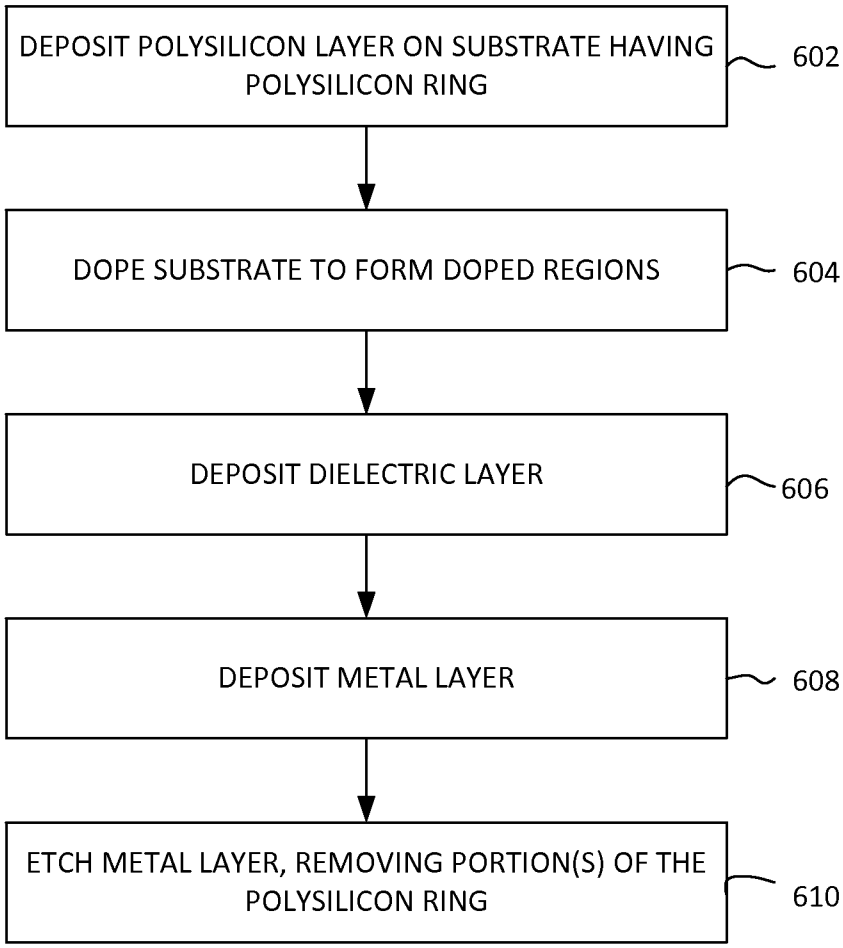
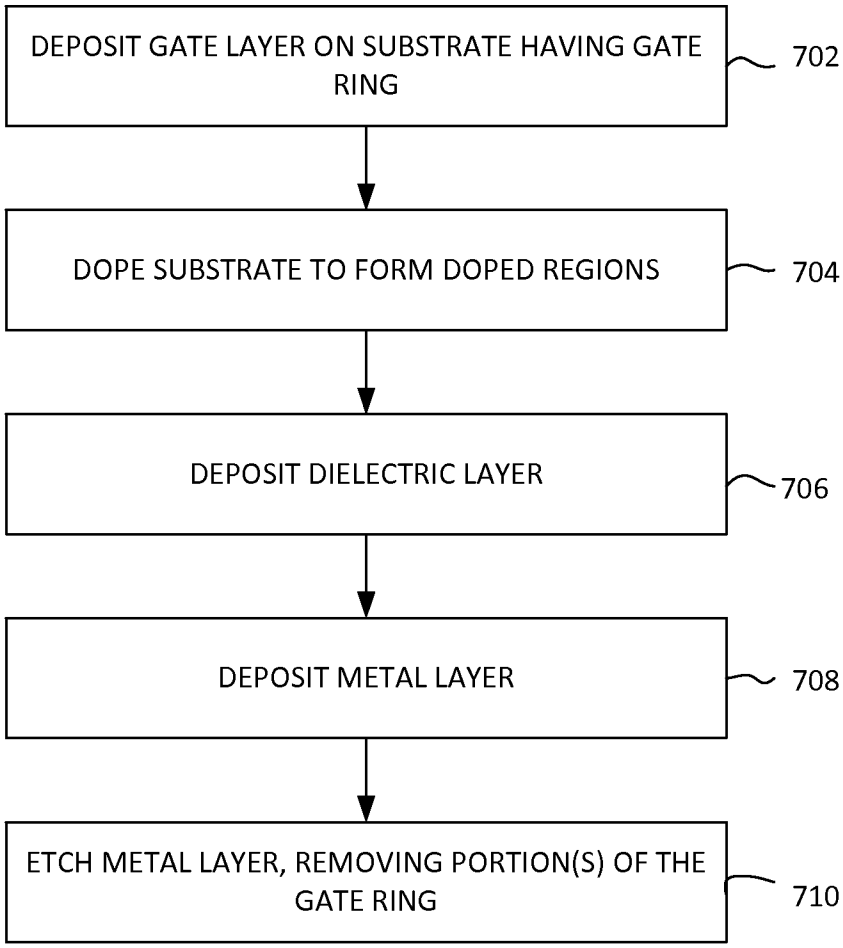

DEPOSIT POLYSILICON LAYER ON SUBSTRATE HAVING POLYSILICON RING
602
DOPE SUBSTRATE TO FORM DOPED REGIONS
604
DEPOSIT DIELECTRIC LAYER
606
DEPOSIT METAL LAYER
608
ETCH METAL LAYER, REMOVING PORTION(S) OF THE POLYSILICON RING
610
600

FIG. 6


DEPOSIT GATE LAYER ON SUBSTRATE HAVING GATE RING
702
DOPE SUBSTRATE TO FORM DOPED REGIONS
704
DEPOSIT DIELECTRIC LAYER
706
DEPOSIT METAL LAYER
708
ETCH METAL LAYER, REMOVING PORTION(S) OF THE GATE RING
710

710

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/057482

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 21/20; H01L 21/8236; H01L 29/78; H01L 21/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: polysilicon, gate, ring, transistor, substrate, doping, etching, dielectric, metal and mask

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2008-0060995 A (DONGBU ELECTRONICS CO., LTD.) 02 July 2008 See abstract, paragraphs [0011]-[0025] and figures 2-5.	9-10
A		1-8
Y	KR 10-1999-0045409 A (LUCENT TECHNOLOGIES INC.) 25 June 1999 See abstract, claims 1-14 and figures 1-6.	9-10
A	US 2012-0306014 A1 (RENATA CAMILLO-CASTILLO et al.) 06 December 2012 See abstract, paragraphs [0014]-[0023] and figures 1A-1K.	1-10
A	US 2002-0086491 A1 (ISIK C. KIZILYALLI et al.) 04 July 2002 See abstract, paragraphs [0022]-[0036] and figures 1-9.	1-10
A	US 2005-0212063 A1 (FUMIKI NAKANO et al.) 29 September 2005 See paragraphs [0051]-[0062], [0080]-[0091] and figures 2A-2B, 9A-14.	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 May 2014 (28.05.2014)	**29 May 2014 (29.05.2014)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/057482

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2008-0060995 A	02/07/2008	None	
KR 10-1999-0045409 A	25/06/1999	JP 11-261065 A	24/09/1999
US 2012-0306014 A1	06/12/2012	None	
US 2002-0086491 A1	04/07/2002	GB 0028873 D0	10/01/2001
		GB 2363903 A	09/01/2002
		JP 2001-196468 A	19/07/2001
		KR 10-2001-0062112 A	07/07/2001
		TW 480670 A	21/03/2002
		TW 480670 B	21/03/2002
		US 2002-0048893 A1	25/04/2002
		US 6383879 B1	07/05/2002
		US 6573149 B2	03/06/2003
		US 6579775 B2	17/06/2003
US 2005-0212063 A1	29/09/2005	JP 2005-311323 A	04/11/2005
		US 2007-0228469 A1	04/10/2007
		US 7309900 B2	18/12/2007