613153

FORM 1
REGULATION 9

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952-1973

APPLICATION FOR A PATENT

We GEC PLESSEY TELECOMMUNICATIONS LIMITED

of P.O. Box 53, Telephone Road, Coventry CV3 1HJ, ENGLAND

hereby apply for the grant of a Patent for an invention entitled:

MEMORY ADDRESSING SYSTEM

which is described in the accompanying complete specification. This Application is a Convention Application and is based on the Application numbered: 8803926 for a Patent or similar protection made in United Kingdom on 19 February 1988.

Our address for service is:

GRIFFITH HACK & CO.
71 YORK STREET
SYDNEY N.S.W. 2000
AUSTRALIA

DATED this 17th day of February, 1989.

GEC PLESSEY TELECOMMUNICATIONS LIMITED
By their Patent Attorneys

GRIFFITH HACK & CO.

TO: THE COMMISSIONER OF PATENTS
COMMONWEALTH OF AUSTRALIA

005572 17/02/89

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FORM 8

COMMONWEALTH OF AUSTRALIA TEX/3066 AU.

PATENTS ACT 1952

DECLARATION IN SUPPORT OF AN APPLICATION FOR A PATENT

In support of an application made by:
GEC PLESSEY TELECOMMUNICATIONS LIMITED

for a patent for an invention entitled:
"MEMORY ADDRESSING SYSTEM"

I, COLIN FRANCIS HOSTE

of, THE GENERAL ELECTRIC COMPANY, plc., PATENT DEPT., (WEMBLEY OFFICE) Hirst Research Centre, East Lane, Wembley, Middx. HA9 7PP, England,
do solemnly and sincerely declare as follows:

1. I am authorised by the above mentioned applicant for the patent to make this declaration on its behalf.

2. The name and address of each actual inventor of the invention is as follows:

   Anthony Peter Lumb, Michael John Mills and Howard Williams of 63 Merlin Avenue, Nuneaton, Warwickshire, ENGLAND, 47 Common Lane, Kenilworth, Warwickshire, ENGLAND and 18 Sunnyside Close, Chapelfield, Conventry, Warwickshire, ENGLAND, respectively

   and the fact(s) upon which the applicant is entitled to make this application are as follows:

The inventors have assigned the application to General Electric Company plc who have in turn assigned the application to GEC Plessey Telecommunications Limited.

3. The basic application as defined by Section 141 of the Act was made as follows:

   In United Kingdom on 19th February 1988
   in the name GENERAL ELECTRIC COMPANY p.l.c.

4. The basic application referred to in the preceding paragraph of this Declaration was the first application made in a Convention country in respect of the invention the subject of this application.

DECLARED at Wembley, England.

this 4th day of February 19 91.

Signed: C F Hoste COLIN FRANCIS HOSTE

Position: THEIR ATTORNEY

GRIFFITH HACK & CO, GPO BOX 4164, SYDNEY, NSW, 2001
AUSTRALIA

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(12) PATENT ABRIDGMENT (11) Document No. AU-B-30056/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 613153

(54) Title
MEMORY ADDRESSING SYSTEM

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(30) Priority Data

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8803926 **19.02.88** **GB UNITED KINGDOM**

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(71) Applicant(s)
GEC PLESSEY TELECOMMUNICATIONS LIMITED

(72) Inventor(s)
ANTHONY PETER LUMB; MICHAEL JOHN MILLA; HOWARD WILLIAMS

(74) Attorney or Agent
GRIFFITH HACK & CO. , GPO Box 4164, SYDNEY NSW 2001

(56) Prior Art Documents
GB 2099619
US 4307448

(57) Claim

1. A memory addressing system comprising at least two main processor units, at least one input/output processor unit, at least two dynamic RAM memory modules, and a synchronous bus inter-connecting the modules and units, the memory modules together providing a physical address space greater than the address range available on the synchronous bus, and wherein each processor unit is connected in parallel with the synchronous bus to first static RAM arrays each of which is associated with an individual one of said memory modules, each of said first static RAM arrays being connected to an associated second static RAM array in turn connected to the associated dynamic RAM memory module, said second static RAM arrays each containing translation tables relating to the address space of the associated memory module, the system being such that when a processor unit wishes to access one of said memory modules a sequence is followed in which the processor unit outputs an address onto said bus and data to the first static RAM array associated with the memory module which the processor unit wishes to access, the first static array outputting to its associated second static RAM a plurality of bits associated with the particular processor unit requiring access, the second array in response to this data and to part of the address enabled onto the bus by the processor unit outputting part of the address

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required to access the memory module, the remainder of the address being provided by the remainder of the address enabled on to the bus.

COMMONWEALTH OF AUSTRALIA 6 13153

PATENTS ACT 1952 Form 10

COMPLETE SPECIFICATION

FOR OFFICE USE

Short Title:

Int. Cl:

Application Number:
Lodged:

Complete Specification-Lodged:
Accepted:
Lapsed:
Published:

Priority:

Related Art:

TO BE COMPLETED BY APPLICANT

Name of Applicant:	GEC PLESSEY TELECOMMUNICATIONS LIMITED
Address of Applicant:	P.O. Box 53, Telephone Road, Coventry CV3 1HJ, ENGLAND
Actual Inventor:	Anthony Peter Lumb ; Michael John Milla and Howard Williams
Address for Service:	GRIFFITH HACK & CO. 71 YORK STREET SYDNEY NSW 2000 AUSTRALIA

Complete Specification for the invention entitled:

MEMORY ADDRESSING SYSTEM

The following statement is a full description of this invention, including the best method of performing it known to me/us:-

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TEX/3066 AU

MEMORY ADDRESSING SYSTEM

The present invention concerns a memory addressing system particularly suited to the main processors of a digital telephone exchange.

A typical digital telephone exchange may have four main processors and two input/output processors co-operating with a plurality of storage units. The processors and storage units can be referred to as modules with the modules being interconnected by duplicated synchronous buses. In one example each bus will contain 22 address bits and 16 data bits with 16 bits being defined as a word.

A problem arises because of the limited address range available to each of the processor modules. With 22 address bits available each processor module can address 4 Megawords. Thus each module can address either a single 4 Megaword storecard or several storecards of reduced capacity. In a typical system having seven storecards each storecard has accordingly been limited to 0.5 inwords.

The present invention has for an object effectively to increase the address range available to a processor unit in a memory addressing system of the kind just described.

Accordingly the present invention consists of a memory addressing system comprising at least two main processor units, at least one input/output processor unit, at least two dynamic RAM memory modules, and a synchronous bus

inter-connecting the modules and units, the memory modules together providing a physical address space greater than the address range available on the synchronous bus, and wherein each processor unit is connected in parallel with the synchronous bus to first static RAM arrays each of which is associated with an individual one of said memory modules, each of said first static RAM arrays being connected to an associated second static RAM array in turn connected to the associated dynamic RAM memory module, said second static RAM arrays each containing translation tables relating to the address space of the associated memory module, the system being such that when a processor unit wishes to access one of said memory modules a sequence is followed in which the processor unit outputs an address onto said bus and data to the first static RAM array associated with the memory module which the processor unit wishes to access, the first static array outputting to its associated second static RAM a plurality of bits associated with the particular processor unit requiring access, the second array in response to this data and to part of the address enabled onto the bus by the processor unit outputting part of the address required to access the memory module, the remainder of the address being provided by the remainder of the address enabled on to the bus.

Preferably the memory address system has duplicated synchonous buses. These may be implemented using TTL technology.

In accordance with another feature of the invention each module has an individual address and is operative to monitor said bus for said address. the access sequence commencing when a memory module detects a match with its address and the presence on the bus of valid commands.

In order that the invention may be more readily understood, an embodiment thereof will now be described by way of example and with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a memory addressing system according to the present invention, and

Figure 2 is a block diagram showing part of the system of Figure 1 in greater detail.

Referring now to Figure 1 of the drawings this shows four

main processor units or CPUs' 10A - 10D, two input/out processor 11A, 11B, seven storage units 12A - 12G normally called storecards and duplicated clock units CLOCK 0 and CLOCK 1. Timing signals for the various modules making up the system are supplied by clock units CLOCK 1 and 0 over duplicated synchronous buses 1 and 0.

Each of the synchronous buses (0 or 1) has 22 address bits plus parity and 16 data bits plus parity. Furthermore each bus also contains 5 command lines, these being respectively Read, Write, Read/Clear, Maintenance Read and Maintenance Write.

Finally each bus also contains a transfer validation signal, a response line which is used to indicate the success or failure of a bus access, and 6 Grant code lines. Each of the modules in the system is allocated a unique Grant Code and enables this code onto one of the two buses whenever the module also drives the address and data lines of the bus. The grant code lines are implemented using Open Collector technology drives so that should a module become faulty and enable address/data onto the bus at the wrong time the grant codes received by the destination module will be invalid as they will consist of a combination of two grant codes.

In previous systems of this type the address range available on the buses limited the storecards 12A - 12G to 0.5 MWord capacity and the storecards only checked the grant codes for a valid CPU or I/OP code. However in the embodiment being described each storecard has a capacity of 4 Mwords and uses a received grant code to establish translations from a physical bus address to a dynamic RAM address which can be unique to one of the processor modules.

In order to achieve this each storecard is associated with an individual first static RAM array which is connected to the processor modules in parallel to the two main synchronous buses 0 and 1. This additional data line is shown in Figure 1 at 25. In a preferred embodiment a just static RAM array and a second RAM array storage translation tables are physically incorporated in the individual storecards. Figure 2 of the drawings shows the actual relationship between a synchronous bus, in this case bus 1, a first static RAM 30, a second static RAM 35 and storecard 12A.

There will now be described the sequence followed when a processor module wishes to access one of the storecards.

A sequence of time slots are defined by the clock 0 or 1 and

during a specified time slot all the storecards 12A -12G monitor one of the duplicated buses 0 or 1 for its unique address. In the present embodiment this address is defined by the top three bus address bits 19, 20 and 21 as shown on the 22 bit synchonous bus address. When a storecard detects a match between its unique address and the top three bus bits together with a valid command (Read, Write, or Read/Clear) that storecard begins the access sequence.

The start of this access sequence is the application of certain parts of the selected bus grant code to the address of a first static RAM 30 which is a small fast static RAM array. On receipt of this data array 30 outputs 11 bits of data plus a single parity bit to the second static RAM array 35. Of these 11 bits 7 are associated with the particular processor module performing the storecard access. This data will be referred to as the Bank value and in the present embodiment only 5 of the 7 bits are valid on the 4 Mwords storecard. Thus there are 32 possible Bank values. The 5 bits of Bank value output by array 30 are then combined with 11 bus address bits. These are bits 8 -18 of the 22 bus address bits. The 16 bits so generated are then applied to the second static RAM array 35. The RAM array 35 has a 64K capacity. In this way the 4 Mwords address space of the storecard can be divided into sections or banks each containing a maximum of 2K (2 to the power of 11) address translations. The array 35 provides 16 data outputs plus a single parity bit of which 14 are combined with the remaining 8 bits on the 22 bit bus address. These remaining bits are bit 0 - 7. This combination generates the 22 bits necessary to address the 4 Mword memory space of the selected storecard. The unused two bits from the two arrays 30, 35 allow for an expansion in the size of array 35 to 256 K words and of the storecards to 16 Mword arrays.

In the system described a means has to be provided for setting up the two RAM arrays 30 and 35 and also for enabling direct accesses of the storecards in a manner which does not involve the use of the translation tables stored in the 64 K static array 35. These requirements, in the present embodiment, are achieved by extracting 11 page addresses from the internal address range of each storecard. This reduces the number of translations available to one of the processor modules from 2048 (2K locations) down to 2037. However

these facilities do not affect the size of Synamic RAM address available to a processor module, this size being maintained in the unexpanded form at 4 Mwords. However a security check can be implemented into each storecard to check on the data stored in the second array 35. This indicates that a translation stored in array 35 is undefined and hence should not have been used by a processor module. This security measure removes one page from the maximum dynamic RAM range of each store card of 16 Mwords.

In the embodiment being described the data in the two static RAM arrays 30 and 35 can only be set up by a main processor unit 10A - 10D, not one of the input/output processor 11A, 11B

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A memory addressing system comprising at least two main processor units, at least one input/output processor unit, at least two dynamic RAM memory modules, and a synchronous bus inter-connecting the modules and units, the memory modules together providing a physical address space greater than the address range available on the synchronous bus, and wherein each processor unit is connected in parallel with the synchronous bus to first static RAM arrays each of which is associated with an individual one of said memory modules, each of said first static RAM arrays being connected to an associated second static RAM array in turn connected to the associated dynamic RAM memory module, said second static RAM arrays each containing translation tables relating to the address space of the associated memory module, the system being such that when a processor unit wishes to access one of said memory modules a sequence is followed in which the processor unit outputs an address onto said bus and data to the first static RAM array associated with the memory module which the processor unit wishes to access, the first static array outputting to its associated second static RAM a plurality of bits associated with the particular processor unit requiring access, the second array in response to this data and to part of the address enabled onto the bus by the processor unit outputting part of the address required to access the memory module, the remainder of the address being provided by the remainder of the address enabled on to the bus.

2. A memory addressing system as claimed in Claim 1, wherein each module has an individual address, and the bus includes a plurality of Grant Code lines on which the individual addresses of the modules are carried, each of the first static arrays being connected to said Grant Code lines.

3. A memory addressing system substantially as hereinbefore described with reference to the accompanying drawings.

Dated this 2nd day of November 1990.

GEC PLESSEY TELECOMMUNICATIONS LTD
By their Patent Attorney
GRIFFITH HACK & CO.

Fig. 1.

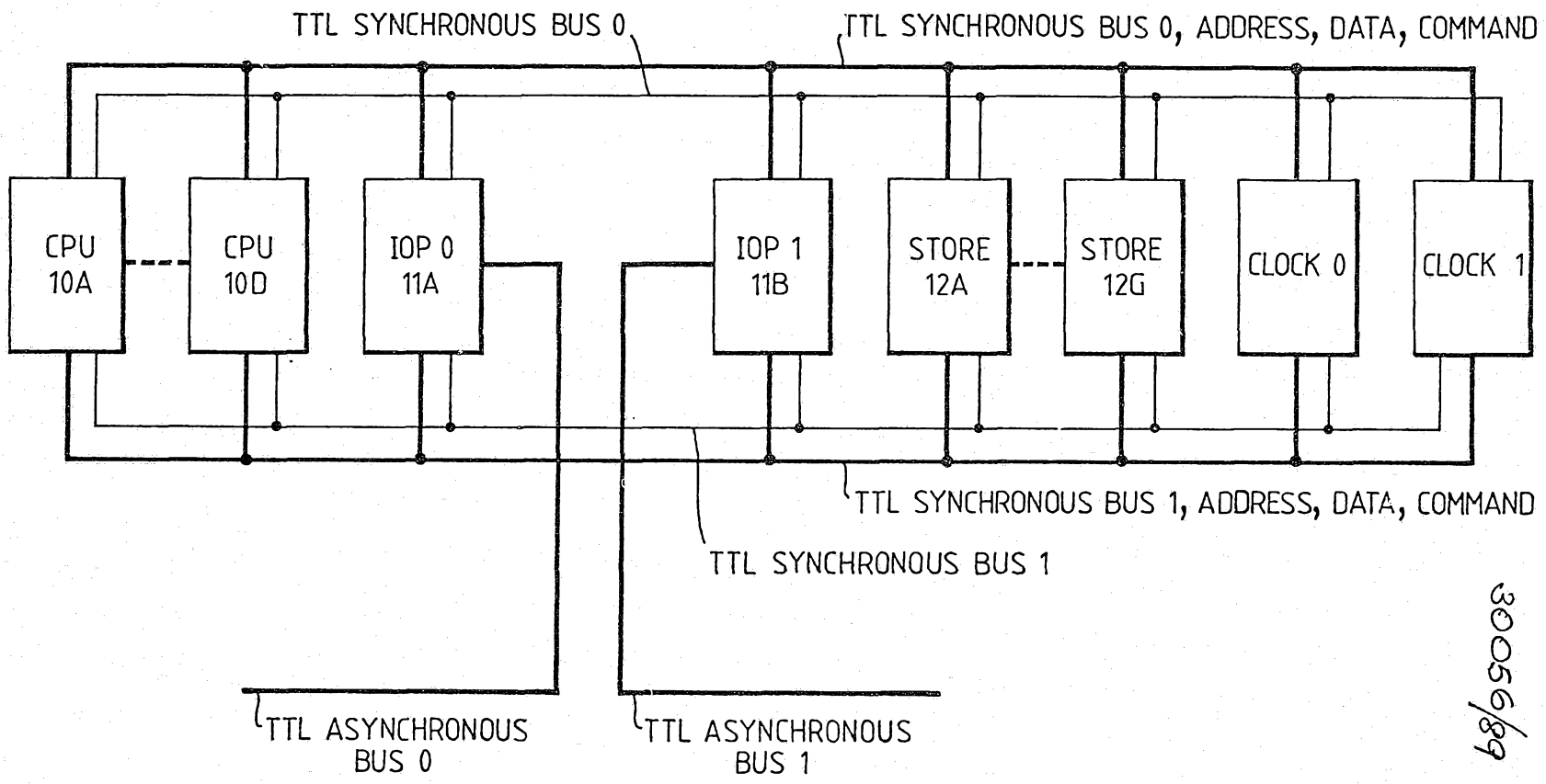

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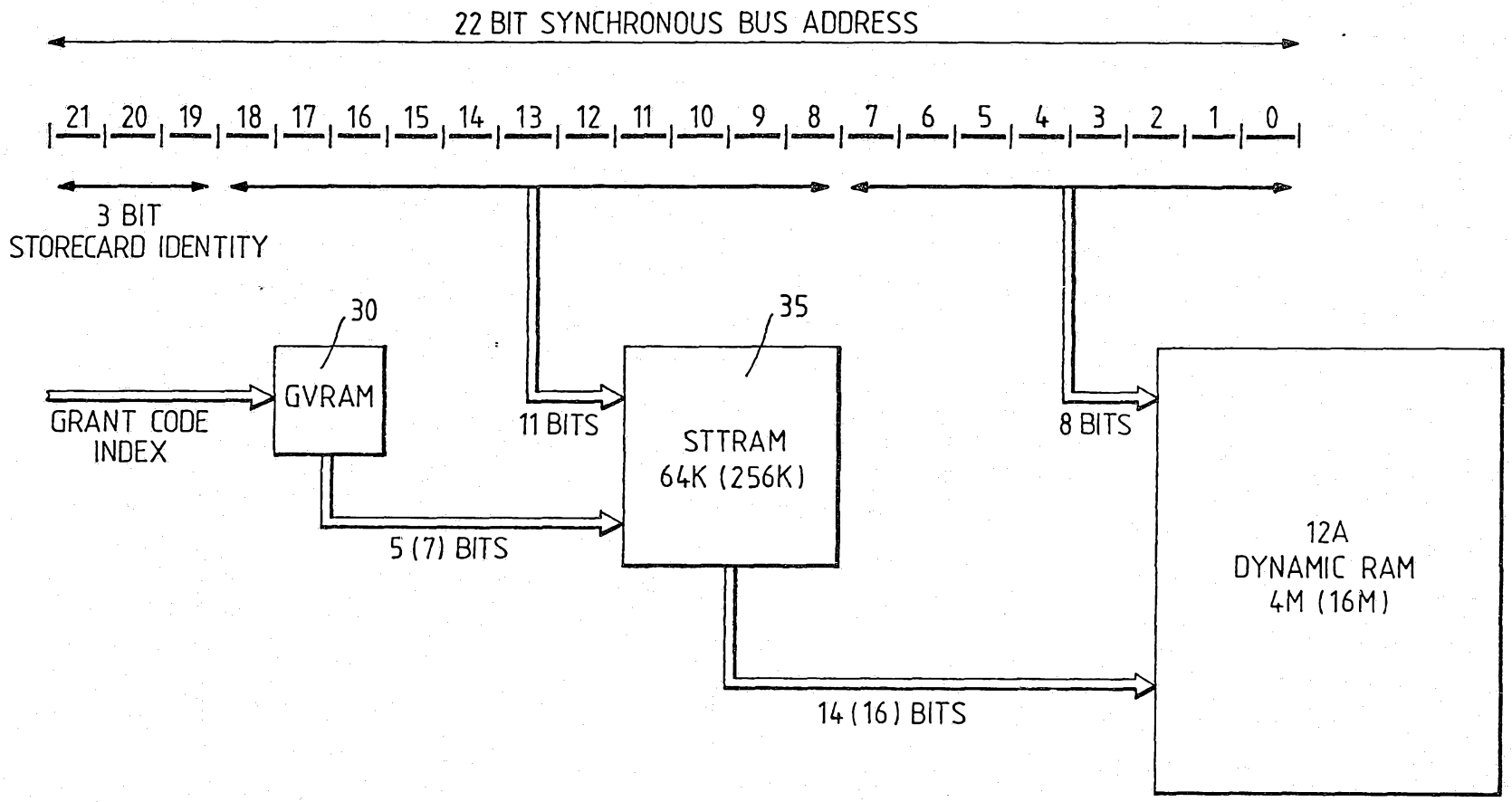
Fig.2.


22 BIT SYNCHRONOUS BUS ADDRESS
21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
3 BIT
STORECARD IDENTITY
30
GVRAM
GRANT CODE
INDEX
11 BITS
35
STTRAM
64K (256K)
8 BITS
5 (7) BITS
12A
DYNAMIC RAM
4M (16M)
14 (16) BITS