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(54) FLASH EEPROM CELL AND METHOD OF MANUFACTURING THE SAME

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(57) **ABSTRACT**

The invention relates to a flash EEPROM cell and method of manufacturing the same. The method of manufacturing a flash EEPROM cell includes sequentially forming a tunnel oxide film, a polysilicon layer for a floating gate and a hard mask layer on a semiconductor substrate; patterning the hard mask layer and then forming a hard mask layer spacer at the etching side of the patterned hard mask layer; removing the exposed portion of the ploysilicon layer for the floating gate by etching process using the patterned hard mask layer and the hard mask layer spacer as etching masks thus to form first and second patterns that are separated in two; removing the patterned hard mask layer and the hard mask layer spacer and then depositing a dielectric film and a polysilicon layer for a floating gate on the entire structure, thus forming a first floating gate, a second floating gate and a control gate by self-aligned etching process; and forming a drain junction and a source junction by cell source/drain ion implantation process. Thus, the present invention can prevent lower of the quality of the tunnel oxide film and thus increase the coupling ratio.

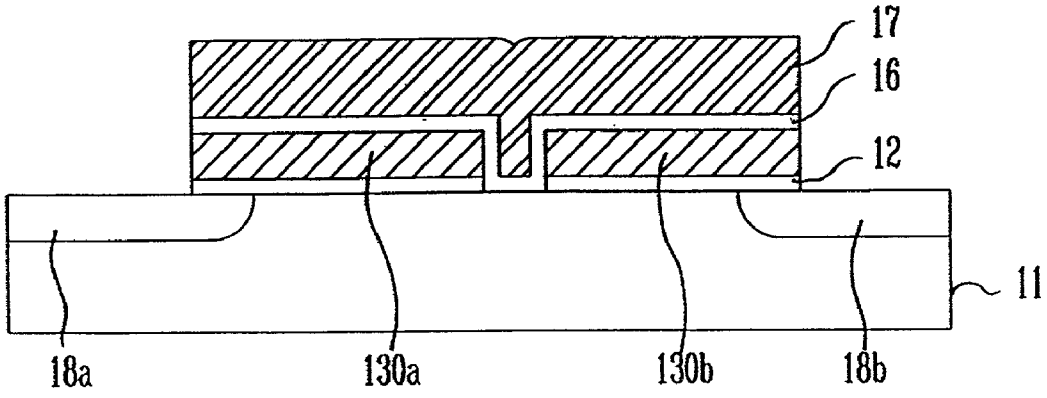


FIG. 1A

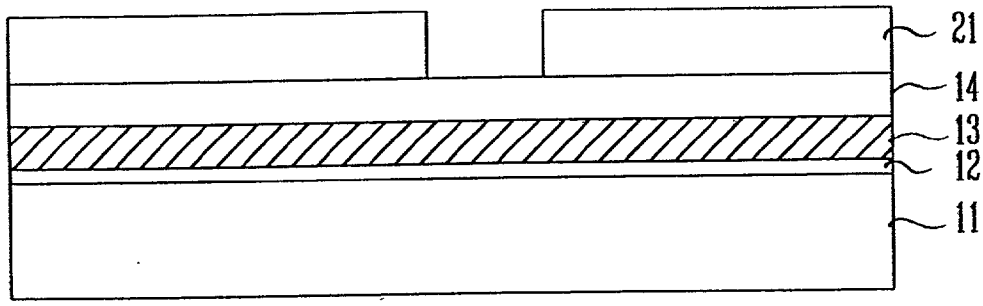


FIG. 1B

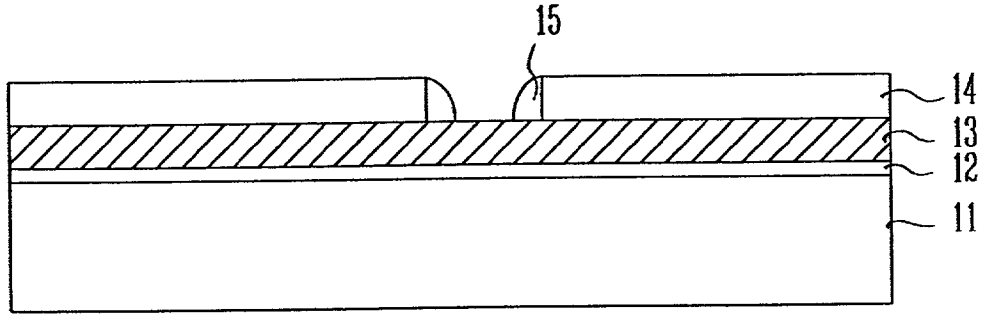


FIG. 1C

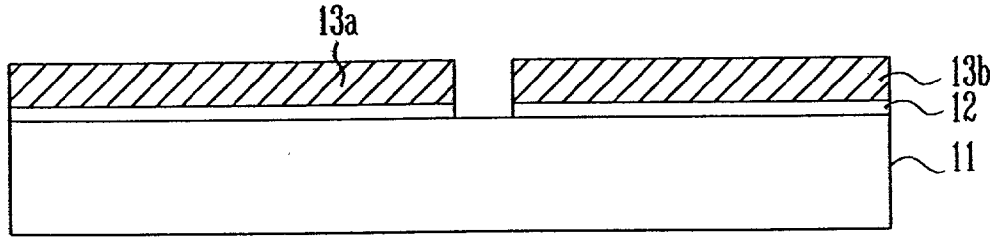
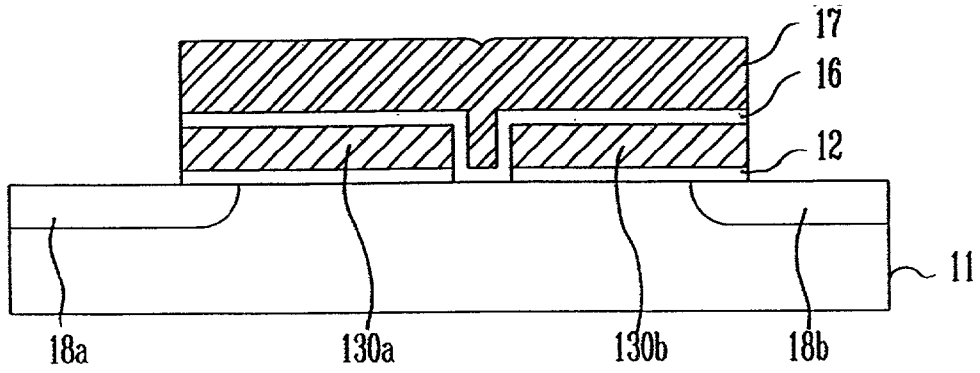


FIG. 1D



FLASH EEPROM CELL AND METHOD OF MANUFACTURING THE SAME

RELATED APPLICATIONS

[0001] This is a Divisional of application Ser. No. 09/609,337, filed Jun. 30, 2000, now U.S. Pat. No. 6,339,006.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates generally to a flash EEPROM cell and method of manufacturing the same. More particularly, the present invention relates to a flash EEPROM cell in which two floating gates having different sizes can be simply formed at a single cell using a hard mask layer in a multi-level cell, capable of preventing lower of the quality of a tunnel oxide film and increasing the coupling ratio, and method of manufacturing the same.

[0004] 2. Description of the Prior Art

[0005] The greatest bottleneck to prevent customization of the current flash EEPROM is that the cost per unit information is high. For this, the higher integration of a cell is required and thus various manufacturers have made an effort to develop it. However, as the structure of the EEPROM is complicated compared to that of the DRAM, there is a problem that the integration level of the EEPROM is difficult to increase.

[0006] The conventional flash EEPROM cell has only two states (storing only binary information) depending on whether the electrons is charged at the floating gate or not. Thus, it has a drawback that the chip size is increased due to one bit per one cell in the large-scale configuration of the cell array depending on it.

[0007] On the other hand, as the multi-level cell has four states, it can store information at one cell instead of storing it at two cells. Thus, it can store much information at the same area. However, in the multi-level cell, as two floating gates have to be formed at one cell, many processes has to be experienced to manufacture it. Also, as forming the tunnel oxide film has to be performed in two steps, it is difficult to assure the quality of the tunnel oxide film and to assure the quality of the tunnel oxide film below a poly spacer in case of using the poly spacer.

SUMMARY OF THE INVENTION

[0008] It is therefore an object of the present invention to provide a flash EEPROM cell in which two floating gates having different size can be simply formed at a single cell using a hard mask layer in a multi-level cell, capable of preventing lower of the quality of a tunnel oxide film and increasing the coupling ratio, and method of manufacturing the same.

[0009] In order to accomplish the above object, a flash EEPROM cell according to the present invention is characterized in that it comprises first and second floating gates, that are different in size and separated in two, formed to be electrically separated from a semiconductor substrate by a tunnel oxide film; control gate formed to be electrically separated from said first and second floating gates by a dielectric film; drain junction formed on said semiconductor substrate at the side of said first floating gate; and source junction formed on said semiconductor substrate at the side of said second floating gate.

[0010] Also, in order to accomplish the above object, the method of manufacturing a flash EEPROM cell according to the present invention is characterized in that it comprises the steps of sequentially forming a tunnel oxide film, a polysilicon layer for a floating gate and a hard mask layer on a semiconductor substrate; patterning said hard mask layer and then forming a hard mask layer spacer at the etching side of the patterned hard mask layer; removing the exposed portion of the ploysilicon layer for the floating gate by etching process using said patterned hard mask layer and said hard mask layer spacer as etching masks thus to form first and second patterns that are separated in two; removing said patterned hard mask layer and said hard mask layer spacer and then depositing a dielectric film and a polysilicon layer for a floating gate on the entire structure, thus forming a first floating gate, a second floating gate and a control gate by self-aligned etching process; and forming a drain junction and a source junction by cell source/drain ion implantation process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[0012] **FIGS. 1A through 1D** are sectional views for explaining a flash EEPROM cell and method of manufacturing the same according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0013] The present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

[0014] **FIGS. 1A through 1D** are sectional views for explaining a flash EEPROM cell and method of manufacturing the same according to the present invention.

[0015] Referring now to **FIG. 1A, a** field oxide film (not shown) is formed and a tunnel oxide film **12** is formed on a semiconductor substrate **11** in which an active region and a field region are defined. Then, a polysilicon layer for the floating gate **13** is formed on the tunnel oxide film **12**. Next, a hard mask layer **14** is formed on the polysilicon layer for the floating gate **13**. Thereafter, a photoresist pattern **21** is formed on the hard mask **14** by exposure and developing process using the mask for the floating gate.

[0016] In the above, the tunnel oxide film **12** is formed in thickness of 50 through 150 Angstrom and the polysilicon layer **13** for the floating gate is formed in thickness of 300 through 2000 Angstrom. The hard mask layer **14** is formed of nitride, oxy-nitride, oxide etc. having a high etch selectivity upon etching of the polysilicon layer, in thickness of 200 through 2000 Angstrom. The photoresist pattern **21** is formed at a minimum feature size that can be formed by exposure process in order to reduce its chip size.

[0017] Referring to **FIG. 1**B, the mask layer **14** is patterned by etching process using the photoresist pattern **21** as

an etching mask. After the photoresist pattern **21** is removed, a hard mask layer spacer **15** is formed at the etching face of the patterned hard mask layer **14**.

[**0018**] In the above, the hard mask layer spacer **15** is formed of nitride, oxy-nitride, oxide etc. having a high etch selectivity upon etching of the polysilicon layer, in thickness of 200 through 2000 Angstrom, using blanket etching process. As the hard mask layer spacer **15** is formed, still smaller size of spacer can be obtained than the minimum size that can be formed by exposure process, thus increasing the effect of reducing the chip size.

[**0019**] Referring now to **FIG. 1**C, by etching process using the patterned hard mask layer **14** and the hard mask layer spacer **15** as etching mask, the exposed portion of the polysilicon layer for the floating gate **13** is removed to form a first pattern **13***a* and a second pattern **13***b* which are separated in two section. Then, annealing process for recovering the portion of the tunnel oxide film **12** that is damaged by etching process is performed.

[**0020**] Referring to **FIG. 1**D, the patterned hard mask layer **14** and the hard mask layer spacer **15** are removed and a dielectric film **16** and a polysilicon layer for the floating gate **17** are deposited on the entire structure including the first pattern **13***a* and the second pattern **13***b* which are separated in two section. Then, self-aligned etching process using the control gate as a mask is used to allow the polysilicon layer for the floating gate **17** and the polysilicon layer for the floating gate **13** etching the first pattern **13***a* and the second pattern **13***b* which are separated in two section, thus forming a first floating gate **130***a* made of some of the first pattern **13***a*, a second floating gate **130***b* made of some of the second pattern **13***b* and a control gate **17** lying over the floating gates **130***a* and **130***b*. Then, a drain junction **18***a* and a source junction **18***b* are formed by cell source/drain ion implantation process.

[**0021**] In the above, the dielectric film **16** is consisted of the combination of oxide and nitride and has the thickness of 100 through 300 Angstrom. The polysilicon layer for the floating gate **17** is formed in thickness of 300 through 2000 Angstrom. A polycide layer may be formed instead of the polysilicon layer for the floating gate **17**. The first floating gate **130***a* and the second floating gate **130***b* are different in size, wherein the ratio of the size of the first floating gate **130***a* to the second floating gate **130***b* is ⅓ through 1. The drain junction **18***a* is formed on the semiconductor substrate **11** at the side of the first floating gate **130***a* and the source junction **18***b* is formed on the semiconductor substrate **11** at the side of the second floating gate **130***b*.

[**0022**] Meanwhile, additional process may be added, by which the patterned hard mask layer **14** and the hard mask layer spacer **15** are removed and then dopants different in polarity with the semiconductor substrate **11** are ion-implanted at the dose of 1E14 through 7E16 ions/cm^2.

[**0023**] In the flash EEPROM cell of the present invention formed by the above process, the separated first and second floating gates **130***a* and **130***b* having different sizes are formed to be electrically separated from the semiconductor substrate **11** by the tunnel oxide film **12**, the control gate **17** is formed to be electrically separated from the first and second floating gates **130***a* and **130***b* by the dielectric film **12**, the drain junction **18***a* is located at the side of the first floating gate **130***a* and the source junction **18***b* is located at the side of the second floating gate **130***b*.

[**0024**] In the flash EEPROM cell manufactured by an embodiment of the present invention, the erase operation is performed to discharge from the floating gates to the junction or the channel region due to a tunneling method, and the program operation does not have a significant hot carrier injection problem.

[**0025**] As described above, the flash EEPROM cell using the multi-level cell of the present invention can increase the productivity of the wafers due to the effect of chip size reduction because it allows a data memory of two bits on one cell, can assure the quality of the tunnel oxide film since it can simply form the floating gate most important in the multi-level cell, and can increase the throughput due to increased speed and uniformity upon program and erase because the coupling ratio between the control gate and the floating gate is increased as much as the hard mask layer spacer.

[**0026**] The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

[**0027**] It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.

What is claimed is:

1. A flash EEPROM cell, comprising:

first and second floating gates, that are different in size and separated in two, formed to be electrically separated from a semiconductor substrate by a tunnel oxide film;

control gate formed to be electrically separated from said first and second floating gates by a dielectric film;

drain junction formed on said semiconductor substrate at the side of said first floating gate; and

source junction formed on said semiconductor substrate at the side of said second floating gate.

2. The flash EEPROM cell according to claim 1, wherein the ratio of the size of the first floating gate to the second floating gate is ⅓ to less than **1**.

3. A flash EEPROM cell comprising:

a semiconductor substrate;

spaced apart drain and source junctions formed in the semiconductor substrate;

spaced apart first and second portions of a first film formed above the semiconductor substrate, the first portion of the first film at least partially overlapping one of the drain and source junctions and the second portion of the first film at least partially overlapping the other of the drain and source junctions;

a first floating gate formed above the first portion of the first film and a second floating gate formed above the second portion of the first film, the first and second

floating gates being spaced apart from one another by a gap and having opposing sidewalls;

a dielectic film formed above the first and second floating gates and also covering the opposing sidewalls of the first and second floating gates;

a control gate formed on the dielectric film, the control gate extending over both the first and second floating gates and also extending at least partially into said gap so as to be interposed between the opposing sidewalls of the first and second floating gates;

wherein the first and second floating gates are different in size.

4. The flash EEPROM cell according to claim 3, wherein a ratio of the size of the first floating gate to the second floating gate is ⅓ to less than 1.

5. The flash EEPROM cell according to claim 3, wherein said first film has a thickness of 50 through 150 Angstroms.

6. The flash EEPROM cell according to claim 3, wherein said dielectric film is made of a combination of oxide and nitride and has the thickness of 100 through 300 Angstroms.

7. The flash EEPROM cell according to claim 3, wherein the first and second floating gates are formed from polysilicon having a thickness of 300 through 2000 Angstroms.

8. The flash EEPROM cell according to claim 3, wherein the first and second floating gates are formed from polysilicon having a thickness of 300 through 2000 Angstroms.

9. The flash EEPROM cell according to claim 3, wherein the control gate is formed from polysilicon having a thickness of 300 through 2000 Angstroms

10. The flash EEPROM cell according to claim 3, wherein:

the first film has a thickness of 50 through 150 Angstroms;

the dielectric film is made of a combination of oxide and nitride and has a thickness of 100 through 300 Angstroms;

the first and second floating gates are formed from polysilicon having a thickness of 300 through 2000 Angstroms; and

the control gate is formed from polysilicon having a thickness of 300 through 2000 Angstroms.

11. The flash EEPROM cell according to claim 10, wherein the ratio of the size of the first floating gate to the second floating gate is ⅓ to less than 1.

12. The flash EEPROM cell according to claim 3, wherein the drain junction is formed near the first floating gate and the source junction is formed near the second floating gate.

13. The flash EEPROM cell according to claim 12, wherein the ratio of the size of the first floating gate to the second floating gate is ⅓ to less than 1.

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