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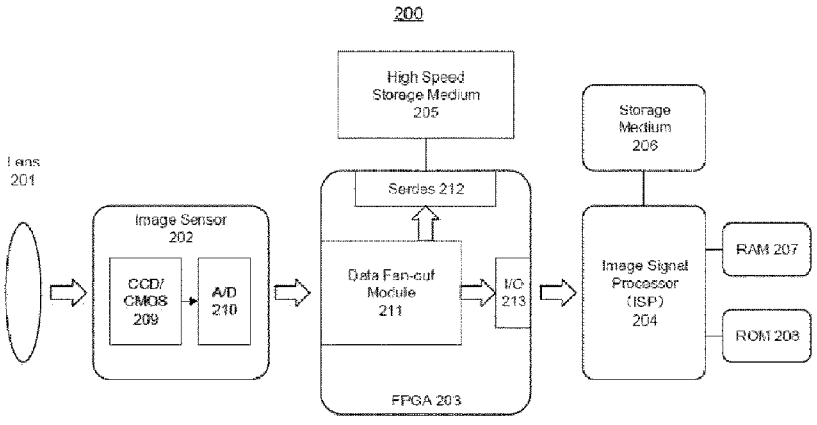


Fig. 2

(57) Abstract: System and method can support an image signal processing apparatus, such as a camera system. The image signal processing apparatus includes a processing device, such as a field programmable gate array (FPGA) device, which operates to receive one or more image data from an image sensor via an image data interface. The processing device can forward the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data and save the compressed image data in a first storage medium. Furthermore, the processing device can export the received one or more image data to a second storage medium via a data communication interface.

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SYSTEM AND METHOD FOR STORING IMAGE DATA IN PARALLEL IN A CAMERA SYSTEM

BACKGROUND

[0001] With the development of faster and higher resolution image sensors, the modern camera becomes ever more versatile and powerful. For example, a cinema camera can use an image sensor to generate a rapid sequence of photographs (i.e., multiple frames of images in one shot), while each photograph (or image frame) contains a large amount of pixels. Thus, there is a need for processing and storing a large amount of image data in the modern camera system. This is the general area that embodiments of the invention are intended to address.

[0002] SUMMARY

[0003] Described herein are systems and methods that can support an image signal processing apparatus, such as a camera system. The image signal processing apparatus includes a processing device, such as a field programmable gate array (FPGA) device, which operates to receive one or more image data from an image sensor via an image data interface. The processing device can forward the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data and save the compressed image data in a first storage medium. Furthermore, the processing device can export the received one or more image data to a second storage medium via a data communication interface.

BRIEF DESCRIPTION OF THE DRAWING

[0004] The novel features of the invention are set forth with particularity in the appended claims. A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description that sets forth illustrative embodiments, in which the principles of the invention are utilized, and the accompanying drawings of which:

[0005] Figure 1 is an exemplary illustration of an exemplary camera system, in accordance with various embodiments of the present invention.

[0006] Figure 2 is an exemplary illustration of a camera system that is capable of storing image data in parallel, in accordance with various embodiments of the present invention.

[0007] Figure 3 is an exemplary illustration of providing various interfaces in an image signal processing system for storing image data in parallel, in accordance with various embodiments of the present invention.

[0008] Figure 4 is an exemplary illustration of an alternative camera system that is capable

of storing image data in parallel, in accordance with various embodiments of the present invention.

[0009] Figure 5 is an exemplary illustration of providing various interfaces in an alternative image signal processing system for storing image data in parallel, in accordance with various embodiments of the present invention.

[0010] Figure 6 is an exemplary illustration of another alternative camera system that is capable of storing image data in parallel, in accordance with various embodiments of the present invention.

[0011] Figure 7 shows a flowchart of storing image data in parallel, in accordance with various embodiments of the present invention.

DETAILED DESCRIPTION

[0012] The invention is illustrated, by way of example and not by way of limitation, in the figures of the accompanying drawings in which like references indicate similar elements. It should be noted that references to "an" or "one" or "some" embodiment(s) in this disclosure are not necessarily to the same embodiment, and such references mean at least one.

[0013] The description of the invention as following uses a field-programmable gate array (FPGA) device as example for a processing device. It will be apparent to those skilled in the art that other types of processing devices can be used without limitation.

[0014] An Exemplary Camera System

[0015] Figure 1 is an exemplary illustration of a camera system, in accordance with various embodiments of the present invention. As shown in Figure 1, a camera system 100 includes various components such as a lens 101, an image sensor 102, and an image signal processor (ISP) 103. For example, the image sensor 102 can include a CCD/ CMOS device 109. Alternatively, the image sensor 102 can be based on an N-type metal-oxide-semiconductor (NMOS) device and other hybrids/variants thereof.

[0016] The image sensor 102 can convert light signals collected by a light collection device (e.g. the lens 101) into electric signals (e.g. analog signals). Then, an A/D converter 112 can convert the analog signals into the digital signals that can be processed by the ISP 103. Additionally, the ISP 103 can use a RAM 105 and a ROM 106 as data storage (e.g. for caching and buffering purposes).

[0017] As shown in Figure 1, the ISP 103 can receive from the image sensor 102 the image data that are generated by the image sensor 102 in raw data format. For example, the ISP 103 can receive the image data via a multi-path high-speed differential signal transporting interface, such as a low-voltage differential signaling (LVDS) interface and/or a sub-LVDS interface.

[0018] In accordance with various embodiments of the present invention, the image sensor 102 can generate a large amount of raw image data, which may overwhelm the camera

system 100 in real time. Thus, in order to accommodate for the limited processing and storage capability of the camera system 100, the ISP 103 may need to compress the raw image data before storing the compressed image data into the storage medium 104 (e.g. a memory card).

[0019] Storing Image Data in Parallel

[0020] Figure 2 is an exemplary illustration of a camera system that is capable of storing image data in parallel, in accordance with various embodiments of the present invention. As shown in Figure 2, a camera system 200 can include various components, such as a lens 201, an image sensor 202, and an image signal processor (ISP) 204. For example, the image sensor 202 can include a CCD/CMOS device 209. Alternatively, the image sensor 202 can be based on an N-type metal-oxide-semiconductor (NMOS) device and other hybrids/variants thereof.

[0021] The image sensor 202 can convert light signals collected by a light collection device (e.g. the lens 201) into electric signals (e.g. analog signals). Then, an A/D converter 212 can convert the analog signals into the digital signals that can be processed by the ISP 204.

[0022] As shown in Figure 2, the camera system 200 includes a processing device such as a field-programmable gate array (FPGA) device 203, which can receive the digital signals generated by the image sensor 202 (e.g. in an image data flow). Additionally, the FPGA device 203 can perform intermediate data processing tasks between the image sensor 202 and the ISP 204. Additionally, the ISP 204 can use a RAM 207 and a ROM 208 as data storage (e.g. for caching and buffering purposes).

[0023] In accordance with various embodiments of the present invention, the FPGA device 204 can include a data fan-out module 211, which can simultaneously forward the received digital image signals along multiple paths targeting different components within or outside of the camera system 200, e.g. via different modules (or units) on the FPGA device 204. Alternatively, the data fan-out module 211 can forward the received digital image signals toward the different components within or outside of the camera system 200 at different times.

[0024] As shown in Figure 2, the FPGA device 204 can use an I/O module 213 for transmitting the received digital image signals to the ISP 204. Then, the ISP 204 can compress the received raw image data and save the compressed image data into the storage medium 206 (e.g. a memory card).

[0025] Additionally, the FPGA device 204 can configure the serialization/deserialization (Serdes) module 212 for storing the received digital signals in a high speed storage medium 205, such as a solid state disk (SSD). The raw image data stored in the high speed storage medium 205 can provide more information than the compressed image data saved in the storage medium 206. Such information can be beneficial to

improving the handling of the image processing at late stage, such as assisting the professional photographic treatment of the images.

[0026] Figure 3 is an exemplary illustration of providing various interfaces in an image signal processing system for storing image data in parallel, in accordance with various embodiments of the present invention. As shown in Figure 3, an image signal processing system 300 can take advantage of a FPGA device 301 for processing and storing the raw image data 310. The FPGA device 301 can receive the raw image data 310 from an image sensor 309 via an image data interface 311.

[0027] For example, the image data interface 311 can be based on a serial scalable low-voltage signaling (SLVS), a serial mobile industry processor interface (MIPI) camera serial interface (CSI), a parallel sub-LVDS, a parallel low voltage complementary metal oxide semiconductor (LVCMOS), a fast YUV source, or other image data communication protocols.

[0028] In accordance with various embodiments of the present invention, the image data interface 311 can be configured to pass the raw image data 310 to the FPGA device 301 in a parallel fashion (e.g. with configuration options such as x2, x3, x4, x8, x12, x16 and more).

[0029] Furthermore, the FPGA device 301 can be initiated and configured (or reconfigured) using various information, such as instructions stored in the memory 305 (e.g. a flash memory). For example, depending on the type of the image sensor 309, the FPGA device 301 can be configured to support (or is adapted to) the image data interface 311, which is associated with any one of the above image data communication protocols.

[0030] As shown in Figure 3, the FPGA device 301 can include a data fan-out module 306, which can simultaneously forward the received raw digital image data 310 to a serialization/deserialization (Serdes) module 307 and an I/O module 308. Alternatively, the data fan-out module 306 can forward the received raw digital image data 310 to the Serdes module 307 and the I/O module 308 at different times. Also, the data fan-out module 306 can forward the received raw digital image data 310 to other targets or modules on the FPGA device 301 either simultaneously or at different times.

[0031] The FPGA device 301 can use the I/O module 308 for transmitting the received digital image signals to the ISP 302, via an image interface 312. The image interface 312 may have a similar configuration as the image data interface 311. Then, the ISP 302 can compress the received raw image data and save the compressed image data 314 into the storage medium 304.

[0032] Additionally, the FPGA device 301 can configure the Serdes module 307 to use a data communication protocol 313 for storing the received digital signals in a high speed storage medium 303, e.g. a solid state disk (SSD). For example, the data communication protocol 313 can be a high speed serial interfacing protocol, such as a

serial ATA (SATA) interface and/or a peripheral component interconnect express (PCIe) protocol.

[0033] In accordance with various embodiments of the present invention, the Serdes module 307 can convert the received raw image data from a configuration that supports the image data interface 311 to a different configuration that supports the data communication protocol 313 in real time. For example, the Serdes module 307 can convert the received raw image data, which are received in parallel, to support the data communication protocol 313, which may operates in a serial fashion.

[0034] Also as shown in Figure 3, the ISP 302 can reconfigure the image sensor 309 either directly via a control interface 316 or indirectly via the FPGA 301 (using a control interface 315). Then, the FPGA 301 can dynamically modify the I/O pin assignment and other configurations in order to accommodate for the configuration changes on the image sensor 309.

[0035] Figure 4 is an exemplary illustration of an alternative camera system that is capable of storing image data in parallel, in accordance with various embodiments of the present invention. As shown in Figure 4, a camera system 400 can include various components, such as a lens 401 and an image sensor 402. For example, the image sensor 402 can include a CCD/CMOS device 409. Alternatively, the image sensor 402 can be based on an N-type metal-oxide-semiconductor (NMOS) device and other hybrids/variants thereof.

[0036] The image sensor 402 can convert light signals collected by a light collection device (e.g. the lens 401) into electric signals, such as analog signals. Then, an A/D converter 410 can convert the analog signals into digital signals.

[0037] In accordance with various embodiments of the present invention, the camera system 400 includes a processing device such as a field-programmable gate array (FPGA) device 403. The FPGA device 403 can include a data fan-out module 411, which can simultaneously forward the received digital image signals to modules (or units) on the FPGA device 403, such as a serialization/deserialization (Serdes) module 412 and an image signal processing module 404. Alternatively, the data fan-out module 411 can forward the received raw digital image data 310 to the different modules at different times.

[0038] As shown in Figure 4, the FPGA device 403 can configure the Serdes module 412 for storing the received digital signals in a high speed storage medium 405, such as a solid state disk (SSD), via a data communication protocol.

[0039] Additionally, the FPGA device 403 can forward the received raw image data directly to an image signal processing module 404 on the FPGA device 403, which provides the functionality of an image signal processor (ISP). Then, the image signal processing module 404 on the FPGA device 403 can compress the received raw image data and

save the compressed image data in the storage medium 406 (e.g. a memory card).

[0040] Figure 5 is an exemplary illustration of providing various interfaces in an alternative image signal processing system for storing image data in parallel, in accordance with various embodiments of the present invention. As shown in Figure 5, an image signal processing system 500 can take advantage of a FPGA device 501 for processing and storing the raw image data 510.

[0041] For example, the image data interface 511 can be based on a serial scalable low-voltage signaling (SLVS), a serial mobile industry processor interface (MIPI) camera serial interface (CSI), a parallel sub-LVDS, a parallel low voltage complementary metal oxide semiconductor (LVCMOS), a fast YUV source, or other image data communication protocols.

[0042] Furthermore, the image data interface 511 can be configured to pass the raw image data 510 to the FPGA device 501 in a parallel fashion (e.g. with configuration options such as x2, x3, x4, x8, x12, x16 and more).

[0043] In accordance with various embodiments of the present invention, the FPGA device 501 can be initiated and configured (or reconfigured) using various information (e.g. instructions) stored in the memory 505 (e.g. a flash memory). For example, depending on the type of the image sensor 509, the FPGA device 501 can be configured to support different image data communication protocols associated with the image data interface 511.

[0044] As shown in Figure 5, the FPGA device 501 can include a data fan-out module 506, which can simultaneously forward the received raw digital image data 510 to different modules on the FPGA device 501. Alternatively, the data fan-out module 506 can forward the received raw digital image data 510 to the Serdes module 507 and the I/O module 508 at different times. Also, the data fan-out module 506 can forward the received raw digital image data 510 to other targets or modules on the FPGA device 501 either simultaneously or at different times.

[0045] The data fan-out module 506 can forward the received raw image data 510 to an image signal processing (ISP) module 508, which can compress the received raw image data and save the compressed image data 509 into the storage medium 504 (e.g. a memory card).

[0046] Also, the data fan-out module 506 can forward the received raw image to the Serdes module 507, which uses a data communication interface 512 for saving the raw image data into a high speed storage medium 503, e.g. a solid state disk (SSD). For example, the data communication protocol 512 can be a high speed serial interfacing protocol, such as a serial ATA (SATA) interface and/or a peripheral component interconnect express (PCIe) protocol.

[0047] In accordance with various embodiments of the present invention, the Serdes module

507 can convert the received raw image data from a configuration that supports the image data interface 511 to a different configuration that supports the data communication protocol 512 in real time. For example, the Serdes module 507 can convert the received raw image data, which are received in parallel, to support the data communication protocol 512, which may be in a serial fashion.

[0048] As shown in Figure 5, in real time, the FPGA 501 can reconfigure the image sensor 502 via a control interface 513. Also, the FPGA 501 can dynamically modify the I/O pin assignment and other configurations in order to accommodate for such changes on the image sensor 502.

[0049] Figure 6 is an exemplary illustration of another alternative camera system that is capable of storing image data in parallel, in accordance with various embodiments of the present invention. As shown in Figure 6, a camera system 600 can include various components, such as a lens 601 and an image sensor 602. For example, the image sensor 602 can include a CCD/CMOS device 609. Alternatively, the image sensor 602 can be based on an N-type metal-oxide-semiconductor (NMOS) device and other hybrids/variants thereof.

[0050] The image sensor 602 can convert light signals collected by a light collection device (e.g. the lens 601) into electric signals, such as analog signals. Then, an A/D converter 610 can convert the analog signals into digital signals.

[0051] As shown in Figure 6, the camera system 600 includes a processing device such as an integrated processor 603, which uses a RAM 607 and a ROM 608 as data storage (e.g. for caching and buffering purposes). The integrated processor 603 can include different ASIC units, such as a data fan-out unit 611, a serialization/deserialization (Serdes) unit 612, an image signal processing unit 604, and a graphic processing unit 605.

[0052] The data fan-out unit 611 can simultaneously forward the received digital image signals along multiple paths, e.g. via different units on the integrated processor 603. Alternatively, the data fan-out unit 611 can forward the received raw digital image data to the Serdes unit 612 and the image signal processing unit 604 at different times.

[0053] As shown in Figure 6, the Serdes unit 612 can store the received digital signals into a high speed storage medium 205, such as a solid state disk (SSD), via a data communication protocol. The image signal processing unit 604 can compress the received raw image data and save the compressed image data into the storage medium 606 (e.g. a memory card).

[0054] Additionally, the graphic processing unit 605 can receive the raw and processed image data from the data fan-out unit 611 and/or the image signal processing unit 604, and perform various graphic processing tasks. Additionally, the graphic processing unit 605 can save the processed graphic information in either the storage medium 606 or the high speed storage medium 605 and provides the graphic information to other

components within or outside of the camera system 600.

[0055] Figure 7 shows a flowchart of storing image data in parallel, in accordance with various embodiments of the present invention. As shown in Figure 7, at step 701, a processing device can receive one or more image data from an image sensor. Then, at step 702, the processing device can forward the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data into compressed image data before saving the compressed image data in a first storage medium. Furthermore, at step 703, the processing device can export the received one or more image data to a second storage medium.

[0056] Many features of the present invention can be performed in, using, or with the assistance of hardware, software, firmware, or combinations thereof. Consequently, features of the present invention may be implemented using a processing system (e.g., including one or more processors). Exemplary processors can include, without limitation, one or more general purpose microprocessors (for example, single or multi-core processors), application-specific integrated circuits, application-specific instruction-set processors, graphics processing units, physics processing units, digital signal processing units, coprocessors, network processing units, audio processing units, encryption processing units, and the like.

[0057] Features of the present invention can be implemented in, using, or with the assistance of a computer program product which is a storage medium (media) or computer readable medium (media) having instructions stored thereon/in which can be used to program a processing system to perform any of the features presented herein. The storage medium can include, but is not limited to, any type of disk including floppy disks, optical discs, DVD, CD-ROMs, microdrive, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, DRAMs, VRAMs, flash memory devices, magnetic or optical cards, nanosystems (including molecular memory ICs), or any type of media or device suitable for storing instructions and/or data.

[0058] Stored on any one of the machine readable medium (media), features of the present invention can be incorporated in software and/or firmware for controlling the hardware of a processing system, and for enabling a processing system to interact with other mechanism utilizing the results of the present invention. Such software or firmware may include, but is not limited to, application code, device drivers, operating systems and execution environments/containers.

[0059] Features of the invention may also be implemented in hardware using, for example, hardware components such as application specific integrated circuits (ASICs) and field-programmable gate array (FPGA) devices. Implementation of the hardware state machine so as to perform the functions described herein will be apparent to persons

skilled in the relevant art.

[0060] Additionally, the present invention may be conveniently implemented using one or more conventional general purpose or specialized digital computer, computing device, machine, or microprocessor, including one or more processors, memory and/or computer readable storage media programmed according to the teachings of the present disclosure. Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those skilled in the software art.

[0061] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention.

[0062] The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have often been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the invention.

[0063] The foregoing description of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. The breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments. Many modifications and variations will be apparent to the practitioner skilled in the art. The modifications and variations include any relevant combination of the disclosed features. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications that are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalence.

Claims

[Claim 1] An image signal processing method, comprising:
receiving one or more image data from an image sensor;
forwarding, via a processing device, the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data and save the compressed image data in a first storage medium; and
exporting the received one or more image data to a second storage medium.

[Claim 2] The image processing method of Claim 1, further comprising:
providing a data fan-out module on the processing device, wherein the data fan-out module operates to forward the received one or more image data to different modules on the processing device.

[Claim 3] The image processing method of Claim 2, further comprising:
forwarding, via an input/out (I/O) module on the processing device, the received one or more image data to the image signal processor; and
exporting, via a serializer/deserializer (Serdes) module on the processing device, the received one or more image data to the second storage medium, which is a high speed storage medium.

[Claim 4] The image processing method of Claim 1, further comprising: using an image data interface to receive the one or more image data from the image sensor, wherein the image data interface is based on a protocol that is selected from a group of image data communication protocols.

[Claim 5] The image processing method of Claim 1, further comprising: using a data communication interface to export the received one or more image data to the second storage medium, wherein the data communication interface is based on a protocol that is selected from a group of high speed serial interfacing protocols.

[Claim 6] The image processing method of Claim 1, further comprising:
converting the received one or more image data from a first configuration, which supports an image data interface for the image sensor, to a second configuration, which supports a data communication interface for a high speed data storage.

[Claim 7] The image processing method of Claim 1, further comprising: using, via the image signal processor, a control interface to reconfigure the image sensor.

[Claim 8] The image processing method of Claim 1, wherein: said processing

device is a field programmable gate array (FPGA) device.

[Claim 9] The image processing method of Claim 8, further comprising: providing an input/output (I/O) pin assignment to the FPGA device in order to support a configuration for the image sensor.

[Claim 10] The image processing method of Claim 1, wherein: the image signal processor (ISP) is an image signal processing module in the processing device.

[Claim 11] The image processing method of Claim 1, wherein: the processing device is an integrated processor, which includes a graphic processing unit (GPU).

[Claim 12] The image processing method of Claim 1, further comprising: receiving the one or more image data in an image data flow, which includes a plurality of frames of images.

[Claim 13] The image processing method of Claim 1, further comprising: including the processing device in a high resolution cinema camera, wherein the one or more image data received by the processing device is in a raw image data format.

[Claim 14] The image processing method of Claim 1, wherein: the first storage medium includes a memory card and the second storage medium includes a solid state disk (SSD).

[Claim 15] An image signal processing apparatus, comprising:
a processing device, wherein the processing device operates to
receive one or more image data from an image sensor;
forward the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data and save the compressed image data in a first storage medium; and
export the received one or more image data to a second storage medium.

[Claim 16] The image processing apparatus of Claim 15, further comprising: a data fan-out module on the processing device, wherein the data fan-out module operates to forward the received one or more image data to different modules on the processing device.

[Claim 17] The image processing apparatus of Claim 16, wherein: the processing device includes an input/out (I/O) module, which operates to forward the received one or more image data to the image signal processor; and a serializer/deserializer (Serdes) module, which operates to export the received one or more image data to the second storage medium, which

is a high speed storage medium.

[Claim 18] The image processing apparatus of Claim 15, further comprising: an image data interface to receive the one or more image data from the image sensor, wherein the image data interface is based on a protocol that is selected from a group of image data communication protocols.

[Claim 19] The image processing apparatus of Claim 15, further comprising: a data communication interface to export the received one or more image data to the second storage medium, wherein the data communication interface is based on a protocol that is selected from a group of high speed serial interfacing protocols.

[Claim 20] The image processing apparatus of Claim 15, wherein: the processing device operates to convert the received one or more image data from a first configuration, which supports an image data interface for the image sensor, to a second configuration, which supports a data communication interface for a high speed data storage.

[Claim 21] The image processing apparatus of Claim 15, wherein: the image signal processor use a control interface to reconfigure the image sensor.

[Claim 22] The image processing method of Claim 1, wherein: said processing device is a field programmable gate array (FPGA) device.

[Claim 23] The image processing method of Claim 8, wherein: the FPGA device operates to use an input/output (I/O) pin assignment in order to support a configuration for the image sensor.

[Claim 24] The image processing method of Claim 1, wherein: the image signal processor (ISP) is an image signal processing module in the processing device.

[Claim 25] The image processing method of Claim 1, wherein: the processing device is an integrated processor, which includes a graphic processing unit (GPU).

[Claim 26] The image processing method of Claim 1, wherein: the processing device operates to receive the one or more image data in an image data flow, which includes a plurality of frames of images.

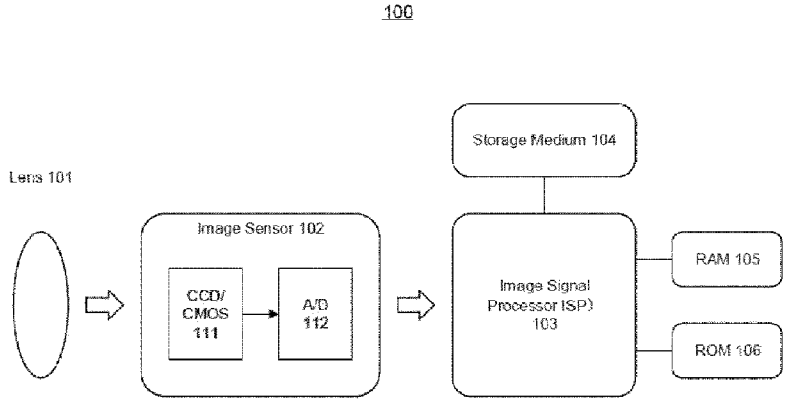
[Claim 27] The image processing method of Claim 1, wherein: the processing device is part of a high resolution cinema camera, wherein the one or more image data received by the processing device is in a raw image data format.

[Claim 28] The image processing method of Claim 1, wherein: the first storage medium includes a memory card and the second storage medium includes a solid state disk (SSD).

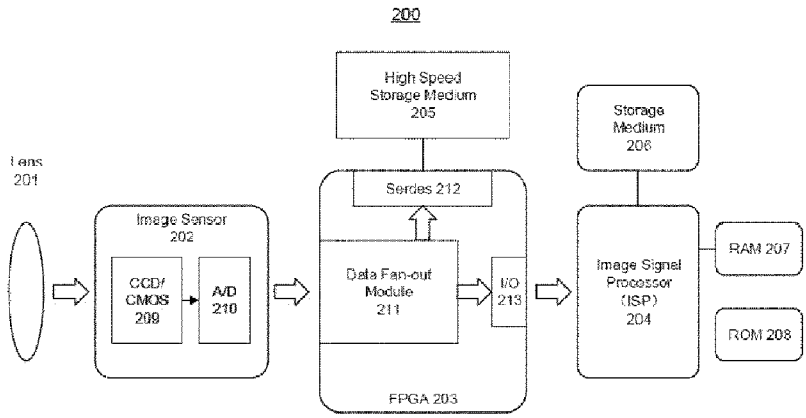
[Claim 29] A non-transitory computer-readable medium with instructions stored thereon, that when executed by a processor, perform the steps comprising:
receiving one or more image data from an image sensor;
forwarding, via a processing device, the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data and save the compressed image data in a first storage medium; and
exporting the received one or more image data to a second storage medium.

[Claim 30] A camera system, comprising:
an image sensor, which is coupled to a lens, operates to generate one or more image data; and
a processing device operates to
receive one or more image data from an image sensor;
forward the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data and save the compressed image data in a first storage medium; and
export the received one or more image data to a second storage medium.

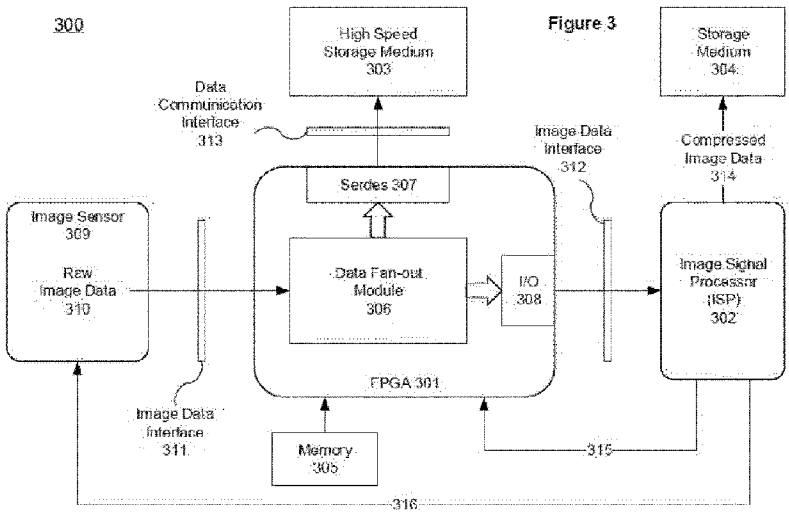
[Fig. 1]


100
Storage Medium 104
Lens 101
Image Sensor 102
CCD/ CMOS 111
A/D 112
Image Signal Processor ISP) 103
RAM 105
ROM 106

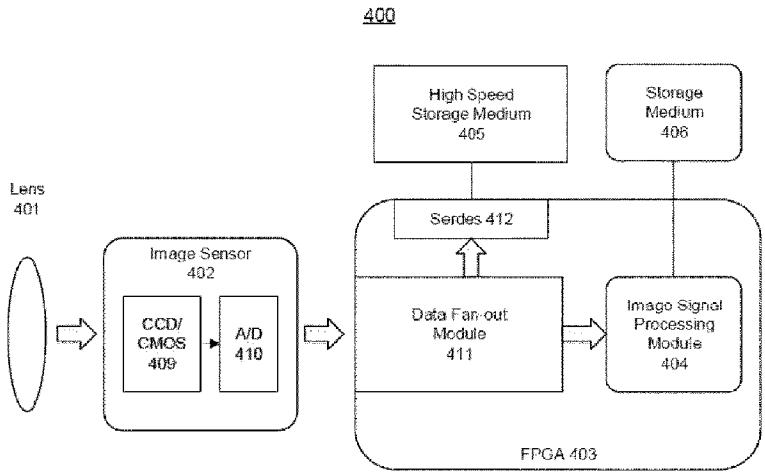
[Fig. 2]


200
High Speed Storage Medium 205
Storage Medium 206
Lens 201
Serdes 212
Image Sensor 202
CCD/ CMOS 209
A/D 210
Data Fan-out Module 211
I/O 213
Image Signal Processor (ISP) 204
RAM 207
ROM 208
FPGA 203

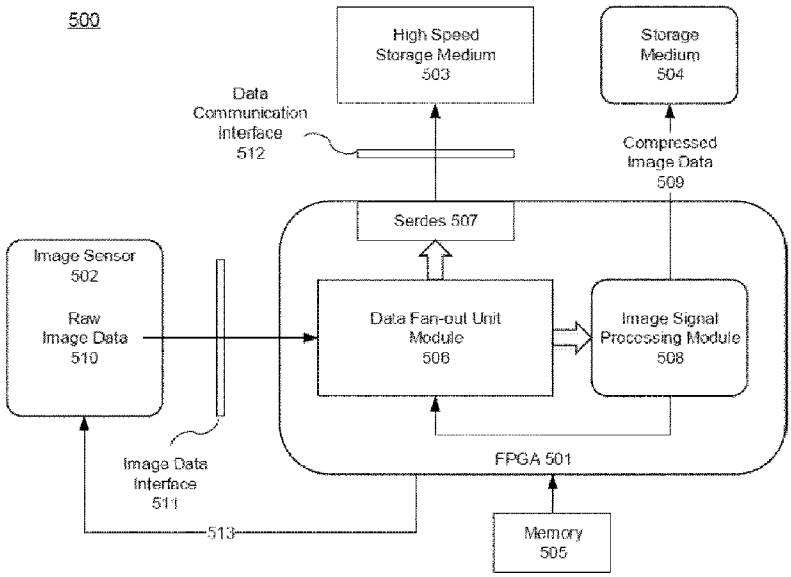
[Fig. 3]


300
High Speed Storage Medium 303
Figure 3
Storage Medium 304
Data Communication Interface 313
Image Data Interface 312
Compressed Image Data 314
Serdes 307
Image Sensor 309
Raw Image Data 310
Data Fan-out Module 306
I/O 308
Image Signal Processor (ISP) 302
FPGA 301
Image Data Interface 311
Memory 305
315
316

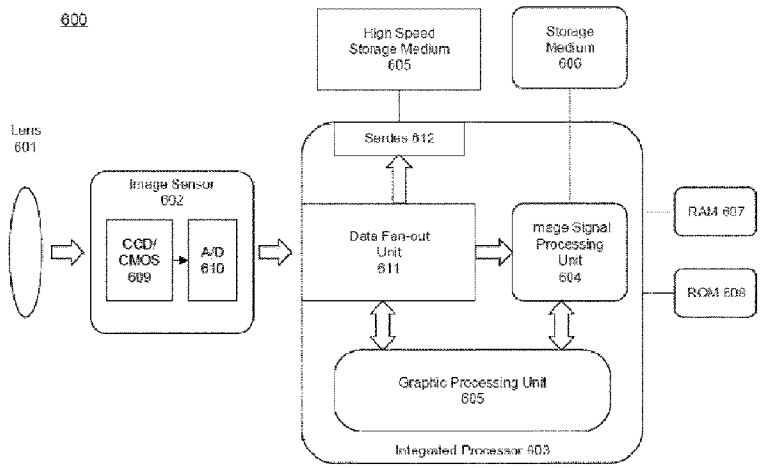
[Fig. 4]


400
High Speed Storage Medium 405
Storage Medium 406
Lens 401
Serdes 412
Image Sensor 402
CCD/ CMOS 409
A/D 410
Data Fan-out Module 411
Image Signal Processing Module 404
FPGA 403

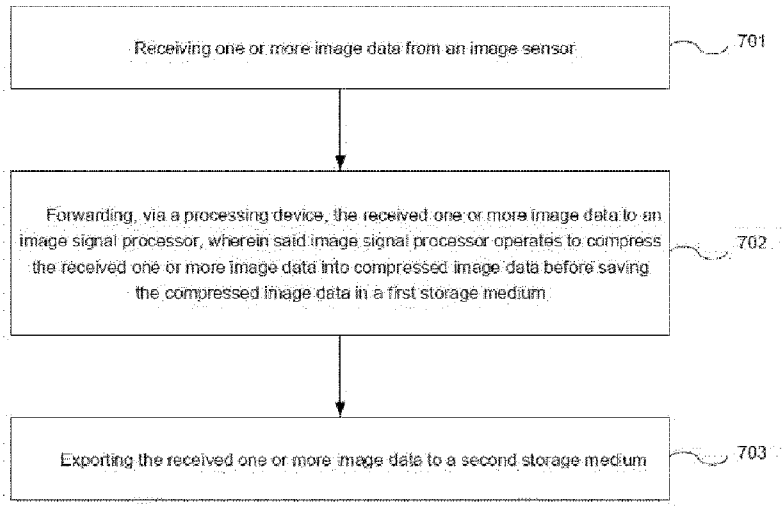
[Fig. 5]


500
High Speed Storage Medium 503
Storage Medium 504
Data Communication Interface 512
Compressed Image Data 509
Serdes 507
Image Sensor 502
Raw Image Data 510
Data Fan-out Unit Module 506
Image Signal Processing Module 508
Image Data Interface 511
FPGA 501
513
Memory 505

[Fig. 6]


600
High Speed Storage Medium 605
Storage Medium 606
Lens 601
Image Sensor 602
CCD/ CMOS 609
A/D 610
Sensor 612
Data Fan-out Unit 611
Image Signal Processing Unit 604
RAM 607
ROM 608
Graphic Processing Unit 605
Integrated Processor 603

[Fig. 7]


Receiving one or more image data from an image sensor
701
Forwarding, via a processing device, the received one or more image data to an image signal processor, wherein said image signal processor operates to compress the received one or more image data into compressed image data before saving the compressed image data in a first storage medium
702
Exporting the received one or more image data to a second storage medium
703

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/076013

A. CLASSIFICATION OF SUBJECT MATTER

G06T 5/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06T; H04N; G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT;WPI;EPODOC;GOOGLE;CNKI;ISI;Patentics: image?, picture?, compress+, stor+, memory, first, second, parallel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 103247035 A (CHONGQING UNIVERSITY OF POSTS AND TELECOMMUNICATIONS) 14 August 2013 (2013-08-14) paragraphs [0045]-[0051] and figure 2	1-2, 8, 10-16, 22, 24-30
A	KR 20050112998 A (PANTECH CO., LTD.) 01 December 2005 (2005-12-01) the whole document	1-30
A	US 2002081104 A1 (SHIMIZU, TETSUYA) 27 June 2002 (2002-06-27) the whole document	1-30
A	US 2002001410 A1 (HAGIWARA, SHINICHI) 03 January 2002 (2002-01-03) the whole document	1-30

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 June 2015	**17 July 2015**
Name and mailing address of the ISA/CN **STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer **ZHANG,Linlin** Telephone No. **(86-10)82245951**

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2015/076013

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KR	20050112998	A	01 December 2005	None			
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				JP	4454837	B2	21 April 2010
				JP	2002176611	A	21 June 2002
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				JP	2002016870	A	18 January 2002
				US	6990240	B2	24 January 2006