(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 March 2023 (23.03.2023)

WIPO | PCT

(10) International Publication Number
WO 2023/039830 A1

(51) International Patent Classification:
G09G 3/32 (2016.01) *H01L 27/32* (2006.01)

(21) International Application Number:
PCT/CN2021/119060

(22) International Filing Date:
17 September 2021 (17.09.2021)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicants: **BOE TECHNOLOGY GROUP CO., LTD.** [CN/CN]; No.10 Jiuxianqiao Rd., Chaoyang District, Beijing 100015 (CN). **CHENGDU BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.** [CN/CN]; No.1188 Hezuo Rd., (West Zone), Hi-Tech Development Zone, Chengdu, Sichuan 611731 (CN).

(72) Inventors: **WANG, Rui**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **ZENG, Chao**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **HU, Ming**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **QIU, Haijun**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **HUANG, Weiyun**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **CHENG, Tianyi**; No.9 Dize Rd., BDA, Beijing 100176 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: PIXEL DRIVING CIRCUIT,ARRAY SUBSTRATE AND DISPLAY APPARATUS

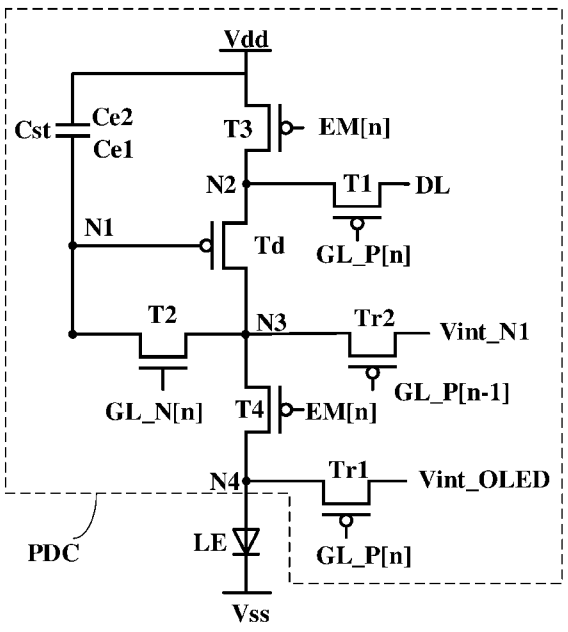

FIG. 2

(57) Abstract: A pixel driving circuit (PDC), an array substrate and a display apparatus are provided. The pixel driving circuit (PDC) includes a driving transistor (Td); a storage capacitor (Cst); a first reset transistor (Tr1) having a gate electrode connected to a first gate line (GL_P[n]) in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line (Vint_OLED) of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element (LE); and a second reset transistor (Tr2) having a gate electrode connected to a first gate line (GL_P[n-1]) in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line (Vint_N1) of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor (Td).

WO 2023/039830 A1

PIXEL DRIVING CIRCUIT,ARRAY SUBSTRATE AND DISPLAY APPARATUS

TECHNICAL FIELD

[0001] The present invention relates to display technology, more particularly, to an array substrate and a display apparatus.

BACKGROUND

[0002] Organic Light Emitting Diode (OLED) display is one of the hotspots in the field of flat panel display research today. Unlike Thin Film Transistor-Liquid Crystal Display (TFT-LCD), which uses a stable voltage to control brightness, OLED is driven by a driving current required to be kept constant to control illumination. The OLED display panel includes a plurality of pixel units configured with pixel-driving circuits arranged in multiple rows and columns. Each pixel-driving circuit includes a driving transistor having a gate terminal connected to one gate line per row and a drain terminal connected to one data line per column. When the row in which the pixel unit is gated is turned on, the switching transistor connected to the driving transistor is turned on, and the data voltage is applied from the data line to the driving transistor via the switching transistor, so that the driving transistor outputs a current corresponding to the data voltage to an OLED device. The OLED device is driven to emit light of a corresponding brightness.

SUMMARY

[0003] In one aspect, the present disclosure provides a pixel driving circuit, comprising a driving transistor; a storage capacitor; a first reset transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element; and a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor.

[0004] Optionally, the first gate line in the previous stage is connected to the gate electrode of the second reset transistor in the present stage and a gate electrode of a first reset transistor in the previous stage; and the first gate line in the present stage is connected to the gate electrode of the first reset transistor in the present stage and a gate electrode of a second reset transistor in a next stage.

[0005] Optionally, the pixel driving circuit further comprises a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the

driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element.

[0006] Optionally, the first gate line in the present stage comprises a first gate line first branch and a first gate line second branch configured to be provided with a same gate scanning signal; the gate electrode of the first reset transistor is connected to the first gate line second branch in the present stage; and the gate electrode of the second reset transistor is connected to the first gate line second branch in the previous stage.

[0007] Optionally, the pixel driving circuit further comprises a first transistor having a gate electrode connected to the first gate line first branch in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor.

[0008] Optionally, the pixel driving circuit further comprises a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to a first capacitor electrode of the storage capacitor and a gate electrode of the driving transistor, and a drain electrode connected to a drain electrode of the driving transistor; wherein the plurality of first gate lines and the plurality of second gate lines are spaced apart by one or more insulating layer.

[0009] Optionally, the respective second gate line in a present stage comprises a second gate line first branch and a second gate line second branch in two different layers.

[0010] Optionally, the pixel driving circuit further comprises a second reset transistor having a gate electrode connected to a first gate line in a previous stage of a plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; a first transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor; a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to the first capacitor electrode of the storage capacitor and the gate electrode of the driving transistor, and a drain electrode connected to the drain electrode of the driving transistor; a third transistor having a gate electrode connected to a respective light emitting control signal line of a plurality of light emitting control signal lines, a source electrode connected to a respective voltage supply line of a plurality of voltage supply lines, and a drain electrode connected to the source electrode of the driving transistor and the drain electrode of the first transistor; and a fourth transistor having a gate electrode connected to the respective light emitting control signal line, a source electrode connected to drain electrodes of the driving transistor and the second transistor, and a

drain electrode connected to an anode of a light emitting element; wherein a second capacitor electrode of the storage capacitor is connected to the respective voltage supply line and the source electrode of the third transistor.

[0011] In another aspect, the present disclosure provides an array substrate, comprising the pixel driving circuit described herein, and the light emitting element connected to the pixel driving circuit.

[0012] Optionally, the pixel driving circuit further comprises a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; the first gate line in the previous stage is connected to the gate electrode of the second reset transistor in the present stage and a gate electrode of a first reset transistor in the previous stage; and the first gate line in the present stage is connected to the gate electrode of the first reset transistor in the present stage and a gate electrode of a second reset transistor in a next stage.

[0013] Optionally, the pixel driving circuit further comprises a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element.

[0014] Optionally, the first gate line in the present stage comprises a first gate line first branch and a first gate line second branch configured to be provided with a same gate scanning signal; the gate electrode of the first reset transistor is connected to the first gate line second branch in the present stage; and the gate electrode of the second reset transistor is connected to the first gate line second branch in the previous stage.

[0015] Optionally, the pixel driving circuit further comprises a first transistor having a gate electrode connected to the first gate line first branch in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor.

[0016] Optionally, the pixel driving circuit further comprises a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to a first capacitor electrode of the storage capacitor and a gate electrode of the driving transistor, and a drain electrode connected to a drain electrode of the driving transistor; and the plurality of first gate lines and the plurality of second gate lines are spaced apart by one or more insulating layer.

[0017] Optionally, the array substrate comprises a base substrate; a first semiconductor material layer on the base substrate; an insulating layer on a side of the first semiconductor material layer away from the base substrate; and a second semiconductor material layer on a side of the insulating layer away from the first semiconductor material layer; wherein the first semiconductor material layer comprises an active layer of the driving transistor and an active layer of the first reset transistor; and the second semiconductor material layer comprises an active layer of the second transistor.

[0018] Optionally, the first semiconductor material layer further comprises at least a portion of the source electrode of the driving transistor, at least a portion of the drain electrode of the driving transistor, at least a portion of the source electrode of the first reset transistor, at least a portion of the drain electrode of the first reset transistor; and the second semiconductor material layer further comprises at least a portion of the source electrode of the second transistor, and at least a portion of the drain electrode of the second transistor.

[0019] Optionally, the first semiconductor material layer comprises active layers, at least portions of source electrodes, and at least portions of drain electrodes of all transistors other than the second transistor in the pixel driving circuit.

[0020] Optionally, the first semiconductor material layer comprises a polycrystalline silicon material; and the second semiconductor material layer comprises a metal oxide semiconductor material.

[0021] Optionally, the respective second gate line in a present stage comprises a second gate line first branch and a second gate line second branch in two different layers; and an orthographic projection of the second gate line first branch on a base substrate at least partially overlaps with an orthographic projection of the second gate line second branch on the base substrate.

[0022] Optionally, the array substrate comprises a base substrate; a second gate metal layer on the base substrate; a first inter-layer dielectric layer on a side of the second gate metal layer away from the base substrate; a second semiconductor material layer on a side of the first inter-layer dielectric layer away from the second gate metal layer; a second inter-layer dielectric layer on a side of the second semiconductor material layer away from the first inter-layer dielectric layer; and a third gate metal layer on a side of the second inter-layer dielectric layer away from the second semiconductor material layer; wherein the second gate metal layer comprises the second gate line first branch; the second semiconductor material layer comprises an active layer of the second transistor; and the third gate metal layer comprises the second gate line second branch.

[0023] Optionally, the array substrate further comprises a base substrate; a first gate metal layer on the base substrate, the first gate metal layer comprising a first capacitor electrode of

the storage capacitor; a second semiconductor material layer on a side of the first gate metal layer away from the base substrate, the second semiconductor material layer comprising at least a portion of a source electrode of the second transistor; and a first signal line layer on a side of the second semiconductor material layer away from the first gate metal layer, the first signal line layer comprising the plurality of first reset signal lines and a first node connecting line; wherein the first node connecting line is connected to the first capacitor electrode through a first via, and connected to the source electrode of the second transistor through a second via.

[0024] Optionally, the first node connecting line crosses over the respective second gate line in the present stage.

[0025] Optionally, the pixel driving circuit further comprises a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; and a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element; wherein the array substrate further comprises a base substrate; a first semiconductor material layer on the base substrate, the first semiconductor material layer comprising the drain electrode of the second reset transistor, the source electrode of the fourth transistor, and the drain electrode of the driving transistor; a second semiconductor material layer on a side of the first semiconductor material layer away from the base substrate, the second semiconductor material layer comprising the drain electrode of the second transistor; and a first signal line layer on a side of the second semiconductor material layer away from the first gate metal layer, the first signal line layer comprising the plurality of first reset signal lines and a second node connecting line; wherein the second node connecting line is connected to the drain electrode of the second transistor through a third via, connected to the drain electrode of the second reset transistor through a fourth via, and connected to the source electrode of the fourth transistor and the drain electrode of the driving transistor through a fifth via.

[0026] Optionally, the second node connecting line crosses over the respective second gate line in the present stage and a first gate line first branch of the first gate line in the present stage.

[0027] Optionally, the array substrate comprises a base substrate; a second semiconductor material layer on a side of the insulating layer away from the first semiconductor material layer, the second semiconductor material layer comprising an active layer of the second transistor; and a second signal line layer on a side of the second semiconductor material layer away from the base substrate, the second signal line layer comprising a plurality of voltage supply lines; wherein an orthographic projection of a respective voltage supply line of the plurality of

voltage supply lines on the base substrate covers an orthographic projection of the active layer of the second transistor on the base substrate.

[0028] Optionally, the orthographic projection of a respective voltage supply line of the plurality of voltage supply lines on the base substrate further covers an orthographic projection of the source electrode or drain electrode of the second transistor on the base substrate.

[0029] Optionally, voltage supply lines respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure in which the voltage supply lines are connected to each other in a region where orthographic projections of voltage supply lines on the base substrate cover orthographic projections of active layers of second transistors from the first pixel driving circuit and the second pixel driving circuit on the base substrate.

[0030] Optionally, the pixel driving circuit further comprises a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; and wherein second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure in which source or drain electrodes of the second reset transistors are connected to each other in a region where the respective second reset signal line is connected to the source or drain electrodes of the second reset transistors through one or more vias.

[0031] Optionally, a part of the second reset transistor in the first semiconductor material layer is spaced apart from other transistors in a same pixel driving circuit; second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure; and source or drain electrodes of the second reset transistors respectively from the first pixel driving circuit and the second pixel driving circuit directly adjacent to each other and in the present stage are connected to each other, thereby forming the unitary structure.

[0032] Optionally, the respective second reset signal line is connected to the source or drain electrodes of the second reset transistors through a single via.

[0033] Optionally, corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit directly adjacent to each other and in the present stage have a substantially mirror symmetry with respect to each other.

[0034] Optionally, corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit directly adjacent to each other and in the present stage have a substantially translational symmetry.

[0035] In another aspect, the present disclosure provides a display apparatus, comprising the array substrate described herein, and an integrated circuit connected to the array substrate.

BRIEF DESCRIPTION OF THE FIGURES

[0036] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0037] FIG. 1 is a plan view of an array substrate in some embodiments according to the present disclosure.

[0038] FIG. 2 is a circuit diagram illustrating the structure of a pixel driving circuit in some embodiments according to the present disclosure.

[0039] FIG. 3A is a diagram illustrating the structure of two adjacent pixel driving circuits in an array substrate in some embodiments according to the present disclosure.

[0040] FIG. 3B is a diagram illustrating the structure of a first semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0041] FIG. 3C is a diagram illustrating the structure of a first gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0042] FIG. 3D is a diagram illustrating the structure of a second gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0043] FIG. 3E is a diagram illustrating the structure of a second semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0044] FIG. 3F is a diagram illustrating the structure of a third gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0045] FIG. 3G is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate depicted in FIG. 3A.

[0046] FIG. 3H is a diagram illustrating vias extending through a passivation layer and a second inter-layer dielectric layer in an array substrate depicted in FIG. 3A.

[0047] FIG. 3I is a diagram illustrating the structure of a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0048] FIG. 3J is a diagram illustrating vias extending through a first planarization layer in an array substrate depicted in FIG. 3A.

[0049] FIG. 3K is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate depicted in FIG. 3A.

[0050] FIG. 3L is a diagram illustrating the structure of a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0051] FIG. 3M is a diagram illustrating vias extending through a second planarization layer in an array substrate depicted in FIG. 3A.

[0052] FIG. 3N is a diagram illustrating the structure of an anode layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0053] FIG. 3O is a diagram illustrating the structure of a pixel definition layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0054] FIG. 4A is a cross-sectional view along an A-A' line in FIG. 3A.

[0055] FIG. 4B is a cross-sectional view along a B-B' line in FIG. 3A.

[0056] FIG. 4C is a cross-sectional view along a C-C' line in FIG. 3A.

[0057] FIG. 4D is a cross-sectional view along a D-D' line in FIG. 3A.

[0058] FIG. 5A is a diagram illustrating the structure of two adjacent pixel driving circuits in an array substrate in some embodiments according to the present disclosure.

[0059] FIG. 5B is a diagram illustrating the structure of a first semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0060] FIG. 5C is a diagram illustrating the structure of a first gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0061] FIG. 5D is a diagram illustrating the structure of a second gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0062] FIG. 5E is a diagram illustrating the structure of a second semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0063] FIG. 5F is a diagram illustrating the structure of a third gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0064] FIG. 5G is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate depicted in FIG. 5A.

[0065] FIG. 5H is a diagram illustrating vias extending through a passivation layer and a second inter-layer dielectric layer in an array substrate depicted in FIG. 5A.

[0066] FIG. 5I is a diagram illustrating the structure of a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0067] FIG. 5J is a diagram illustrating vias extending through a first planarization layer in an array substrate depicted in FIG. 5A.

[0068] FIG. 5K is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate depicted in FIG. 5A.

[0069] FIG. 5L is a diagram illustrating the structure of a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0070] FIG. 5M is a diagram illustrating vias extending through a second planarization layer in an array substrate depicted in FIG. 5A.

[0071] FIG. 5N is a diagram illustrating the structure of an anode layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0072] FIG. 5O is a diagram illustrating the structure of a pixel definition layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0073] FIG. 6A is a cross-sectional view along a E-E' line in FIG. 5A.

[0074] FIG. 6B is a cross-sectional view along an F-F' line in FIG. 5A.

[0075] FIG. 6C is a cross-sectional view along a G-G' line in FIG. 5A.

[0076] FIG. 6D is a cross-sectional view along an H-H' line in FIG. 5A.

[0077] FIG. 7A is a diagram illustrating the structure of a first semiconductor material layer, a first gate metal layer, a second gate metal layer, a second semiconductor material layer, a third gate metal layer, and a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0078] FIG. 7B is a diagram illustrating the structure of a first signal line layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0079] FIG. 7C is a diagram illustrating the structure of a second semiconductor material layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0080] FIG. 8A is a diagram illustrating the structure of a first semiconductor material layer, a first gate metal layer, a second gate metal layer, a second semiconductor material layer, a third gate metal layer, and a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0081] FIG. 8B is a diagram illustrating the structure of a first signal line layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0082] FIG. 8C is a diagram illustrating the structure of a second semiconductor material layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

DETAILED DESCRIPTION

[0083] The disclosure will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0084] The present disclosure provides, *inter alia*, an array substrate and a display apparatus that substantially obviate one or more of the problems due to limitations and disadvantages of the related art. In one aspect, the present disclosure provides an array substrate. In some embodiments, the array substrate includes a pixel driving circuit and the light emitting element connected to the pixel driving circuit. In some embodiments, the pixel driving circuit includes a driving transistor; a storage capacitor; a first reset transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element; and a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor.

[0085] It should be noted that in embodiments according to the present disclosure, a source electrode or a drain electrode refers to one of a first terminal and a second terminal of a transistor, the first terminal and the second terminal being connected to an active layer of the transistor. A direction of a current flowing through the transistor may be configured to be from a source electrode to a drain electrode, or from a drain electrode to a source electrode. Accordingly, depending on the direction of the current flowing through the transistor, in one example, the source electrode is configured to receive an input signal and the drain electrode is configured to output an output signal; in another example, the drain electrode is configured to receive an input signal and the source electrode is configured to output an output signal.

[0086] Various appropriate pixel driving circuits may be used in the present array substrate. Examples of appropriate driving circuits include 3T1C, 2T1C, 4T1C, 4T2C, 5T2C, 6T1C, 7T1C, 7T2C, 8T1C, and 8T2C. In some embodiments, the respective one of the plurality of pixel driving circuits is an 7T1C driving circuit. Various appropriate light emitting elements

may be used in the present array substrate. Examples of appropriate light emitting elements include organic light emitting diodes, quantum dots light emitting diodes, and micro light emitting diodes. Optionally, the light emitting element is micro light emitting diode. Optionally, the light emitting element is an organic light emitting diode including an organic light emitting layer.

[0087] FIG. 1 is a plan view of an array substrate in some embodiments according to the present disclosure. Referring to FIG. 1, the array substrate includes an array of subpixels Sp. Each subpixel includes an electronic component, e.g., a light emitting element. In one example, the light emitting element is driven by a respective pixel driving circuit PDC. The array substrate includes a plurality of first gate lines GL1, a plurality of second gate lines GL2, a plurality of data lines DL, a plurality of voltage supply line Vdd, and a respective second voltage supply line (e.g., a low voltage supply line Vss). Light emission in a respective subpixel sp is driven by a respective pixel driving circuit PDC. In one example, a high voltage signal (e.g., a VDD signal) is input, through the respective high voltage supply line of the plurality of voltage supply line Vdd, to the respective pixel driving circuit PDC connected to an anode of the light emitting element; a low voltage signal (e.g., a VSS signal) is input, through a low voltage supply line Vss, to a cathode of the light emitting element. A voltage difference between the high voltage signal (e.g., the VDD signal) and the low voltage signal (e.g., the VSS signal) is a driving voltage ΔV that drives light emission in the light emitting element.

[0088] FIG. 2 is a circuit diagram illustrating the structure of a pixel driving circuit in some embodiments according to the present disclosure. Referring to FIG. 2, in some embodiments, the pixel driving circuit includes a driving transistor Td; a storage capacitor Cst having a first capacitor electrode Ce1 and a second capacitor electrode Ce2; a second reset transistor Tr2 having a gate electrode connected to a first gate line GL_P[n-1] in a previous stage of a plurality of first gate lines, a source electrode connected to a respective second reset signal line Vint_N1 of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor Td; a first transistor T1 having a gate electrode connected to a first gate line GL_P[n] in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line DL of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor Td; a second transistor T2 having a gate electrode connected to a respective second gate line GL_N[n] in a present stage of a plurality of second gate lines, a source electrode connected to the first capacitor electrode Ce1 of the storage capacitor Cst and the gate electrode of the driving transistor Td, and a drain electrode connected to the drain electrode of the driving transistor Td; a third transistor T3 having a gate electrode connected to a respective light emitting control signal line EM[n] of a plurality of light emitting control signal lines, a source electrode connected to a respective voltage supply line Vdd of a plurality of voltage supply lines, and a drain electrode connected to the source electrode of the driving transistor Td and the drain electrode of the first transistor

T1; a fourth transistor T4 having a gate electrode connected to the respective light emitting control signal line EM[n], a source electrode connected to drain electrodes of the driving transistor Td and the second transistor T2, and a drain electrode connected to an anode of a light emitting element LE; and a first reset transistor Tr1 having a gate electrode connected to the first gate line GL_P[n] in the present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line Vint_OLED of a plurality of first reset signal lines, and a drain electrode connected to the drain electrode of the fourth transistor T4 and the anode of the light emitting element LE. The second capacitor electrode Ce2 is connected to the respective voltage supply line and the source electrode of the third transistor T3.

[0089] The pixel driving circuit further include a first node N1, a second node N2, a third node N3, and a fourth node N4. The first node N1 is connected to the gate electrode of the driving transistor Td, the first capacitor electrode Ce1, and the source electrode of the second transistor T2. The second node N2 is connected to the drain electrode of the third transistor T3, the drain electrode of the first transistor T1, and the source electrode of the driving transistor Td. The third node N3 is connected to the drain electrode of the driving transistor Td, the drain electrode of the second transistor T2, the source electrode of the fourth transistor T4, and the drain electrode of the second reset transistor Tr2. The fourth node N4 is connected to the drain electrode of the fourth transistor T4, the drain electrode of the first reset transistor Tr1, and the anode of the light emitting element LE.

[0090] It should be noted that in embodiments according to the present disclosure, a source electrode or a drain electrode refers to one of a first terminal and a second terminal of a transistor, the first terminal and the second terminal being connected to an active layer of the transistor. A direction of a current flowing through the transistor may be configured to be from a source electrode to a drain electrode, or from a drain electrode to a source electrode. That is, the source electrode or the drain electrode of the transistor are interchangeable with each other. For example, referring to FIGS. 3B and 5B, a first terminal of the first reset transistor Tr1 (denoted as Sr1) may be a source electrode or a drain electrode depending on a direction of the current or a type of the transistor; similarly, a second terminal of the first reset transistor Tr1 (denoted as Dr1) may be a drain electrode or a source electrode. As another example, a first terminal of the second reset transistor Tr2 (denoted as Sr2) may be a source electrode or a drain electrode depending on a direction of the current or a type of the transistor; similarly, a second terminal of the second reset transistor Tr2 (denoted as Dr2) may be a drain electrode or a source electrode. Accordingly, the source electrode or the drain electrode of other transistors are interchangeable with each other depending on a direction of the current or a type of the transistor.

[0091] The array substrate in some embodiments includes a plurality of subpixels. In some embodiments, the plurality of subpixels includes a respective first subpixel, a respective second subpixel, a respective third subpixel, and a respective fourth subpixel. Optionally, a respective pixel of the array substrate includes the respective first subpixel, the respective second subpixel, the respective third subpixel, and the respective fourth subpixel. The plurality of subpixels in the array substrate are arranged in an array. In one example, the array of the plurality of subpixels includes a S1-S2-S3-S4 format repeating array, in which S1 stands for the respective first subpixel, S2 stands for the respective second subpixel, S3 stands for the respective third subpixel, and S4 stands for the respective fourth subpixel. In another example, the S1-S2-S3-S4 format is a C1-C2-C3-C4 format, in which C1 stands for the respective first subpixel of a first color, C2 stands for the respective second subpixel of a second color, C3 stands for the respective third subpixel of a third color, and C4 stands for the respective fourth subpixel of a fourth color. In another example, the S1-S2-S3-S4 format is a C1-C2-C3-C2' format, in which C1 stands for the respective first subpixel of a first color, C2 stands for the respective second subpixel of a second color, C3 stands for the respective third subpixel of a third color, and C2' stands for the respective fourth subpixel of the second color. In another example, the C1-C2-C3-C2' format is a R-G-B-G format, in which the respective first subpixel is a red subpixel, the respective second subpixel is a green subpixel, the respective third subpixel is a blue subpixel, and the respective fourth subpixel is a green subpixel.

[0092] In some embodiments, a minimum repeating unit of the plurality of subpixels of the array substrate includes the respective first subpixel, the respective second subpixel, the respective third subpixel, and the respective fourth subpixel. Optionally, each of the respective first subpixel, the respective second subpixel, the respective third subpixel, and the respective fourth subpixel, includes the first transistor T1, the second transistor T2, the third transistor T3, the fourth transistor T4, the first reset transistor Tr1, the second reset transistor Tr2, and the driving transistor Td.

[0093] FIG. 3A is a diagram illustrating the structure of two adjacent pixel driving circuits in an array substrate in some embodiments according to the present disclosure. FIG. 3B is a diagram illustrating the structure of a first semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3C is a diagram illustrating the structure of a first gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3D is a diagram illustrating the structure of a second gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3E is a diagram illustrating the structure of a second semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3F is a diagram illustrating the structure of a third gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3G is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an

insulating layer and a gate insulating layer in an array substrate depicted in FIG. 3A. FIG. 3H is a diagram illustrating vias extending through a passivation layer and a second inter-layer dielectric layer in an array substrate depicted in FIG. 3A. FIG. 3I is a diagram illustrating the structure of a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3J is a diagram illustrating vias extending through a first planarization layer in an array substrate depicted in FIG. 3A. FIG. 3K is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate depicted in FIG. 3A. FIG. 3L is a diagram illustrating the structure of a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3M is a diagram illustrating vias extending through a second planarization layer in an array substrate depicted in FIG. 3A. FIG. 3N is a diagram illustrating the structure of an anode layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 3O is a diagram illustrating the structure of a pixel definition layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A.

[0094] FIG. 4A is a cross-sectional view along an A-A' line in FIG. 3A. FIG. 4B is a cross-sectional view along a B-B' line in FIG. 3A. FIG. 4C is a cross-sectional view along a C-C' line in FIG. 3A. FIG. 4D is a cross-sectional view along a D-D' line in FIG. 3A.

[0095] FIG. 5A is a diagram illustrating the structure of two adjacent pixel driving circuits in an array substrate in some embodiments according to the present disclosure. FIG. 5B is a diagram illustrating the structure of a first semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5C is a diagram illustrating the structure of a first gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5D is a diagram illustrating the structure of a second gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5E is a diagram illustrating the structure of a second semiconductor material layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5F is a diagram illustrating the structure of a third gate metal layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5G is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate depicted in FIG. 5A. FIG. 5H is a diagram illustrating vias extending through a passivation layer and a second inter-layer dielectric layer in an array substrate depicted in FIG. 5A. FIG. 5I is a diagram illustrating the structure of a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5J is a diagram illustrating vias extending through a first planarization layer in an array substrate depicted in FIG. 5A. FIG. 5K is a diagram illustrating vias extending through a passivation layer, a second inter-layer dielectric layer, a first inter-layer dielectric layer, an insulating layer and a gate insulating layer in an array substrate

depicted in FIG. 5A. FIG. 5L is a diagram illustrating the structure of a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5M is a diagram illustrating vias extending through a second planarization layer in an array substrate depicted in FIG. 5A. FIG. 5N is a diagram illustrating the structure of an anode layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. FIG. 5O is a diagram illustrating the structure of a pixel definition layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A.

[0096] FIG. 6A is a cross-sectional view along a E-E' line in FIG. 5A. FIG. 6B is a cross-sectional view along an F-F' line in FIG. 5A. FIG. 6C is a cross-sectional view along a G-G' line in FIG. 5A. FIG. 6D is a cross-sectional view along an H-H' line in FIG. 5A.

[0097] Referring to FIG. 3A to FIG. 3O, and FIG. 4A to FIG. 4D, in some embodiments, corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit directly adjacent to each other and in the present stage have a substantially mirror symmetry with respect to each other, e.g., about a plane perpendicular to a main surface of the array substrate and substantially parallel to the data lines in FIG. 3A. As used herein, the term "corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit" is not intended to include layers that are not parts of the pixel driving circuits. For example, the "corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit" do not include an anode layer or a pixel definition layer. In one example, the "corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit" refers to conductive layers of the first pixel driving circuit and conductive layers of a second pixel driving circuit. In one specific example, "corresponding layers" includes at least one of a first semiconductor material layer, a first gate metal layer, a second gate metal layer, a second semiconductor material layer, a third gate metal layer, a first signal line layer, or a second signal line layer. In another specific example, "corresponding layers" further includes at least one of a gate insulating layer, an insulating layer, a first inter-layer dielectric layer, a second inter-layer dielectric layer, a passivation layer, a first planarization layer, or a second planarization layer.

[0098] Referring to FIG. 5A to FIG. 5O, and FIG. 6A to FIG. 6D, in some embodiments, corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit directly adjacent to each other and in the present stage have a substantially translational symmetry with respect to each other, e.g., along an extension direction of the gate lines in FIG. 5A. As used herein, the term "corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit" is not intended to include layers that are not parts of the pixel driving circuits. For example, the "corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit" do not include an anode layer or a pixel definition layer. In one example, the "corresponding layers of a first

pixel driving circuit and corresponding layers of a second pixel driving circuit" refers to conductive layers of the first pixel driving circuit and conductive layers of a second pixel driving circuit. In one specific example, "corresponding layers" includes at least one of a first semiconductor material layer, a first gate metal layer, a second gate metal layer, a second semiconductor material layer, a third gate metal layer, a first signal line layer, or a second signal line layer. In another specific example, "corresponding layers" further includes at least one of a gate insulating layer, an insulating layer, a first inter-layer dielectric layer, a second inter-layer dielectric layer, a passivation layer, a first planarization layer, or a second planarization layer.

[0099] Referring to FIG. 3A to FIG. 3O, FIG. 4A to FIG. 4D, FIG. 5A to FIG. 5O, and FIG. 6A to FIG. 6D, in some embodiments, the array substrate includes a base substrate BS, a first semiconductor material layer SML1 on the base substrate BS, a gate insulating layer GI on a side of the first semiconductor material layer SML1 away from the base substrate BS, a first gate metal layer Gate1 on a side of the gate insulating layer GI away from the first semiconductor material layer SML1, an insulating layer IN on a side of the first gate metal layer Gate1 away from the gate insulating layer GI, a second gate metal layer Gate2 on a side of the insulating layer IN away from the first gate metal layer Gate1, a first inter-layer dielectric layer ILD1 on a side of the second gate metal layer Gate2 away from the insulating layer IN, a second semiconductor material layer SML2 on a side of the first inter-layer dielectric layer ILD1 away from the second gate metal layer Gate2, a second inter-layer dielectric layer ILD2 on a side of the second semiconductor material layer SML2 away from the first inter-layer dielectric layer ILD1, a third gate metal layer Gate3 on a side of the second inter-layer dielectric layer ILD2 away from the second semiconductor material layer SML2, a passivation layer PVX on a side of the third gate metal layer Gate3 away from the second inter-layer dielectric layer ILD2, a first signal line layer SD1 on a side of the passivation layer PVX away from the third gate metal layer Gate3, a first planarization layer PLN1 on a side of the first signal line layer SD1 away from the passivation layer PVX, a second signal line layer SD2 on a side of the first planarization layer PLN1 away from the first signal line layer SD1, a second planarization layer PLN2 on a side of the second signal line layer SD2 away from the first planarization layer PLN1, an anode layer AD on a side of the second planarization layer PLN2 away from the second signal line layer SD2, and a pixel definition layer PDL on a side of the anode layer AD away from the second planarization layer PLN2.

[0100] Referring to FIG. 2, FIG. 3A, FIG. 3B, FIG. 5A, FIG. 5B, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the first semiconductor material layer SML1 includes at least active layers of multiple transistors of the pixel driving circuit, including the first transistor T1, the third transistor T3, the fourth transistor T4, the first reset transistor Tr1, the second reset transistor Tr2, and the driving transistor Td. Optionally, the first semiconductor material layer SML1 further includes at least respective portions of source

electrodes of multiple transistors of the pixel driving circuit, including the first transistor T1, the third transistor T3, the fourth transistor T4, the first reset transistor Tr1, the second reset transistor Tr2, and the driving transistor Td. Optionally, the first semiconductor material layer SML1 further includes at least respective portions of drain electrodes of multiple transistors of the pixel driving circuit, including the first transistor T1, the third transistor T3, the fourth transistor T4, the first reset transistor Tr1, the second reset transistor Tr2, and the driving transistor Td. Optionally, the first semiconductor material layer SML1 includes active layers, source electrodes, and drain electrodes of multiple transistors of the pixel driving circuit, including the first transistor T1, the third transistor T3, the fourth transistor T4, the first reset transistor Tr1, the second reset transistor Tr2, and the driving transistor Td. Various appropriate semiconductor materials may be used for making the first semiconductor material layer SML1. Examples of the semiconductor materials for making the first semiconductor material layer SML1 include silicon-based semiconductor materials such as polycrystalline silicon, single-crystal silicon, and amorphous silicon.

[0101] In FIG. 3B and FIG. 5B, the pixel driving circuit on the left is annotated with labels indicating components of each of multiple transistors (T1, T3, T4, Tr1, Tr2, and Td) in the pixel driving circuit. For example, the first transistor T1 includes an active layer ACT1, a source electrode S1, and a drain electrode D1. The third transistor T3 includes an active layer ACT3, a source electrode S3, and a drain electrode D3. The fourth transistor T4 includes an active layer ACT4, a source electrode S4, and a drain electrode D4. The first reset transistor Tr1 includes an active layer ACTr1, a source electrode Sr1, and a drain electrode Dr1. The second reset transistor Tr2 includes an active layer ACTr2, a source electrode Sr2, and a drain electrode Dr2. The driving transistor Td includes an active layer ACTd, a source electrode Sd, and a drain electrode Dd.

[0102] Optionally, the active layers (ACT1, ACT3, ACT4, ACTr1, ACTr2, and ACTd), the source electrodes (S1, S3, S4, Sr1, Sr2, and Sd), and the drain electrodes (D1, D3, D4, Dr1, Dr2, and Dd) of the respective transistors (T1, T3, T4, Tr1, Tr2, and Td) are in a same layer.

[0103] In some embodiments, the active layers (ACT1, ACT3, ACT4, ACTr1, and ACTd), the source electrodes (S1, S3, S4, Sr1, and Sd), and the drain electrodes (D1, D3, D4, Dr1, and Dd) of the respective transistors (T1, T3, T4, Tr1, and Td) in the pixel driving circuit are parts of a unitary structure. Optionally, a part of the second reset transistor Tr2 in the first semiconductor material layer is spaced apart from other transistors (T1, T3, T4, Tr1, and Td) in a same pixel driving circuit.

[0104] Referring to FIG. 3B, second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure. Specifically, source electrodes (or drain electrodes, depending on the direction of a current flowing through the second reset transistors) of the second reset

transistors respectively from the first pixel driving circuit and the second pixel driving circuit directly adjacent to each other and in the present stage are connected to each other, thereby forming the unitary structure.

[0105] Referring to FIG. 2, FIG. 3A, FIG. 3C, FIG. 5A, FIG. 5C, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the first gate metal layer Gate1 in some embodiments includes a plurality of first gate lines (e.g., a first gate line GL_P[n] in a present stage, a first gate line GL_P[n-1] in a previous stage), a respective light emitting control signal line EM[n] of a plurality of light emitting control signal lines, and a first capacitor electrode Ce1 of the storage capacitor Cst. Various appropriate electrode materials and various appropriate fabricating methods may be used to make the first gate metal layer Gate1. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the first gate metal layer Gate1 include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. Optionally, the plurality of first gate lines (e.g., a first gate line GL_P[n] in the present stage, the first gate line GL_P[n-1] in the previous stage), the respective light emitting control signal line EM[n] of the plurality of light emitting control signal lines, and the first capacitor electrode Ce1 of the storage capacitor Cst are in a same layer.

[0106] As used herein, the term "same layer" refers to the relationship between the layers simultaneously formed in the same step. In one example, the plurality of first gate lines and the first capacitor electrode Ce1 are in a same layer when they are formed as a result of one or more steps of a same patterning process performed in a same layer of material. In another example, the plurality of first gate lines and the first capacitor electrode Ce1 can be formed in a same layer by simultaneously performing the step of forming the plurality of first gate lines, and the step of forming the first capacitor electrode Ce1. The term "same layer" does not always mean that the thickness of the layer or the height of the layer in a cross-sectional view is the same.

[0107] In some embodiments, referring to FIG. 3C and FIG. 5C, the first gate line GL_P[n] in the present stage includes a first gate line first branch GL_P[n]_B1 and a first gate line second branch GL_P[n]_B2 configured to be provided with a same gate scanning signal. The gate electrode of the first reset transistor Tr1 is connected to the first gate line second branch GL_P[n]_B2 in the present stage. The gate electrode of the second reset transistor Tr2 is connected to the first gate line second branch GL_P[n]_B2 in the previous stage.

[0108] In one example, the first gate line GL_P[n-1] in the previous stage in FIG. 3C shows a first gate line second branch in the previous stage.

[0109] Referring to FIG. 2, FIG. 3A, FIG. 3D, FIG. 5A, FIG. 5D, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the second gate metal layer Gate2 in some embodiments includes at least portions of a plurality of second gate lines (e.g., a second gate line first branch GL_N[n]_B1) and a second capacitor electrode Ce2 of the storage capacitor Cst. Various appropriate electrode materials and various appropriate fabricating methods may be used to make the second gate metal layer Gate2. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the second gate metal layer Gate2 include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. Optionally, the second gate line first branch GL_N[n]_B1 and the second capacitor electrode Ce2 of the storage capacitor Cst are in a same layer.

[0110] Referring to FIG. 2, FIG. 3A, FIG. 3E, FIG. 5A, FIG. 5E, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the second semiconductor material layer SML2 includes at least an active layer of the second transistor T2. Optionally, the second semiconductor material layer SML2 further includes at least a portion of a source electrode of the second transistor T2. Optionally, the second semiconductor material layer SML2 further includes at least a portion of a drain electrode of the second transistor T2. Optionally, the second semiconductor material layer SML2 includes the active layer, the source electrode, and the drain electrode of the second transistor T2. In the present array substrate, at least the active layer of the second transistor T2 is in a layer different from at least the active layers of other transistors of the pixel driving circuit. Various appropriate semiconductor materials may be used for making the second semiconductor material layer SML2. Examples of the semiconductor materials for making the second semiconductor material layer SML2 include metal oxide-based semiconductor material such as indium gallium zinc oxide and metal oxynitride-based semiconductor materials such as zinc oxynitride.

[0111] In FIG. 3E and FIG. 5E, the pixel driving circuit on the left is annotated with labels indicating components of the second transistor T2 in the pixel driving circuit. For example, the second transistor T2 includes an active layer ACT2, a source electrode S2, and a drain electrode D2. Optionally, the active layer ACT2, the source electrode S2, and the drain electrode D2 of the second transistor T2 are in a same layer.

[0112] Referring to FIG. 2, FIG. 3A, FIG. 3F, FIG. 5A, FIG. 5F, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the third gate metal layer Gate3 in some embodiments includes at least portions of a plurality of second gate lines (e.g., a second gate line second branch GL_N[n]_B2). Various appropriate electrode materials and various

appropriate fabricating methods may be used to make the third gate metal layer Gate3. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the third gate metal layer Gate3 include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like.

[0113] In some embodiments, the respective second gate line GL_N[n] in a present stage includes the second gate line first branch GL_N[n]_B1 and the second gate line second branch GL_N[n]_B2 in two different layers. Optionally, the second gate line first branch GL_N[n]_B1 is in the second gate metal layer Gate2, and the second gate line second branch GL_N[n]_B2 is in the third gate metal layer Gate3. As shown in FIG. 4B and FIG. 6B, in some embodiments, an orthographic projection of the second gate line first branch GL_N[n]_B1 on a base substrate BS at least partially overlaps with an orthographic projection of the second gate line second branch GL_N[n]_B2 on the base substrate BS.

[0114] Referring to FIG. 2, FIG. 3A, FIG. 3I, FIG. 5A, FIG. 5I, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the first signal line layer SD1 includes a plurality of first reset signal lines (e.g., a respective first reset signal line Vint_OLED), a plurality of second reset signal lines (e.g., a respective second reset signal line Vint_N1), a first node connecting line Cln1, a second node connecting line Cln2, a voltage connecting pad VCP, and a relay electrode RE. Various appropriate conductive materials and various appropriate fabricating methods may be used to make the first signal line layer SD1. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the first signal line layer include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. Optionally, the plurality of first reset signal lines (e.g., the respective first reset signal line Vint_OLED), the plurality of second reset signal lines (e.g., the respective second reset signal line Vint_N1), the first node connecting line Cln1, the second node connecting line Cln2, the voltage connecting pad VCP, and the relay electrode RE are in a same layer. By having the plurality of first reset signal lines and the plurality of second reset signal lines in the first signal line layer SD1, the plurality of first reset signal lines and the plurality of second reset signal lines can be made of a material of low resistance, thereby improving mura particularly in regions display low grayscale image.

[0115] In some embodiments, the first node connecting line Cln1 connects various components of the pixel driving circuit to the node N1. Referring to FIG. 4B and FIG. 6B, the

first node connecting line Cln1 is connected to the first capacitor electrode Ce1 through a first via v1, and connected to the second transistor T2 (e.g., to the source electrode S2 of the second transistor T2) through a second via v2.

[0116] Referring to FIG. 2, FIG. 3A, FIG. 3D, FIG. 5A, FIG. 5D, FIG. 4B, and FIG. 6B, in some embodiments, in a hole region H, a portion of the second capacitor electrode Ce2 is absent. Optionally, an orthographic projection of the second capacitor electrode Ce2 on a base substrate BS completely covers, with a margin, an orthographic projection of the first capacitor electrode Ce1 on the base substrate BS except for the hole region H in which a portion of the second capacitor electrode Ce2 is absent. Optionally, the first via v1 extends through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, the hole region H, and the insulating layer IN.

[0117] In some embodiments, the first node connecting line Cln1 crosses over the respective second gate line GL_N[n] in the present stage. FIG. 7A is a diagram illustrating the structure of a first semiconductor material layer, a first gate metal layer, a second gate metal layer, a second semiconductor material layer, a third gate metal layer, and a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 8A is a diagram illustrating the structure of a first semiconductor material layer, a first gate metal layer, a second gate metal layer, a second semiconductor material layer, a third gate metal layer, and a first signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. As shown in FIG. 7A, FIG. 8A, FIG. 4B, and FIG. 6B, the first node connecting line Cln1 crosses over the second gate line first branch GL_N[n]_B1 in the second gate metal layer Gate2, and the second gate line second branch GL_N[n]_B2 in the third gate metal layer Gate3.

[0118] In some embodiments, the second node connecting line Cln2 connects various components of the pixel driving circuit to the node N3. Referring to FIG. 4A and FIG. 6A, the second node connecting line Cln2 is connected to the second transistor T2 (e.g., to the drain electrode D2 of the second transistor T2) through a third via v3, connected to the second reset transistor Tr2 (e.g., to the drain electrode Dr2 of the second reset transistor Tr2) through a fourth via v4, and connected to the fourth transistor T4 and the driving transistor Td (e.g., to the source electrode S4 of the fourth transistor T4 and the drain electrode Dd of the driving transistor Td) through a fifth via v5.

[0119] Referring to FIG. 2, FIG. 3A, FIG. 3I, FIG. 5A, FIG. 5I, FIG. 4A, and FIG. 6A, in some embodiments, the third via v3 extends through the passivation layer PVX and the second inter-layer dielectric layer ILD2, the fourth via v4 extends through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, the hole region H, and the insulating layer IN, and the fifth via v5 extends through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, the hole region H, and the insulating layer IN.

[0120] In some embodiments, referring to FIG. 7A, FIG. 3I, FIG. 8A, FIG. 5I, FIG. 4A, and FIG. 6A, the second node connecting line Cln2 crosses over the respective second gate line GL_N[n] in the present stage and a first gate line first branch GL_P[n]_B1 of the first gate line GL_P[n] in the present stage. Optionally, the second node connecting line Cln2 crosses over the second gate line first branch GL_N[n]_B1 and the second gate line second branch GL_N[n]_B2 of the respective second gate line GL_N[n] in the present stage, and the first gate line first branch GL_P[n]_B1 of the first gate line GL_P[n] in the present stage.

[0121] Referring to FIG. 2, FIG. 3A, FIG. 3L, FIG. 5A, FIG. 5L, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the second signal line layer SD2 includes a plurality of voltage supply lines (e.g., the respective voltage supply line Vdd), a plurality of data lines (e.g., the respective data line DL), and an anode contact pad ACP. Various appropriate conductive materials and various appropriate fabricating methods may be used to make the second signal line layer SD2. For example, a conductive material may be deposited on the substrate by a plasma-enhanced chemical vapor deposition (PECVD) process and patterned. Examples of appropriate conductive materials for making the second signal line layer SD2 include, but are not limited to, aluminum, copper, molybdenum, chromium, aluminum copper alloy, copper molybdenum alloy, molybdenum aluminum alloy, aluminum chromium alloy, copper chromium alloy, molybdenum chromium alloy, copper molybdenum aluminum alloy, and the like. Optionally, the plurality of voltage supply lines (e.g., the respective voltage supply line Vdd), the plurality of data lines (e.g., the respective data line DL), and the anode contact pad ACP are in a same layer.

[0122] FIG. 7B is a diagram illustrating the structure of a first signal line layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 8B is a diagram illustrating the structure of a first signal line layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. Referring to FIG. 7B, FIG. 8B, FIG. 2, FIG. 3A, FIG. 3I, FIG. 5A, FIG. 5I, FIG. 4C, and FIG. 6C, in some embodiments, the relay electrode RE is connected to the drain electrode D4 of the fourth transistor T4 and the drain electrode Dr1 of the first reset transistor Tr1 through a sixth via v6 extending through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, and the insulating layer IN. An anode contact pad ACP is connected to the relay electrode RE through a seventh via v7 extending through the first planarization layer PLN1.

[0123] Referring to FIG. 2, FIG. 3A, FIG. 3I, FIG. 5A, FIG. 5I, FIG. 4D, and FIG. 6D, in some embodiments, the voltage connecting pad VCP is connected to the third transistor T3 (e.g., to the source electrode S3 of the third transistor T3) through an eighth via v8 extending through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, and the insulating layer IN. The respective voltage supply line Vdd

of the plurality of voltage supply lines is connected to the voltage connecting pad VCP through a ninth via v9 extending through the first planarization layer PLN1. The voltage connecting pad VCP is connected to the second capacitor electrode Ce2 of the storage capacitor Cst through a tenth via v10 extending through the passivation layer PVX, the second inter-layer dielectric layer ILD2, and the first inter-layer dielectric layer ILD1.

[0124] Referring to FIG. 2, FIG. 3A, FIG. 3I, FIG. 5A, FIG. 5I, FIG. 4A, and FIG. 6A, in some embodiments, the respective second reset signal line Vint_N1 of a plurality of second reset signal lines is connected to the second reset transistor Tr2 (e.g., to the source electrode Sr2 of the second reset transistor Tr2) through an eleventh via v11 extending through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, and the insulating layer IN.

[0125] Referring to FIG. 2, FIG. 3A, FIG. 3I, FIG. 5A, FIG. 5I, FIG. 4C, and FIG. 6C, in some embodiments, the respective first reset signal line Vint_OLED of a plurality of first reset signal lines is connected to the first reset transistor Tr1 (e.g., to the source electrode Sr1 of the first reset transistor Tr1) through a twelfth via v12 extending through the passivation layer PVX, the second inter-layer dielectric layer ILD2, the first inter-layer dielectric layer ILD1, and the insulating layer IN.

[0126] Referring to FIG. 2, FIG. 3A, FIG. 3N, FIG. 5A, FIG. 5N, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the array substrate further includes an anode layer AD.

[0127] Referring to FIG. 2, FIG. 3A, FIG. 3O, FIG. 5A, FIG. 5O, FIG. 4A to FIG. 4D, and FIG. 6A to FIG. 6D, in some embodiments, the array substrate further includes a pixel definition layer PDL. The pixel definition layer PDL defines subpixel apertures SA, through which light emitting layers are respectively connected to anodes in respective pixel driving circuits.

[0128] In some embodiments, the array substrate includes a novel pixel driving circuit. The pixel driving circuit in some embodiments includes a driving transistor Td, and a storage capacitor Cst, and a first reset transistor Tr1 having a gate electrode connected to a first gate line GL_P[n] in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line Vint_OLED of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element LE. Optionally, the pixel driving circuit further includes a second reset transistor Tr2 having a gate electrode connected to a first gate line GL_P[n-1] in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line Vint_N1 of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor Td. The first gate line GL_P[n-1] in the previous stage is connected to the gate electrode of the

second reset transistor Tr2 in the present stage and a gate electrode of the first reset transistor Tr1 in the previous stage. The first gate line GL_P[n] in the present stage is connected to the gate electrode of the first reset transistor Tr1 in the present stage and a gate electrode of the second reset transistor Tr2 in a next stage. As used herein, an individual stage corresponds to a row of pixel driving circuits, for example, a present stage corresponds to a present row of pixel driving circuits, and a previous stage corresponds to a previous row of pixel driving circuits. In one example, the first gate line GL_P[n] in the present row of pixel driving circuits is connected to the gate electrode of the first reset transistor Tr1 in the present row of pixel driving circuits and a gate electrode of the second reset transistor Tr2 in a next row of pixel driving circuits.

[0129] By having the second reset transistor Tr2 in the present stage and the first reset transistor Tr1 in the previous stage share a same gate line, and having the first reset transistor Tr1 in the present stage and the second reset transistor Tr2 in a next stage share a same gate line, the layout of the pixel driving circuit can be simplified to enhance light transmittance rate and image display resolution of the array substrate.

[0130] In some embodiments, the pixel driving circuit further includes a fourth transistor T4 having a gate electrode connected to a respective light emitting control signal line EM[n], a source electrode connected to the drain electrode of the second reset transistor Tr2 and the drain electrode of the driving transistor Td, and a drain electrode connected to the drain electrode of the first reset transistor Tr1 and the anode of the light emitting element LE.

[0131] In some embodiments, the first gate line GL_P[n] in the present stage comprises a first gate line first branch GL_P[n]_B1 and a first gate line second branch GL_P[n]_B2 configured to be provided with a same gate scanning signal. The gate electrode of the first reset transistor Tr1 is connected to the first gate line second branch GL_P[n]_B2 in the present stage. The gate electrode of the second reset transistor Tr2 is connected to the first gate line second branch GL_P[n]_B2 in the previous stage.

[0132] In some embodiments, the pixel driving circuit further includes a first transistor T1 having a gate electrode connected to the first gate line first branch GL_P[n]_B1 in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line DL of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor Td.

[0133] In some embodiments, the pixel driving circuit further includes a second transistor T2 having a gate electrode connected to a respective second gate line GL_N[n] in a present stage of a plurality of second gate lines, a source electrode connected to a first capacitor electrode Ce1 of the storage capacitor Cst and a gate electrode of the driving transistor Td, and a drain

electrode connected to a drain electrode of the driving transistor Td. The plurality of first gate lines and the plurality of second gate lines are spaced apart by one or more insulating layer.

[0134] In some embodiments, the array substrate includes a base substrate BS; a first semiconductor material layer SML1 on the base substrate; an insulating layer IN on a side of the first semiconductor material layer SML1 away from the base substrate BS; and a second semiconductor material layer SML2 on a side of the insulating layer IN away from the first semiconductor material layer SML1. The first semiconductor material layer SML1 includes an active layer of the driving transistor Td and an active layer of the first reset transistor Tr1. The second semiconductor material layer SML2 includes an active layer of the second transistor T2. In some embodiments, the first semiconductor material layer SML1 further includes at least a portion of the source electrode of the driving transistor Td, at least a portion of the drain electrode of the driving transistor Td, at least a portion of the source electrode of the first reset transistor Tr1, at least a portion of the drain electrode of the first reset transistor Tr1. In some embodiments, the second semiconductor material layer further includes at least a portion of the source electrode of the second transistor T2, and at least a portion of the drain electrode of the second transistor T2. Optionally, the first semiconductor material layer SML1 includes active layers, at least portions of source electrodes, and at least portions of drain electrodes of all transistors other than the second transistor T2 in the pixel driving circuit. Optionally, the first semiconductor material layer SML1 includes a polycrystalline silicon material; and the second semiconductor material layer SML2 includes a metal oxide semiconductor material.

[0135] In some embodiments, the respective second gate line GL_N[n] in a present stage comprises a second gate line first branch GL_N[n]_B1 and a second gate line second branch GL_N[n]_B2 in two different layers. Optionally, an orthographic projection of the second gate line first branch GL_N[n]_B1 on a base substrate at least partially overlaps with an orthographic projection of the second gate line second branch GL_N[n]_B2 on the base substrate BS.

[0136] In some embodiments, the array substrate includes a base substrate BS; a second gate metal layer Gate2 on the base substrate BS; a first inter-layer dielectric layer ILD1 on a side of the second gate metal layer Gate2 away from the base substrate BS; a second semiconductor material layer SML2 on a side of the first inter-layer dielectric layer ILD1 away from the second gate metal layer Gate2; a second inter-layer dielectric layer ILD2 on a side of the second semiconductor material layer SML2 away from the first inter-layer dielectric layer ILD1; and a third gate metal layer Gate3 on a side of the second inter-layer dielectric layer ILD2 away from the second semiconductor material layer SML2. Optionally, the second gate metal layer Gate2 includes the second gate line first branch GL_N[n]_B1. Optionally, the second semiconductor material layer SML2 includes an active layer of the second transistor T2.

Optionally, the third gate metal layer Gate3 includes the second gate line second branch GL_N[n]_B2.

[0137] In some embodiments, the array substrate includes a base substrate BS; a first gate metal layer Gate1 on the base substrate BS, the first gate metal layer Gate1 including a first capacitor electrode Ce1 of the storage capacitor Cst; a second semiconductor material layer SML2 on a side of the first gate metal layer Gate1 away from the base substrate BS, the second semiconductor material layer SML2 including at least a portion of a source electrode of the second transistor T2; and a first signal line layer SD1 on a side of the second semiconductor material layer SML2 away from the first gate metal layer Gate1, the first signal line layer SD1 including the plurality of first reset signal lines and a first node connecting line Cln1. Optionally, the first node connecting line Cln1 is connected to the first capacitor electrode Ce1 through a first via v1, and connected to the source electrode of the second transistor T2 through a second via v2. Optionally, the first node connecting line Cln1 crosses over the respective second gate line GL_N[n] in the present stage.

[0138] In some embodiments, the array substrate includes a base substrate BS; a first semiconductor material layer SML1 on the base substrate BS, the first semiconductor material layer SML1 including the drain electrode of the second reset transistor Tr2, the source electrode of the fourth transistor T4, and the drain electrode of the driving transistor Td; a second semiconductor material layer SML2 on a side of the first semiconductor material layer SML1 away from the base substrate, the second semiconductor material layer SML2 including the drain electrode of the second transistor T2; and a first signal line layer SD1 on a side of the second semiconductor material layer SML2 away from the first gate metal layer Gate1, the first signal line layer SD1 including the plurality of first reset signal lines and a second node connecting line Cln2. Optionally, the second node connecting line Cln2 is connected to the drain electrode of the second transistor T2 through a third via v3, connected to the drain electrode of the second reset transistor Tr2 through a fourth via v4, and connected to the source electrode of the fourth transistor T4 and the drain electrode of the driving transistor Td through a fifth via v5. Optionally, the second node connecting line Cln2 crosses over the respective second gate line GL_N[n] in the present stage and a first gate line first branch GL_P[n]_B1 of the first gate line GL_P[n] in the present stage.

[0139] In some embodiments, the array substrate includes a base substrate BS; a second semiconductor material layer SML2 on a side of the insulating layer IN away from the first semiconductor material layer SML1, the second semiconductor material layer SML2 including an active layer of the second transistor T2; and a second signal line layer SD2 on a side of the second semiconductor material layer SML2 away from the base substrate BS, the second signal line layer SD2 including a plurality of voltage supply lines. FIG. 7C is a diagram illustrating the structure of a second semiconductor material layer and a second signal line layer of two

adjacent pixel driving circuits in an array substrate depicted in FIG. 3A. FIG. 8C is a diagram illustrating the structure of a second semiconductor material layer and a second signal line layer of two adjacent pixel driving circuits in an array substrate depicted in FIG. 5A. Referring to FIG. 7C and FIG. 8C, in some embodiments, an orthographic projection of a respective voltage supply line Vdd of the plurality of voltage supply lines on the base substrate BS covers an orthographic projection of the active layer of the second transistor T2 on the base substrate BS. Optionally, the orthographic projection of a respective voltage supply line Vdd of the plurality of voltage supply lines on the base substrate BS further covers an orthographic projection of the source electrode (or drain electrode, depending on the direction of a current flowing through the second transistor T2) of the second transistor T2 on the base substrate BS. Optionally, voltage supply lines respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure in which the voltage supply lines are connected to each other in a region where orthographic projections of voltage supply lines on the base substrate cover orthographic projections of active layers of second transistors from the first subpixel and the second subpixel on the base substrate BS.

[0140] Referring to FIG. 3B, FIG. 7A, FIG. 4A, and FIG. 4C, in some embodiments, second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure in which source electrodes (or drain electrodes, depending on the direction of a current flowing through the second reset transistors) of the second reset transistors are connected to each other in a region where the respective second reset signal line Vint_N1 is connected to the source electrodes or drain electrodes of the second reset transistors through one or more vias. Optionally, the second reset transistor Tr2 is spaced apart from other transistors in a same pixel driving circuit, as shown in FIG. 3B. Second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure. Source electrodes or drain electrodes of the second reset transistors respectively from the first pixel driving circuit and the second pixel driving circuit directly adjacent to each other and in the present stage are connected to each other, thereby forming the unitary structure. Optionally, the respective second reset signal line Vint_N1 is connected to the source electrodes or drain electrodes of the second reset transistors through a single via. The single via design can further enhance image display resolution of the array substrate.

[0141] In another aspect, the present invention provides a display apparatus, including the array substrate described herein or fabricated by a method described herein, and one or more integrated circuits connected to the array substrate.

[0142] Examples of appropriate display apparatuses include, but are not limited to, an electronic paper, a mobile phone, a tablet computer, a television, a monitor, a notebook

computer, a digital album, a GPS, etc. Optionally, the display apparatus is an organic light emitting diode display apparatus. Optionally, the display apparatus is a liquid crystal display apparatus.

[0143] In another aspect, the present invention provides a pixel driving circuit. In some embodiments, the pixel driving circuit includes a driving transistor, and a storage capacitor, and a first reset transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element.

[0144] In some embodiments, the pixel driving circuit further includes a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor. Optionally, the first gate line in the previous stage is connected to the gate electrode of the second reset transistor in the present stage and a gate electrode of a first reset transistor in the previous stage; and the first gate line in the present stage is connected to the gate electrode of the first reset transistor in the present stage and a gate electrode of a second reset transistor in a next stage.

[0145] In some embodiments, the pixel driving circuit further includes a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element.

[0146] In some embodiments, the first gate line in the present stage comprises a first gate line first branch and a first gate line second branch configured to be provided with a same gate scanning signal. Optionally, the gate electrode of the first reset transistor is connected to the first gate line second branch in the present stage; and the gate electrode of the second reset transistor is connected to the first gate line second branch in the previous stage.

[0147] In some embodiments, the pixel driving circuit further includes a first transistor having a gate electrode connected to the first gate line first branch in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor.

[0148] In some embodiments, the pixel driving circuit further includes a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to a first capacitor electrode of the storage capacitor and a gate electrode of the driving transistor, and a drain electrode connected

to a drain electrode of the driving transistor. Optionally, the plurality of first gate lines and the plurality of second gate lines are spaced apart by one or more insulating layer.

[0149] In some embodiments, the respective second gate line in a present stage includes a second gate line first branch and a second gate line second branch in two different layers.

[0150] In some embodiments, the pixel driving circuit includes a driving transistor, and a storage capacitor, and a first reset transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element; a second reset transistor having a gate electrode connected to a first gate line in a previous stage of a plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; a first transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor; a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to the first capacitor electrode of the storage capacitor and the gate electrode of the driving transistor, and a drain electrode connected to the drain electrode of the driving transistor; a third transistor having a gate electrode connected to a respective light emitting control signal line of a plurality of light emitting control signal lines, a source electrode connected to a respective voltage supply line of a plurality of voltage supply lines, and a drain electrode connected to the source electrode of the driving transistor and the drain electrode of the first transistor; and a fourth transistor having a gate electrode connected to the respective light emitting control signal line, a source electrode connected to drain electrodes of the driving transistor and the second transistor, and a drain electrode connected to an anode of a light emitting element. Optionally, the second capacitor electrode is connected to the respective voltage supply line and the source electrode of the third transistor.

[0151] The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be

defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the invention”, “the present invention” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use “first”, “second”, etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. A pixel driving circuit, comprising:

a driving transistor;

a storage capacitor;

a first reset transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective first reset signal line of a plurality of first reset signal lines, and a drain electrode connected to an anode of a light emitting element; and

a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor.

2. The pixel driving circuit of claim 1,

wherein the first gate line in the previous stage is connected to the gate electrode of the second reset transistor in the present stage and a gate electrode of a first reset transistor in the previous stage; and

the first gate line in the present stage is connected to the gate electrode of the first reset transistor in the present stage and a gate electrode of a second reset transistor in a next stage.

3. The pixel driving circuit of claim 2, further comprising a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element.

4. The pixel driving circuit of claim 2 or claim 3, wherein the first gate line in the present stage comprises a first gate line first branch and a first gate line second branch configured to be provided with a same gate scanning signal;

the gate electrode of the first reset transistor is connected to the first gate line second branch in the present stage; and

the gate electrode of the second reset transistor is connected to the first gate line second branch in the previous stage.

5. The pixel driving circuit of claim 4, further comprising a first transistor having a gate electrode connected to the first gate line first branch in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor.

6. The pixel driving circuit of any one of claims 1 to 5, further comprising a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to a first capacitor electrode of the storage capacitor and a gate electrode of the driving transistor, and a drain electrode connected to a drain electrode of the driving transistor;

wherein the plurality of first gate lines and the plurality of second gate lines are spaced apart by one or more insulating layer.

7. The pixel driving circuit of claim 6, wherein the respective second gate line in a present stage comprises a second gate line first branch and a second gate line second branch in two different layers.

8. The pixel driving circuit of any one of claims 1 to 7, further comprising:

a second reset transistor having a gate electrode connected to a first gate line in a previous stage of a plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor;

a first transistor having a gate electrode connected to a first gate line in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor;

a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source electrode connected to the first capacitor electrode of the storage capacitor and the gate electrode of the driving transistor, and a drain electrode connected to the drain electrode of the driving transistor;

a third transistor having a gate electrode connected to a respective light emitting control signal line of a plurality of light emitting control signal lines, a source electrode connected to a respective voltage supply line of a plurality of voltage supply lines, and a drain electrode connected to the source electrode of the driving transistor and the drain electrode of the first transistor; and

a fourth transistor having a gate electrode connected to the respective light emitting control signal line, a source electrode connected to drain electrodes of the driving transistor and the second transistor, and a drain electrode connected to an anode of a light emitting element;

wherein a second capacitor electrode of the storage capacitor is connected to the respective voltage supply line and the source electrode of the third transistor.

9. An array substrate, comprising the pixel driving circuit of any one of claims 1 to 8, and the light emitting element connected to the pixel driving circuit.

10. The array substrate of claim 9, wherein the pixel driving circuit further comprises a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor;

the first gate line in the previous stage is connected to the gate electrode of the second reset transistor in the present stage and a gate electrode of a first reset transistor in the previous stage; and

the first gate line in the present stage is connected to the gate electrode of the first reset transistor in the present stage and a gate electrode of a second reset transistor in a next stage.

11. The array substrate of claim 10, wherein the pixel driving circuit further comprises a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element.

12. The array substrate of claim 10 or claim 11, wherein the first gate line in the present stage comprises a first gate line first branch and a first gate line second branch configured to be provided with a same gate scanning signal;

the gate electrode of the first reset transistor is connected to the first gate line second branch in the present stage; and

the gate electrode of the second reset transistor is connected to the first gate line second branch in the previous stage.

13. The array substrate of claim 12, wherein the pixel driving circuit further comprises a first transistor having a gate electrode connected to the first gate line first branch in a present stage of a plurality of first gate lines, a source electrode connected to a respective data line of a plurality of data lines, and a drain electrode connected to a source electrode of the driving transistor.

14. The array substrate of any one of claims 9 to 13, wherein the pixel driving circuit further comprises a second transistor having a gate electrode connected to a respective second gate line in a present stage of a plurality of second gate lines, a source

electrode connected to a first capacitor electrode of the storage capacitor and a gate electrode of the driving transistor, and a drain electrode connected to a drain electrode of the driving transistor; and

the plurality of first gate lines and the plurality of second gate lines are spaced apart by one or more insulating layer.

15. The array substrate of claim 14, comprising:

a base substrate;

a first semiconductor material layer on the base substrate;

an insulating layer on a side of the first semiconductor material layer away from the base substrate; and

a second semiconductor material layer on a side of the insulating layer away from the first semiconductor material layer;

wherein the first semiconductor material layer comprises an active layer of the driving transistor and an active layer of the first reset transistor; and

the second semiconductor material layer comprises an active layer of the second transistor.

16. The array substrate of claim 15, wherein the first semiconductor material layer further comprises at least a portion of the source electrode of the driving transistor, at least a portion of the drain electrode of the driving transistor, at least a portion of the source electrode of the first reset transistor, at least a portion of the drain electrode of the first reset transistor; and

the second semiconductor material layer further comprises at least a portion of the source electrode of the second transistor, and at least a portion of the drain electrode of the second transistor.

17. The array substrate of claim 15 or claim 16, wherein the first semiconductor material layer comprises active layers, at least portions of source electrodes, and at least portions of drain electrodes of all transistors other than the second transistor in the pixel driving circuit.

18. The array substrate of any one of claims 15 to 17, wherein the first semiconductor material layer comprises a polycrystalline silicon material; and

the second semiconductor material layer comprises a metal oxide semiconductor material.

19. The array substrate of any one of claims 14 to 18, wherein the respective second gate line in a present stage comprises a second gate line first branch and a second gate line second branch in two different layers; and

an orthographic projection of the second gate line first branch on a base substrate at least partially overlaps with an orthographic projection of the second gate line second branch on the base substrate.

20. The array substrate of claim 19, comprising:

a base substrate;

a second gate metal layer on the base substrate;

a first inter-layer dielectric layer on a side of the second gate metal layer away from the base substrate;

a second semiconductor material layer on a side of the first inter-layer dielectric layer away from the second gate metal layer;

a second inter-layer dielectric layer on a side of the second semiconductor material layer away from the first inter-layer dielectric layer; and

a third gate metal layer on a side of the second inter-layer dielectric layer away from the second semiconductor material layer;

wherein the second gate metal layer comprises the second gate line first branch;

the second semiconductor material layer comprises an active layer of the second transistor; and

the third gate metal layer comprises the second gate line second branch.

21. The array substrate of any one of claims 14 to 20, further comprising:

a base substrate;

a first gate metal layer on the base substrate, the first gate metal layer comprising a first capacitor electrode of the storage capacitor;

a second semiconductor material layer on a side of the first gate metal layer away from the base substrate, the second semiconductor material layer comprising at least a portion of a source electrode of the second transistor; and

a first signal line layer on a side of the second semiconductor material layer away from the first gate metal layer, the first signal line layer comprising the plurality of first reset signal lines and a first node connecting line;

wherein the first node connecting line is connected to the first capacitor electrode through a first via, and connected to the source electrode of the second transistor through a second via.

22. The array substrate of claim 21, wherein the first node connecting line crosses over the respective second gate line in the present stage.

23. The array substrate of any one of claims 14 to 22, wherein the pixel driving circuit further comprises:

a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; and

a fourth transistor having a gate electrode connected to a respective light emitting control signal line, a source electrode connected to the drain electrode of the second reset transistor and the drain electrode of the driving transistor, and a drain electrode connected to the drain electrode of the first reset transistor and the anode of the light emitting element;

wherein the array substrate further comprises:

a base substrate;

a first semiconductor material layer on the base substrate, the first semiconductor material layer comprising the drain electrode of the second reset transistor, the source electrode of the fourth transistor, and the drain electrode of the driving transistor;

a second semiconductor material layer on a side of the first semiconductor material layer away from the base substrate, the second semiconductor material layer comprising the drain electrode of the second transistor; and

a first signal line layer on a side of the second semiconductor material layer away from the first gate metal layer, the first signal line layer comprising the plurality of first reset signal lines and a second node connecting line;

wherein the second node connecting line is connected to the drain electrode of the second transistor through a third via, connected to the drain electrode of the second reset transistor through a fourth via, and connected to the source electrode of the fourth transistor and the drain electrode of the driving transistor through a fifth via.

24. The array substrate of claim 23, wherein the second node connecting line crosses over the respective second gate line in the present stage and a first gate line first branch of the first gate line in the present stage.

25. The array substrate of any one of claims 14 to 24, comprising:

a base substrate;

a second semiconductor material layer on a side of the insulating layer away from the first semiconductor material layer, the second semiconductor material layer comprising an active layer of the second transistor; and

a second signal line layer on a side of the second semiconductor material layer away from the base substrate, the second signal line layer comprising a plurality of voltage supply lines;

wherein an orthographic projection of a respective voltage supply line of the plurality of voltage supply lines on the base substrate covers an orthographic projection of the active layer of the second transistor on the base substrate.

26. The array substrate of claim 25, wherein the orthographic projection of a respective voltage supply line of the plurality of voltage supply lines on the base substrate further covers an orthographic projection of the source electrode or drain electrode of the second transistor on the base substrate.

27. The array substrate of claim 25 or claim 26, wherein voltage supply lines respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure in which the voltage supply lines are connected to each other in a region where orthographic projections of voltage supply lines on the base substrate cover orthographic projections of active layers of second transistors from the first pixel driving circuit and the second pixel driving circuit on the base substrate.

28. The array substrate of any one of claims 9 to 27, wherein the pixel driving circuit further comprises a second reset transistor having a gate electrode connected to a first gate line in a previous stage of the plurality of first gate lines, a source electrode connected to a respective second reset signal line of a plurality of second reset signal lines, and a drain electrode connected to a drain electrode of the driving transistor; and

wherein second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure in which source or drain electrodes of the second reset transistors are connected to each other in a region where the respective second reset signal line is connected to the source or drain electrodes of the second reset transistors through one or more vias.

29. The array substrate of claim 28, wherein a part of the second reset transistor in the first semiconductor material layer is spaced apart from other transistors in a same pixel driving circuit;

second reset transistors respectively from a first pixel driving circuit and a second pixel driving circuit directly adjacent to each other and in the present stage form a unitary structure; and

source or drain electrodes of the second reset transistors respectively from the first pixel driving circuit and the second pixel driving circuit directly adjacent to each other and in the present stage are connected to each other, thereby forming the unitary structure.

30. The array substrate of claim 29, wherein the respective second reset signal line is connected to the source or drain electrodes of the second reset transistors through a single via.

31. The array substrate of any one of claims 9 to 30, wherein corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit directly adjacent to each other and in the present stage have a substantially mirror symmetry with respect to each other.

32. The array substrate of any one of claims 9 to 30, wherein corresponding layers of a first pixel driving circuit and corresponding layers of a second pixel driving circuit directly adjacent to each other and in the present stage have a substantially translational symmetry.

33. A display apparatus, comprising the array substrate of any one of claims 9 to 32, and an integrated circuit connected to the array substrate.

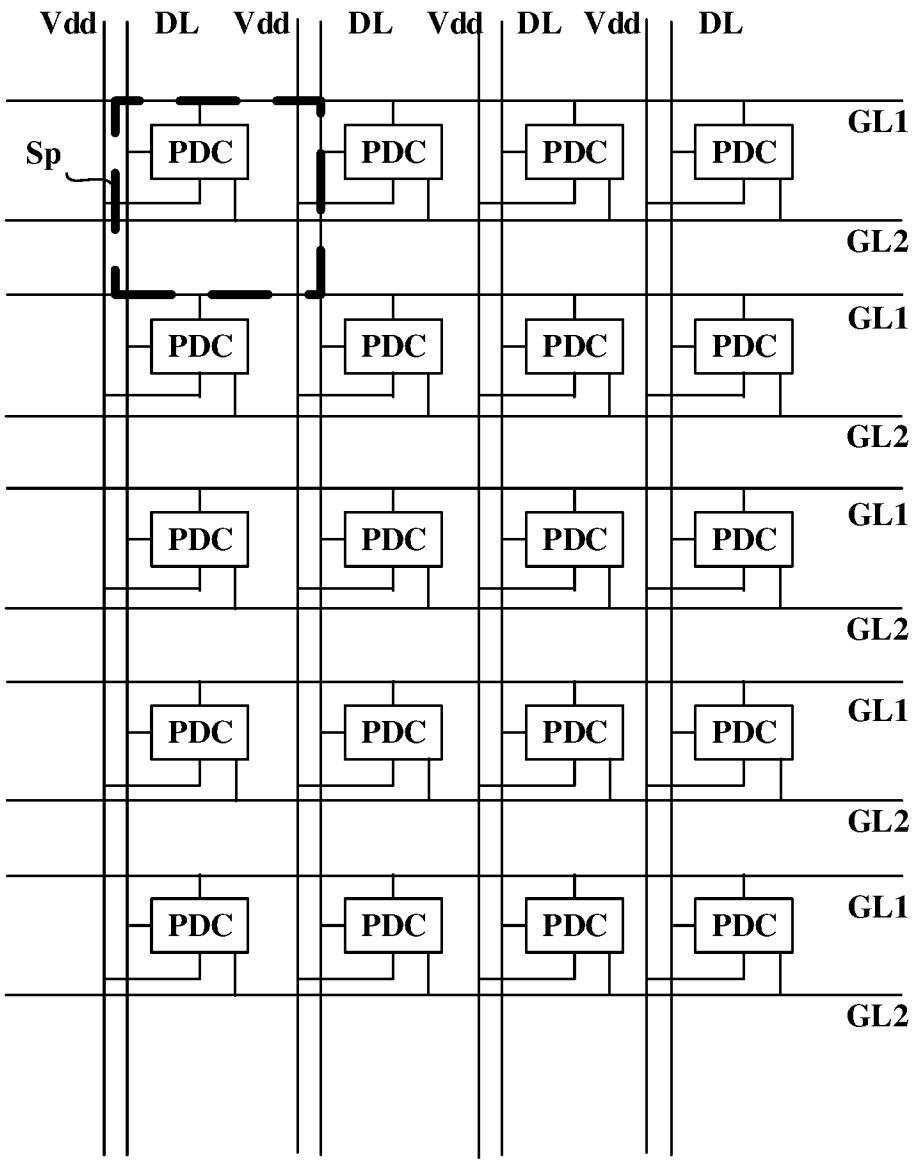

FIG. 1

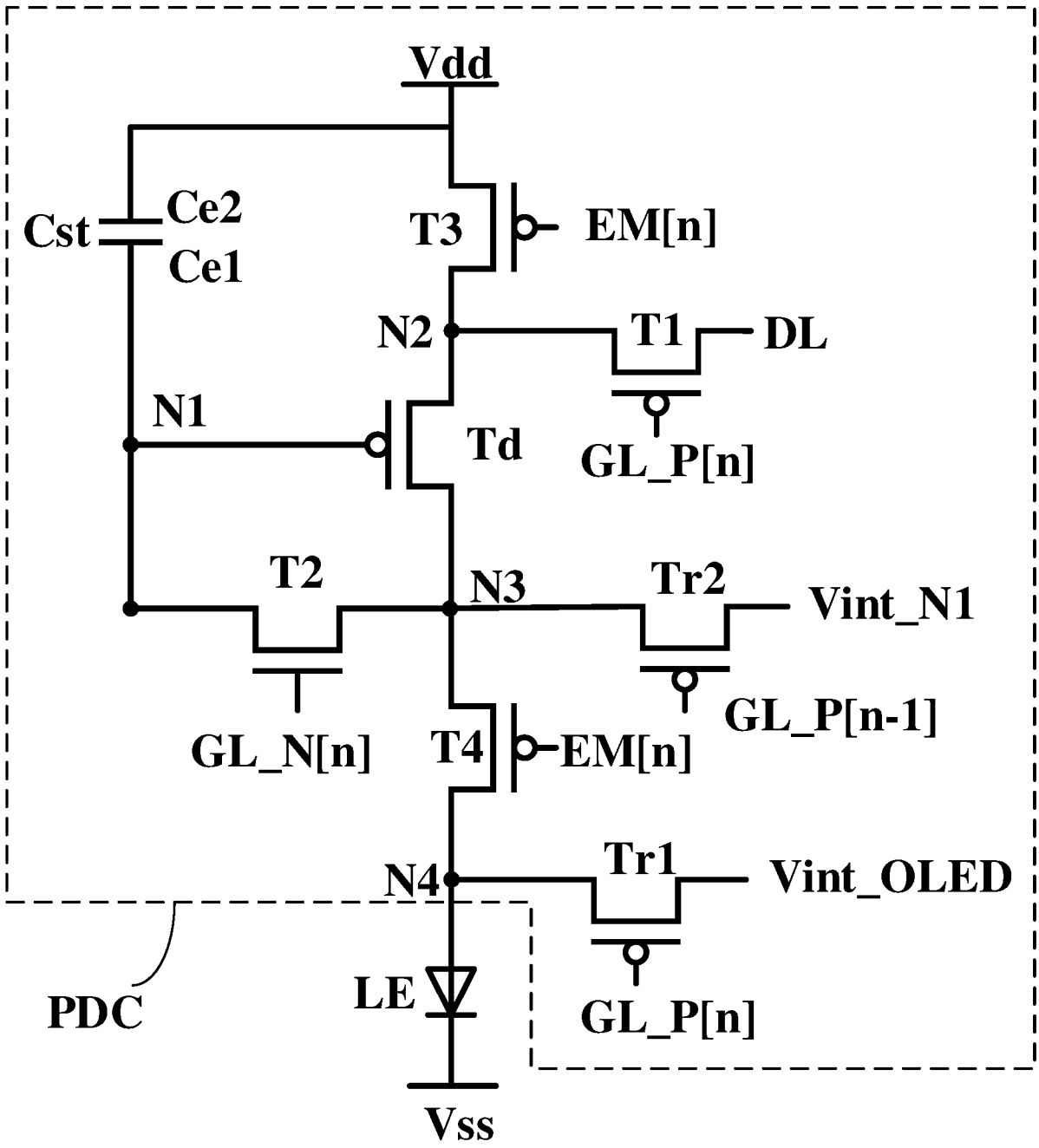
Vdd
Cst
Ce2
Ce1
T3
EM[n]
N2
T1
DL
N1
Td
GL_P[n]
T2
N3
Tr2
Vint_N1
GL_N[n]
GL_P[n-1]
T4
EM[n]
N4
Tr1
Vint_OLED
PDC
LE
GL_P[n]
Vss

FIG. 2

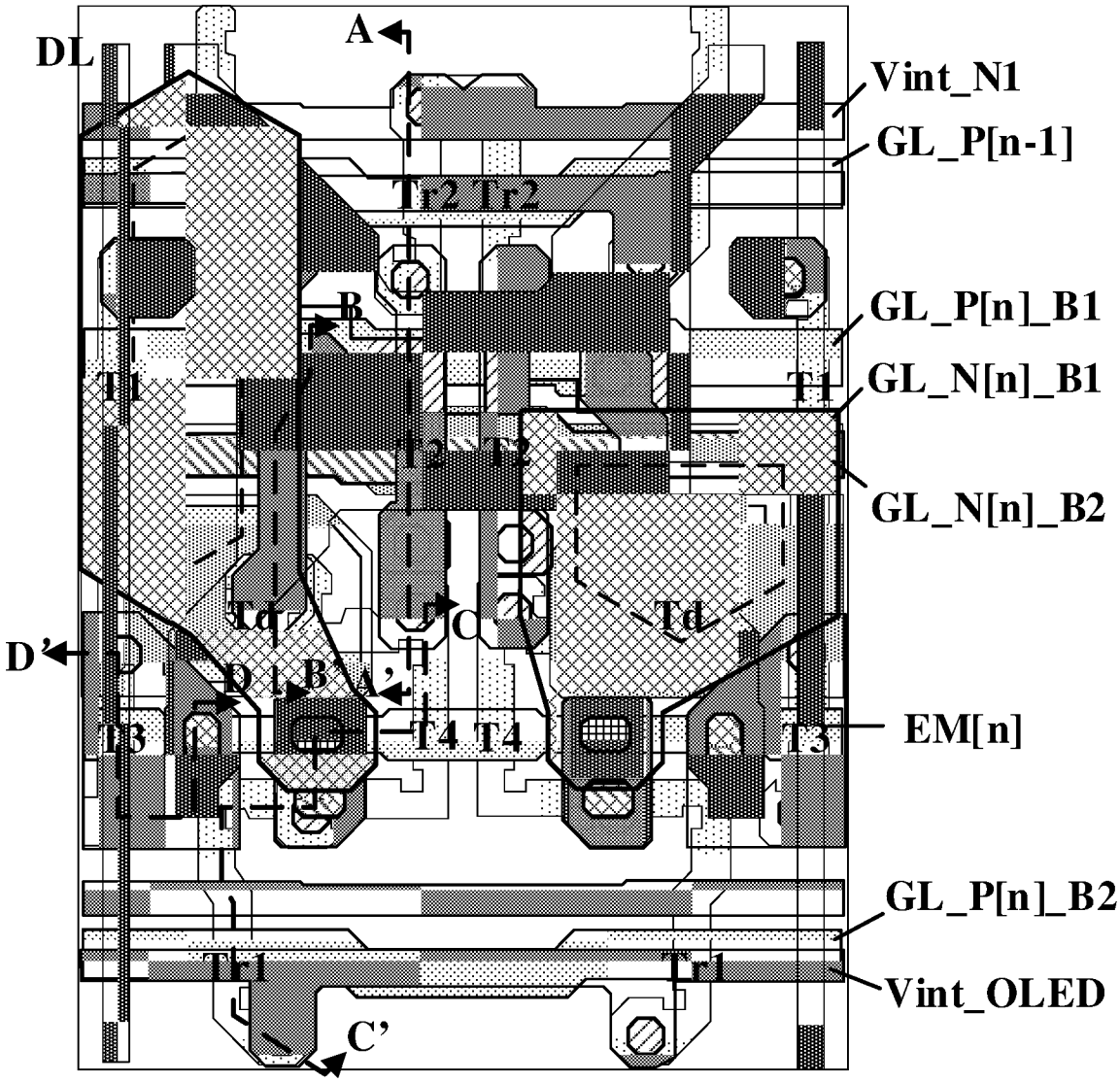
DL
A
Vint_N1
GL_P[n-1]
Tr2 Tr2
B
GL_P[n]_B1
T1
T1
GL_N[n]_B1
T2 T2
GL_N[n]_B2
Td
C
Td
D'
D
B'
A'
T3
T4 T4
T3
EM[n]
GL_P[n]_B2
Tr1
Tr1
Vint_OLED
C'

FIG. 3A

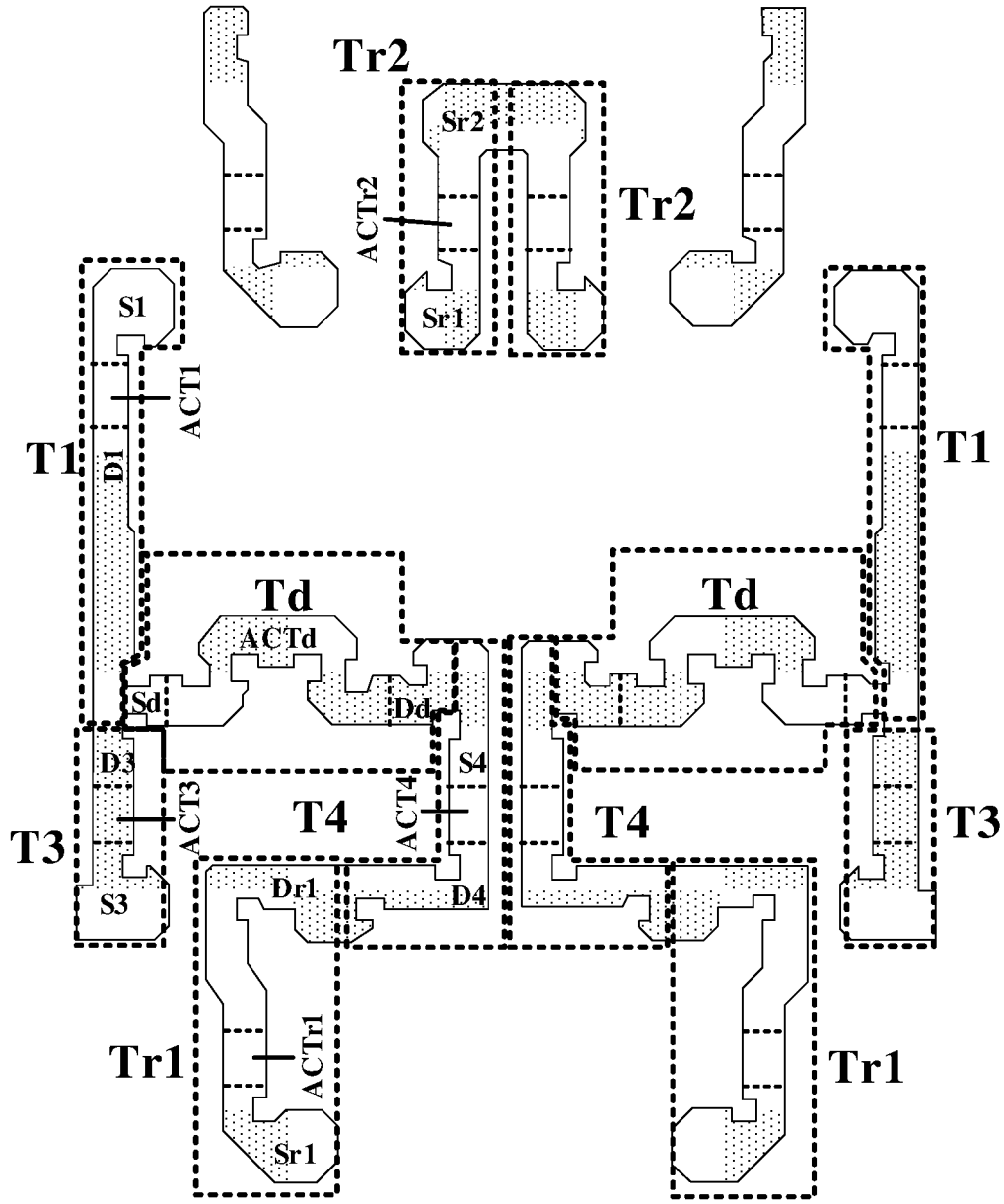
Tr2
Sr2
ACTr2
Tr2
Sr1
S1
ACT1
T1
D1
T1
Td
Td
ACTd
Sd
Dd
D3
S4
ACT3
T4
ACT4
T4
T3
T3
S3
Dr1
D4
Tr1
ACTr1
Tr1
Sr1

FIG. 3B

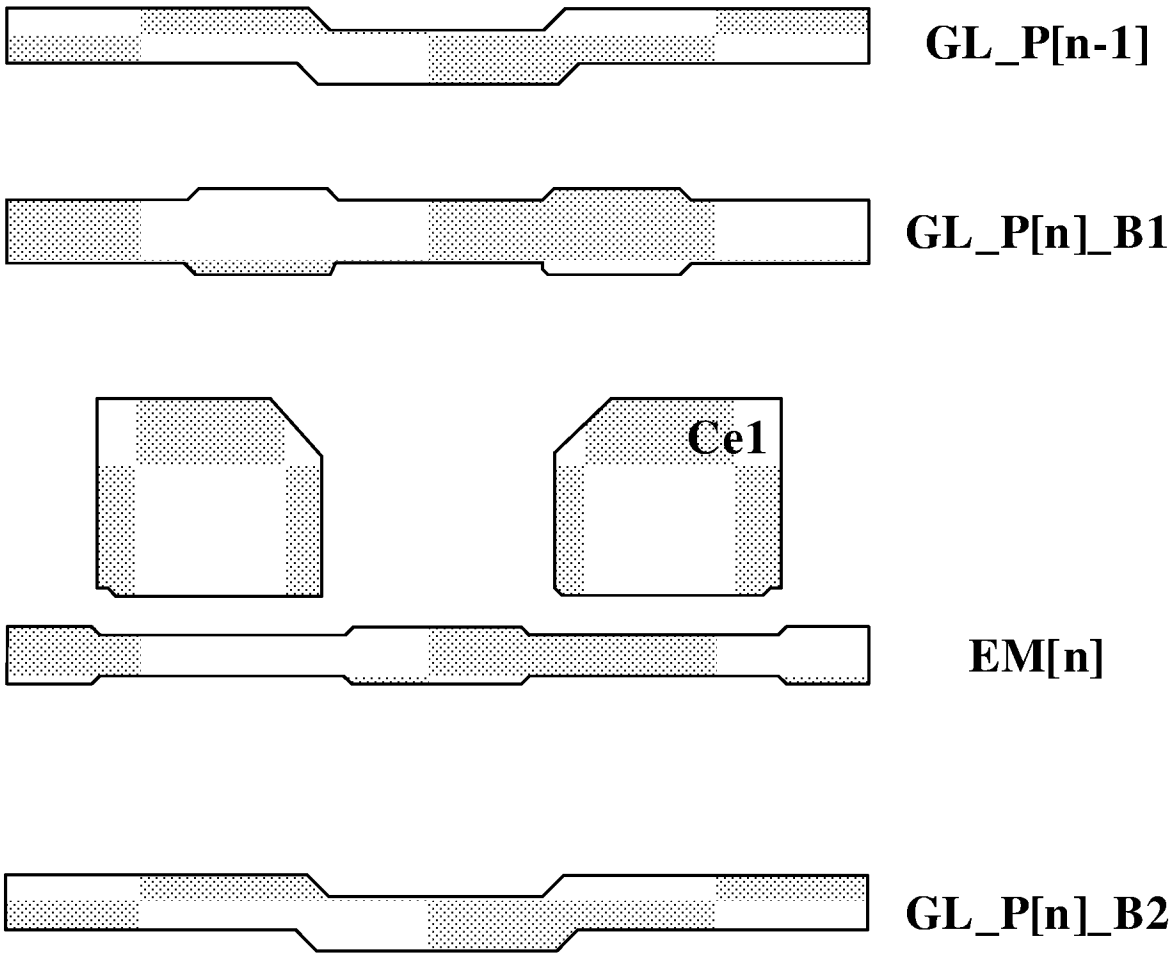

FIG. 3C

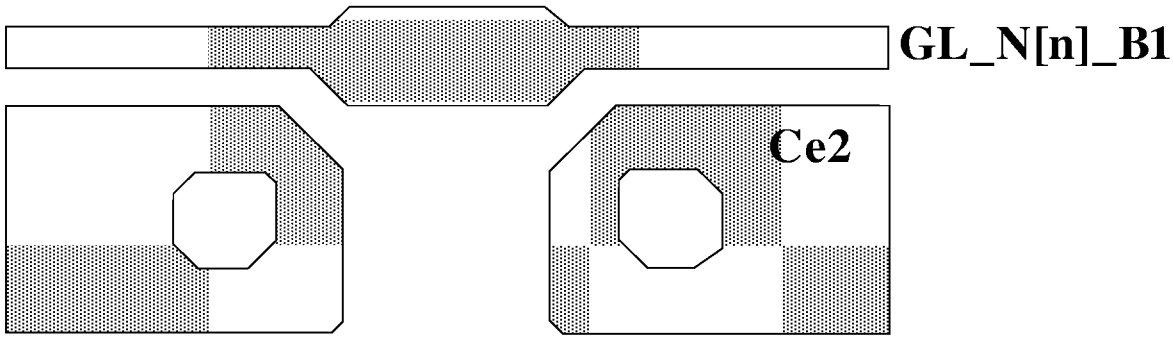

FIG. 3D

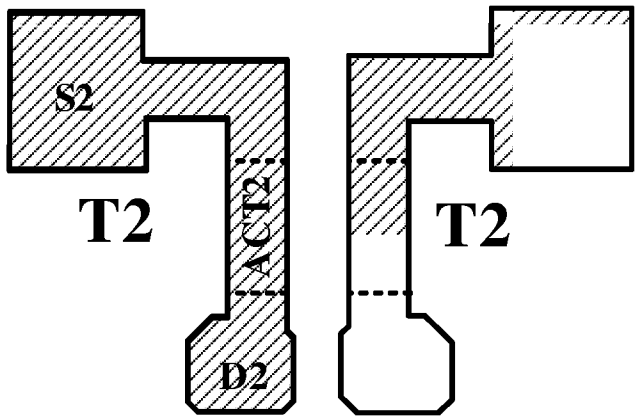

FIG. 3E

FIG. 3F

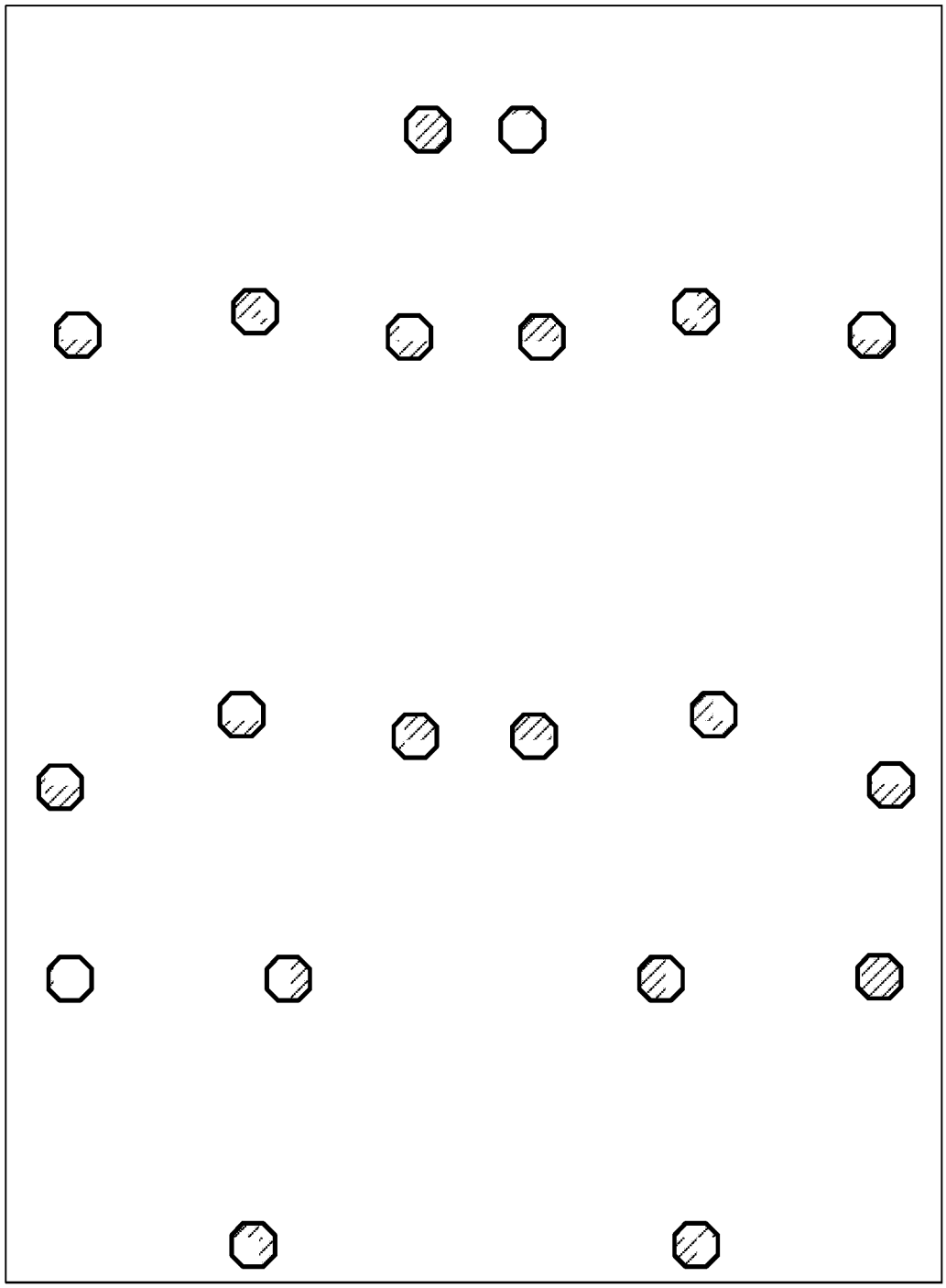

FIG. 3G

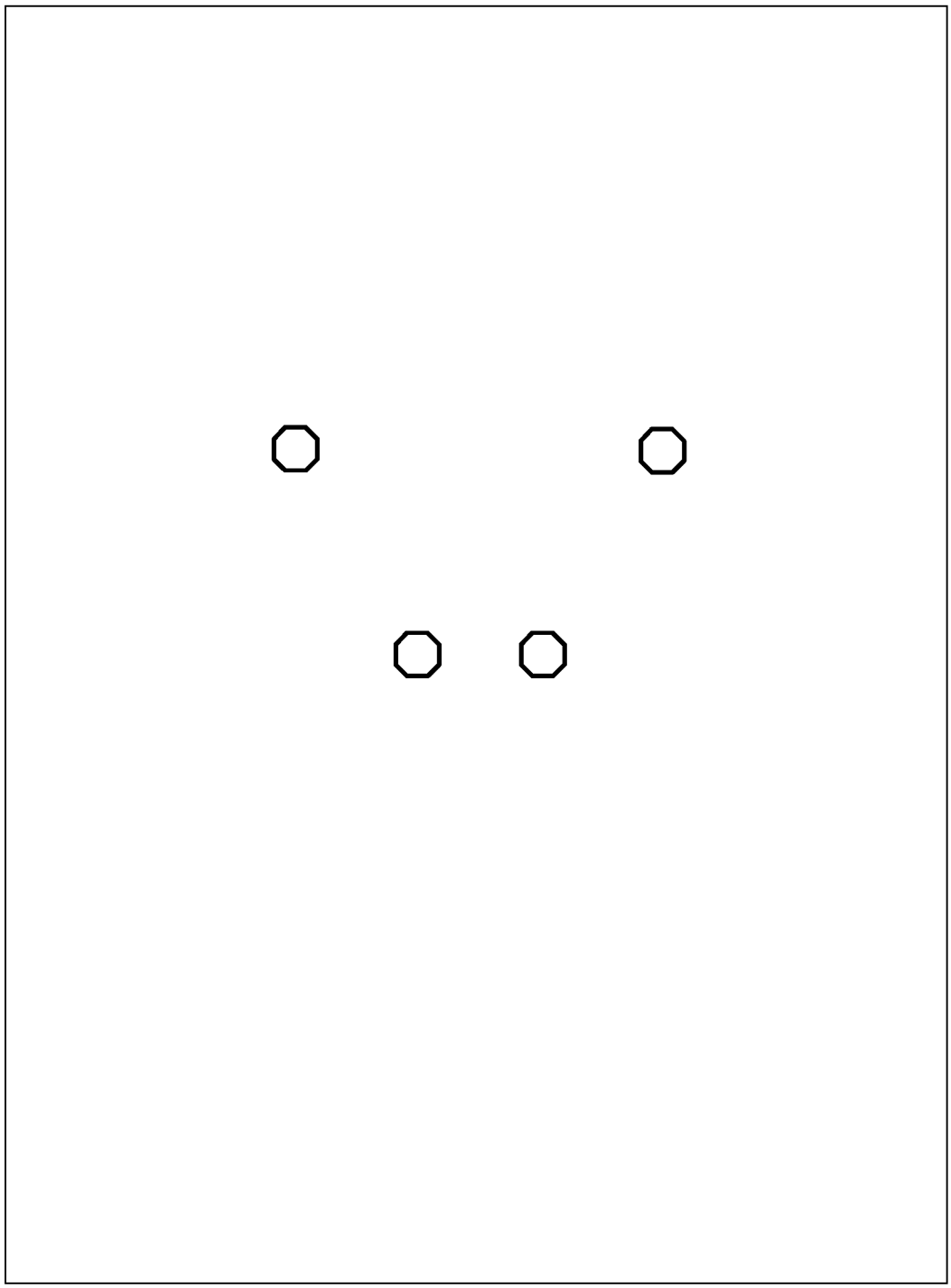

FIG. 3H

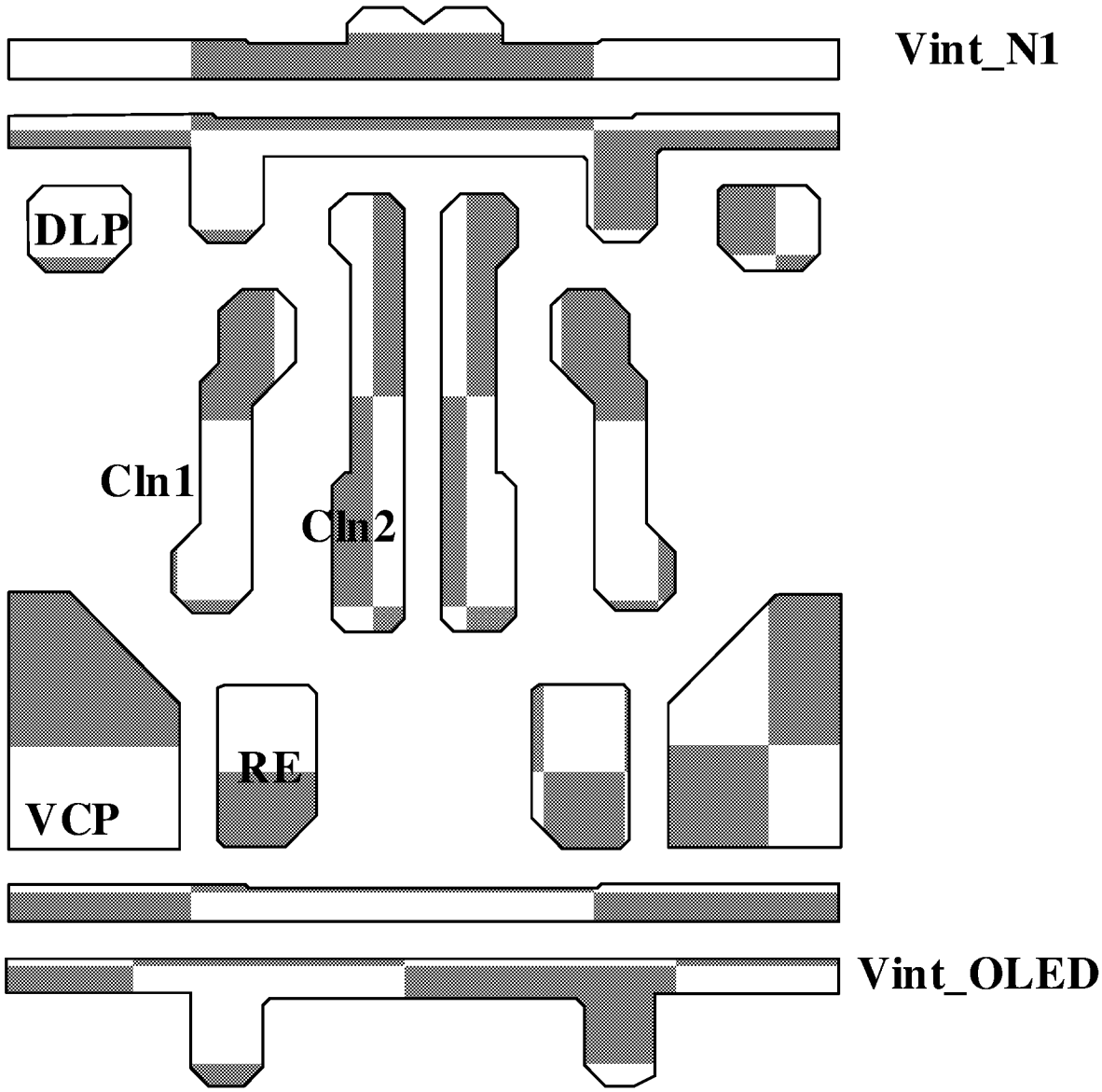

FIG. 3I

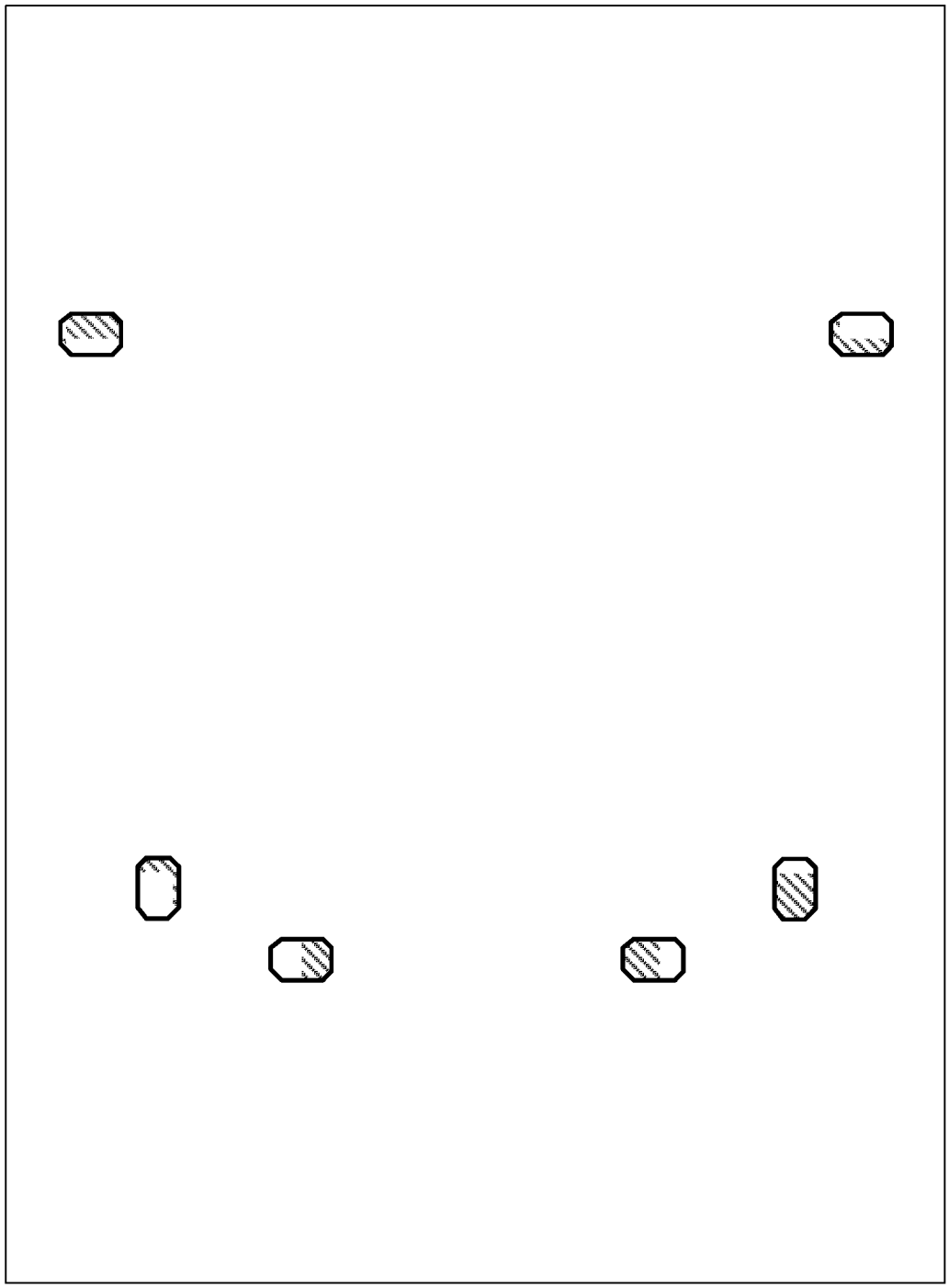

FIG. 3J

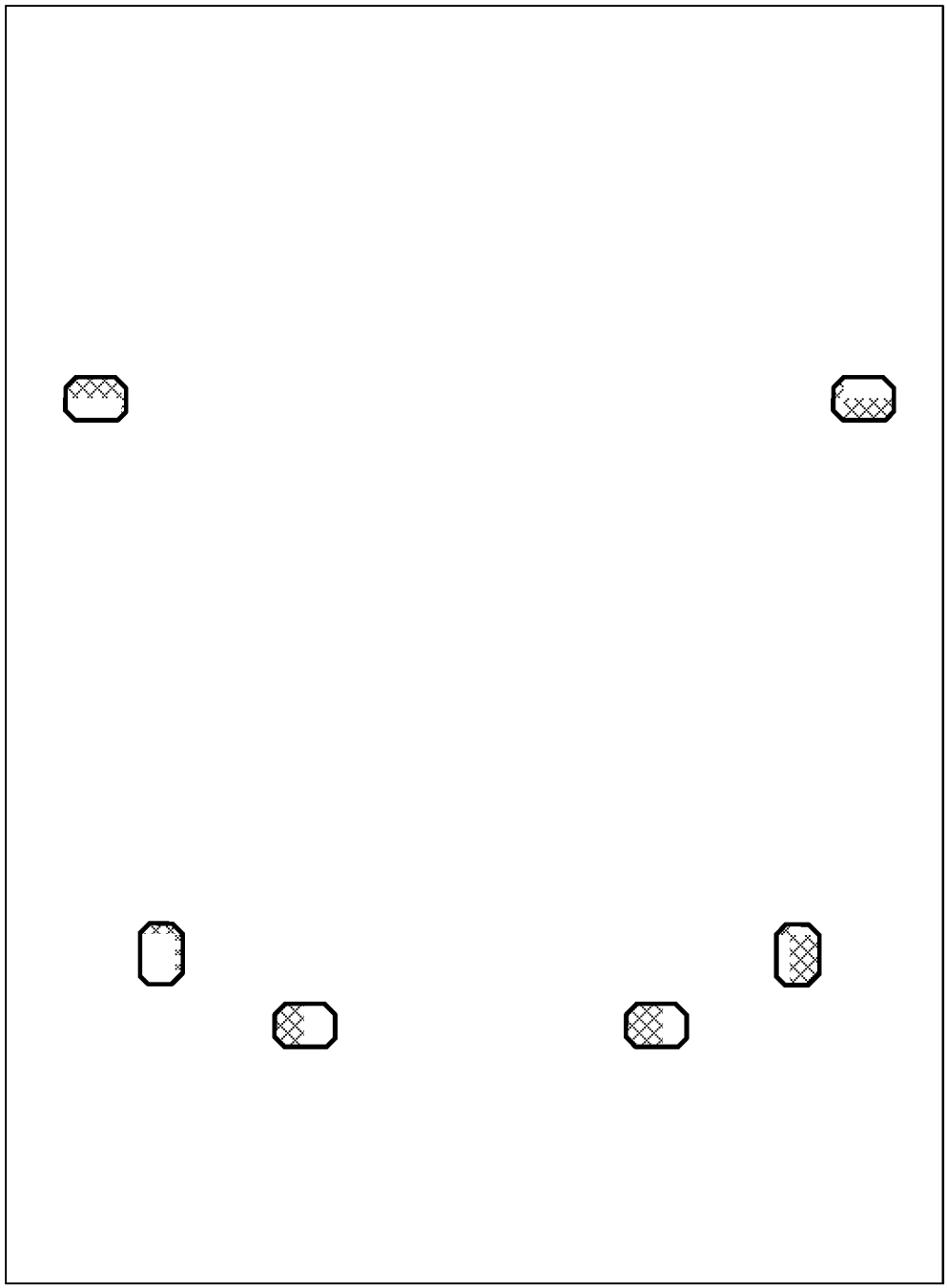

FIG. 3K

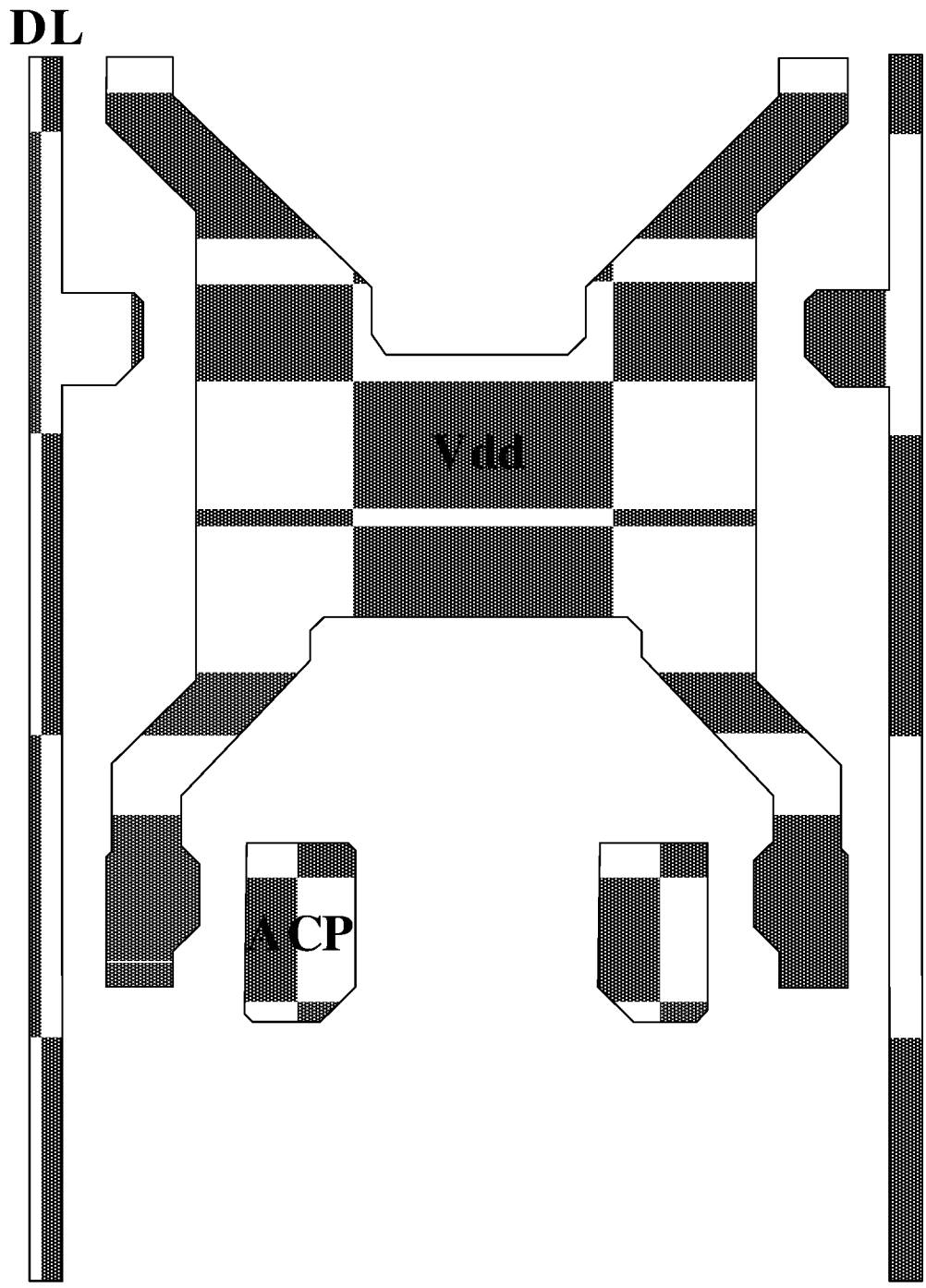

FIG. 3L

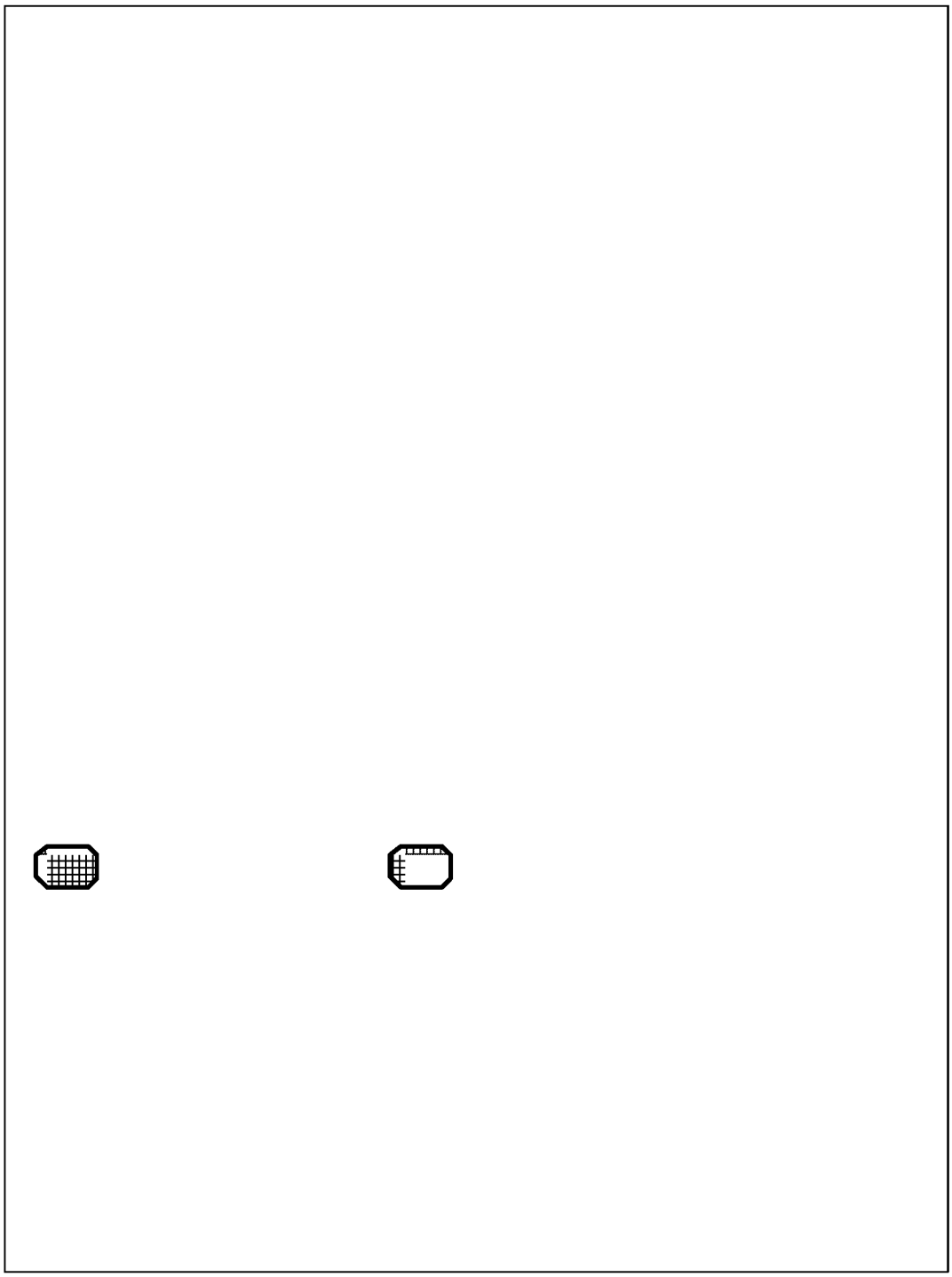

FIG. 3M

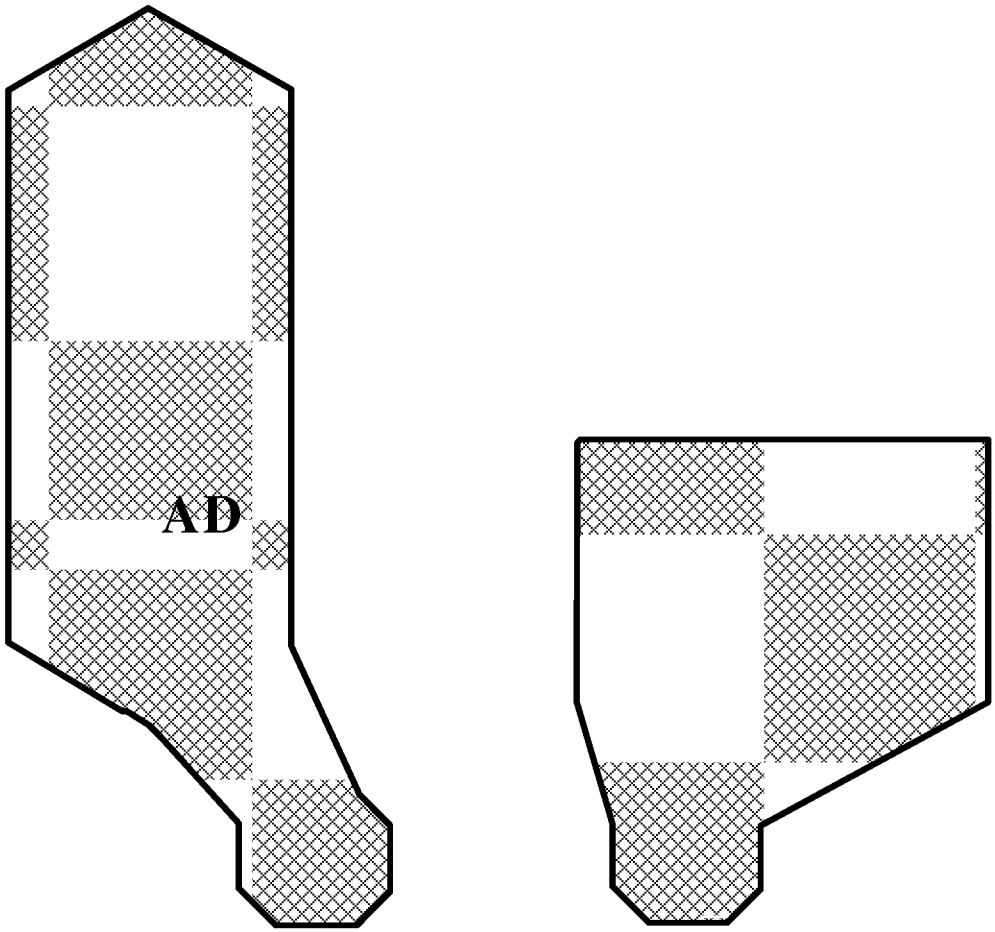

FIG. 3N

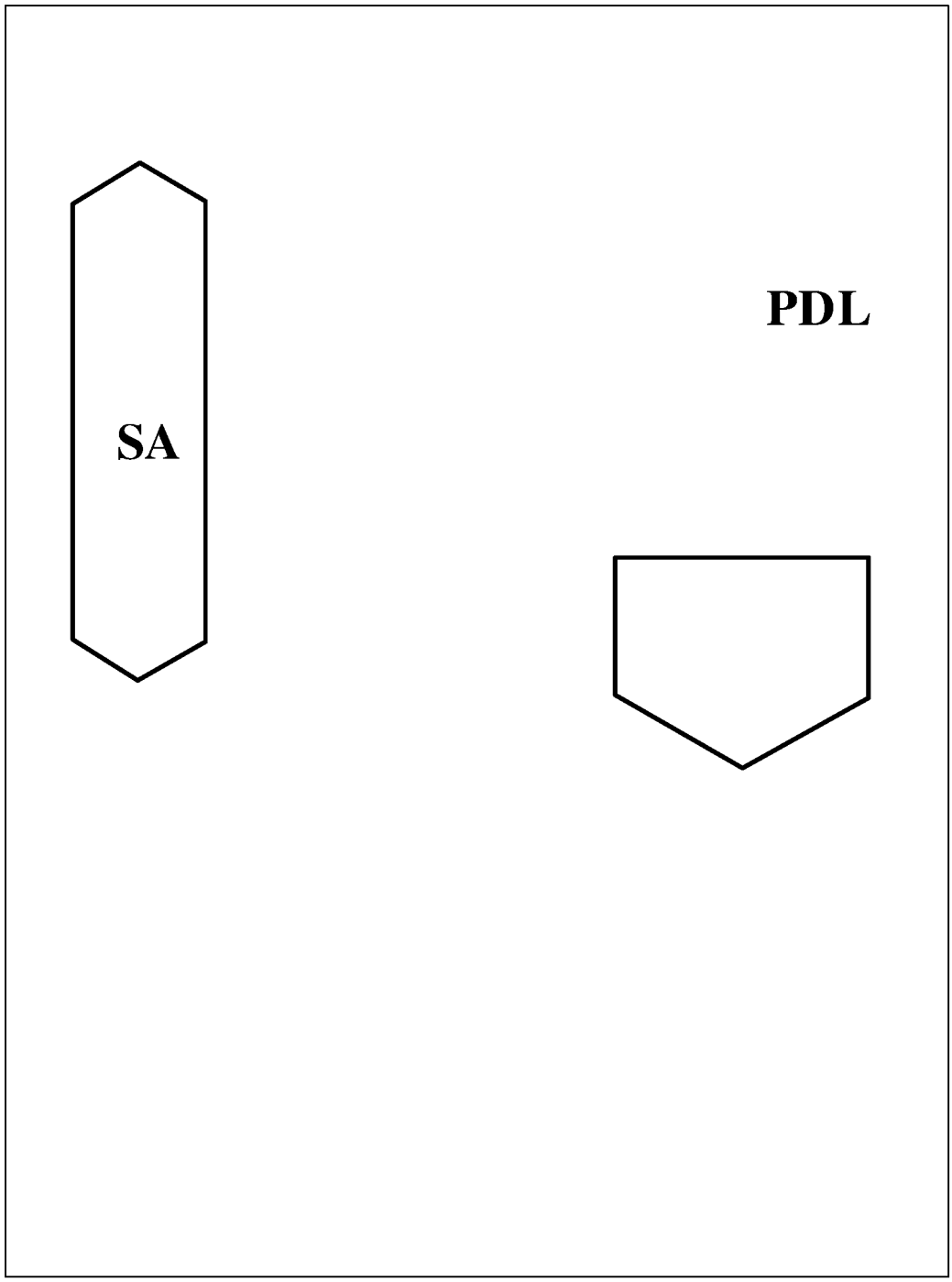

FIG. 3O

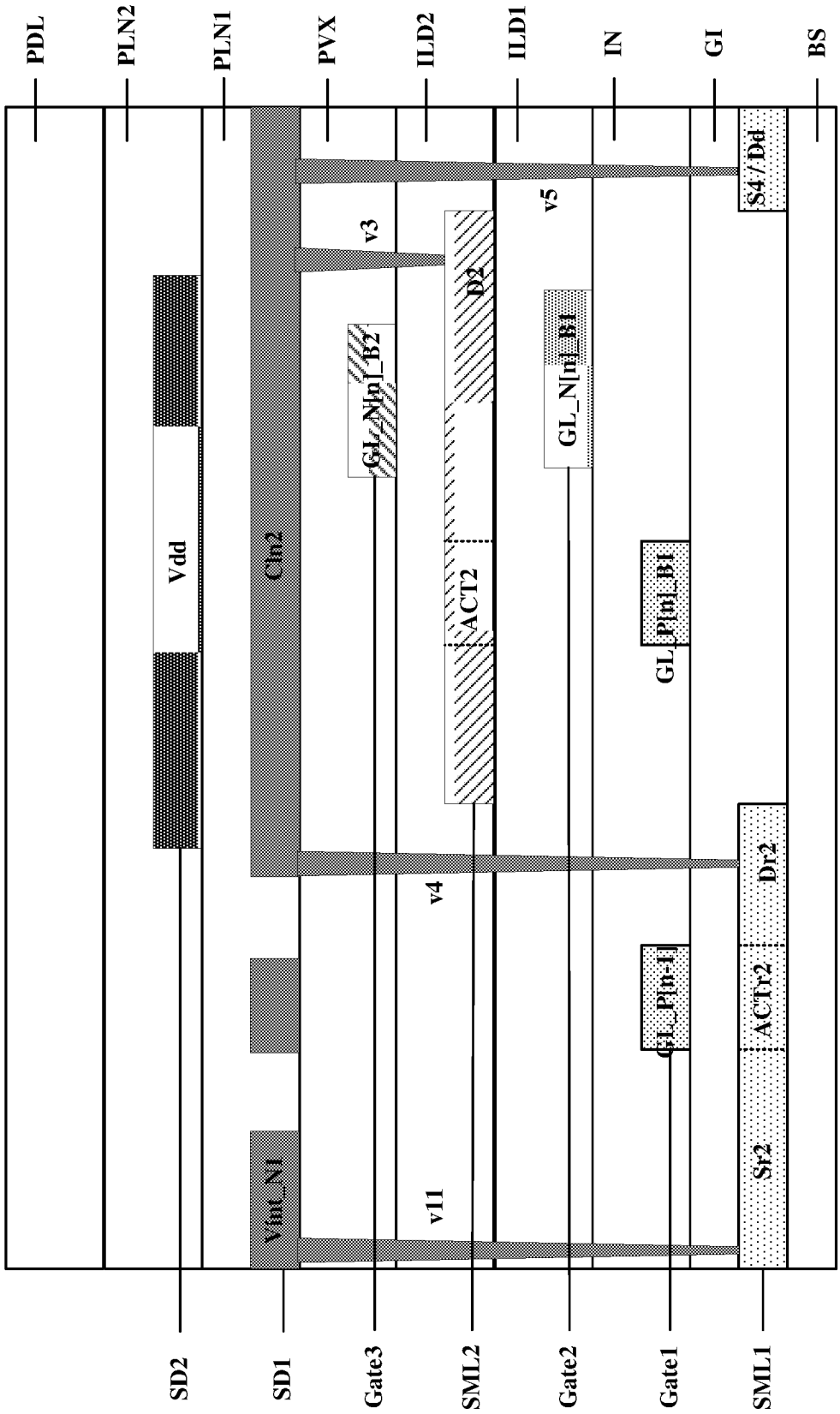
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
Vdd
Cln2
v3
v5
S4 / Dd
D2
GL_Nlp]_B2
GL_N[n]_B1
ACT2
GL_P[n]_B1
v4
Dr2
GL_P[n-1]
ACTr2
Vint_N1
v11
Sr2
SD2
SD1
Gate3
SML2
Gate2
Gate1
SML1

FIG. 4A

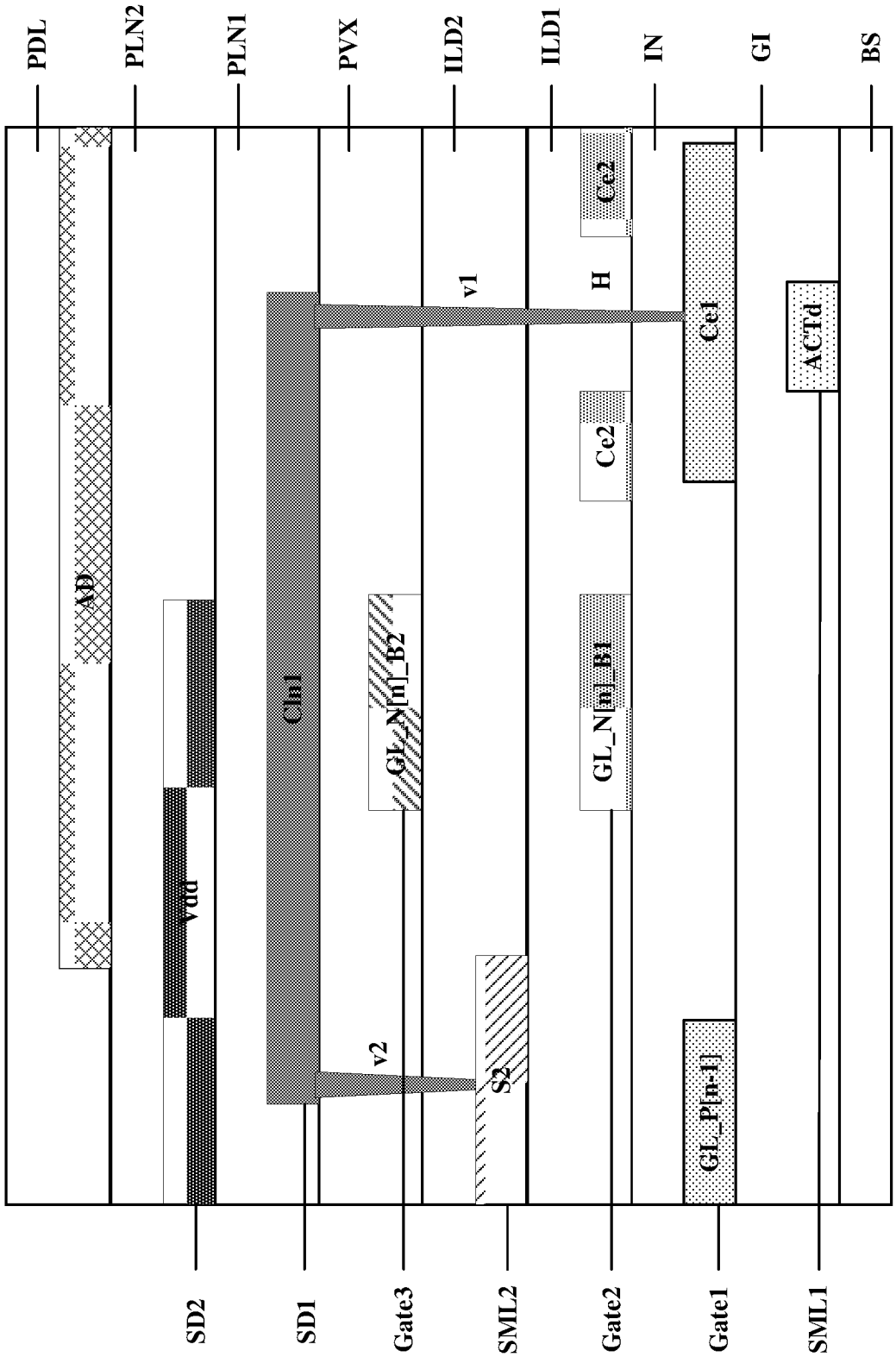
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
AD
Vdd
Cln1
GL_N[n]_B2
v2
S2
v1
H
Ce2
Ce2
GL_N[n]_B1
Ce1
ACTd
G1_P[n-1]
SD2
SD1
Gate3
SML2
Gate2
Gate1
SML1

FIG. 4B

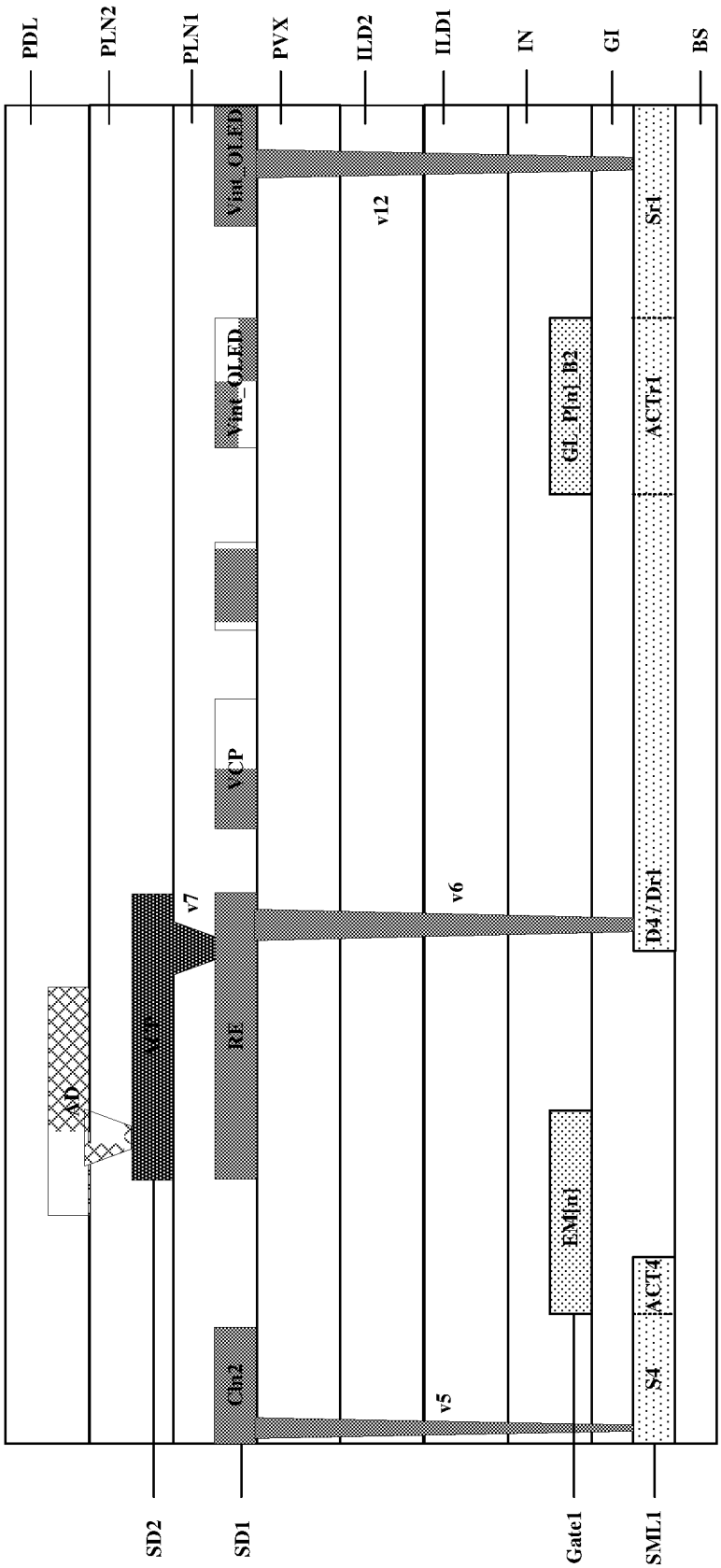
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
Vint_QLED
Vint_QLED
VCP
v12
v7
v6
v5
AD
ADF
RE
Cin2
GI_Pint_B2
EMInt
ACTr1
Sr1
D4/Dr1
S4
ACT4
SD2
SD1
Gate1
SML1

FIG. 4C

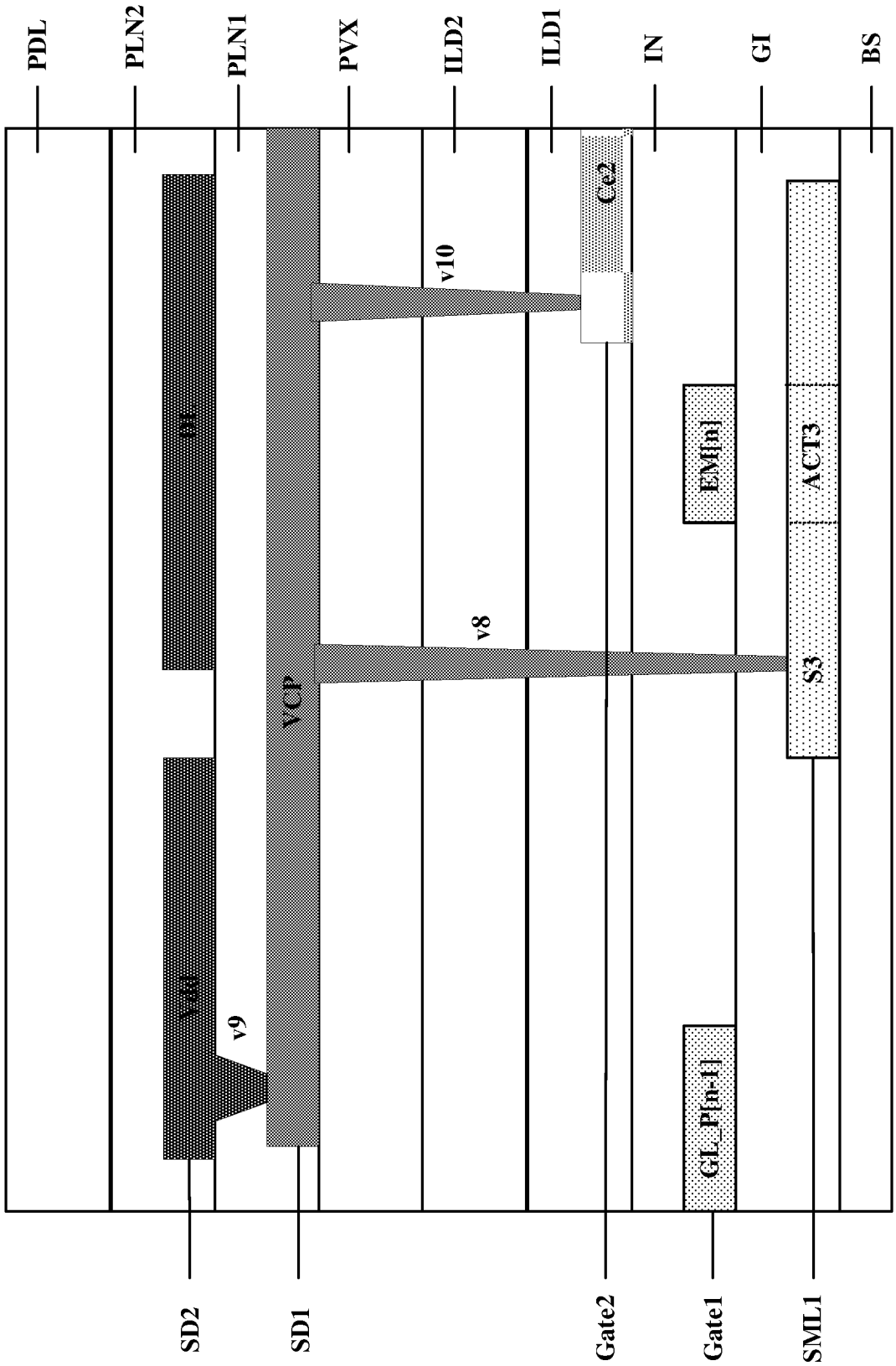
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
v10
Ce2
v8
EM[n]
ACT3
S3
VCP
v9
GL_P[n-1]
SD2
SD1
Gate2
Gate1
SML1

FIG. 4D

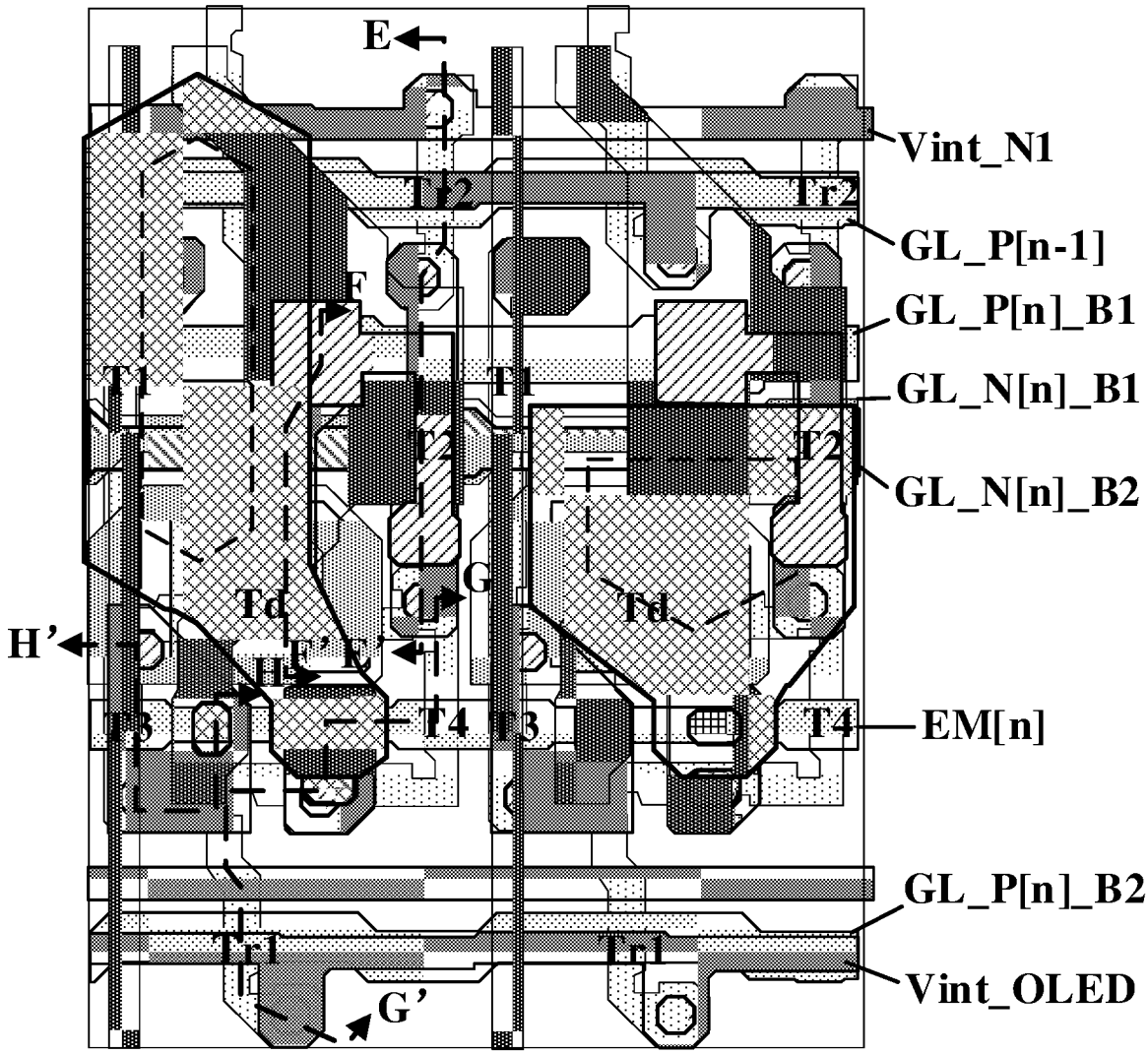
E
Vint_N1
Tr2
Tr2
GL_P[n-1]
F
GL_P[n]_B1
T1
T1
GL_N[n]_B1
T2
T2
GL_N[n]_B2
G
Td
Td
H'
E'
F'
H
T3
T4
T3
T4
EM[n]
GL_P[n]_B2
Tr1
Tr1
Vint_OLED
G'

FIG. 5A

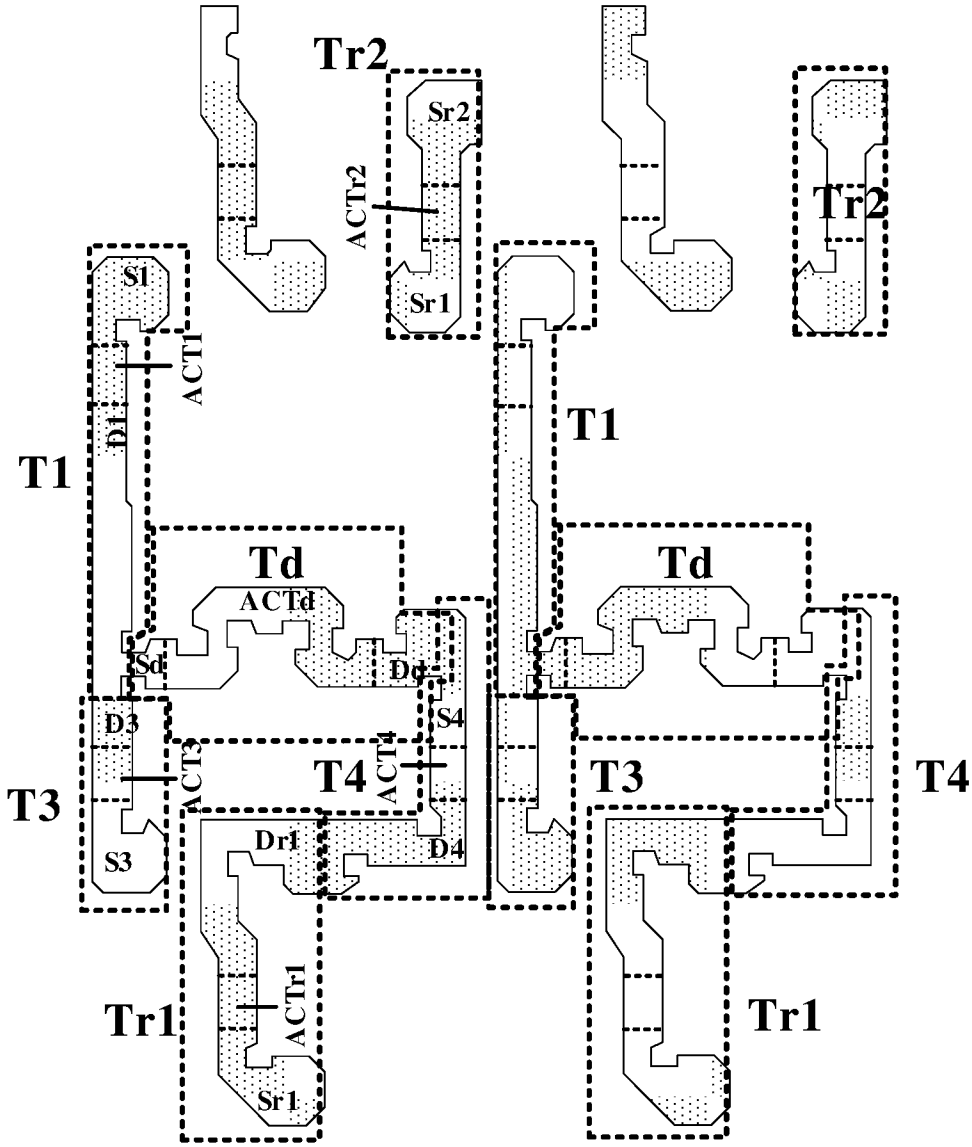
Tr2
Sr2
ACTr2
Sr1
Tr2
S1
ACT1
D1
T1
T1
Td
ACTd
Sd
Dd
Td
D3
S4
T3
ACT3
T4
ACT4
T3
T4
Dr1
D4
S3
Tr1
ACTr1
Sr1
Tr1

FIG. 5B

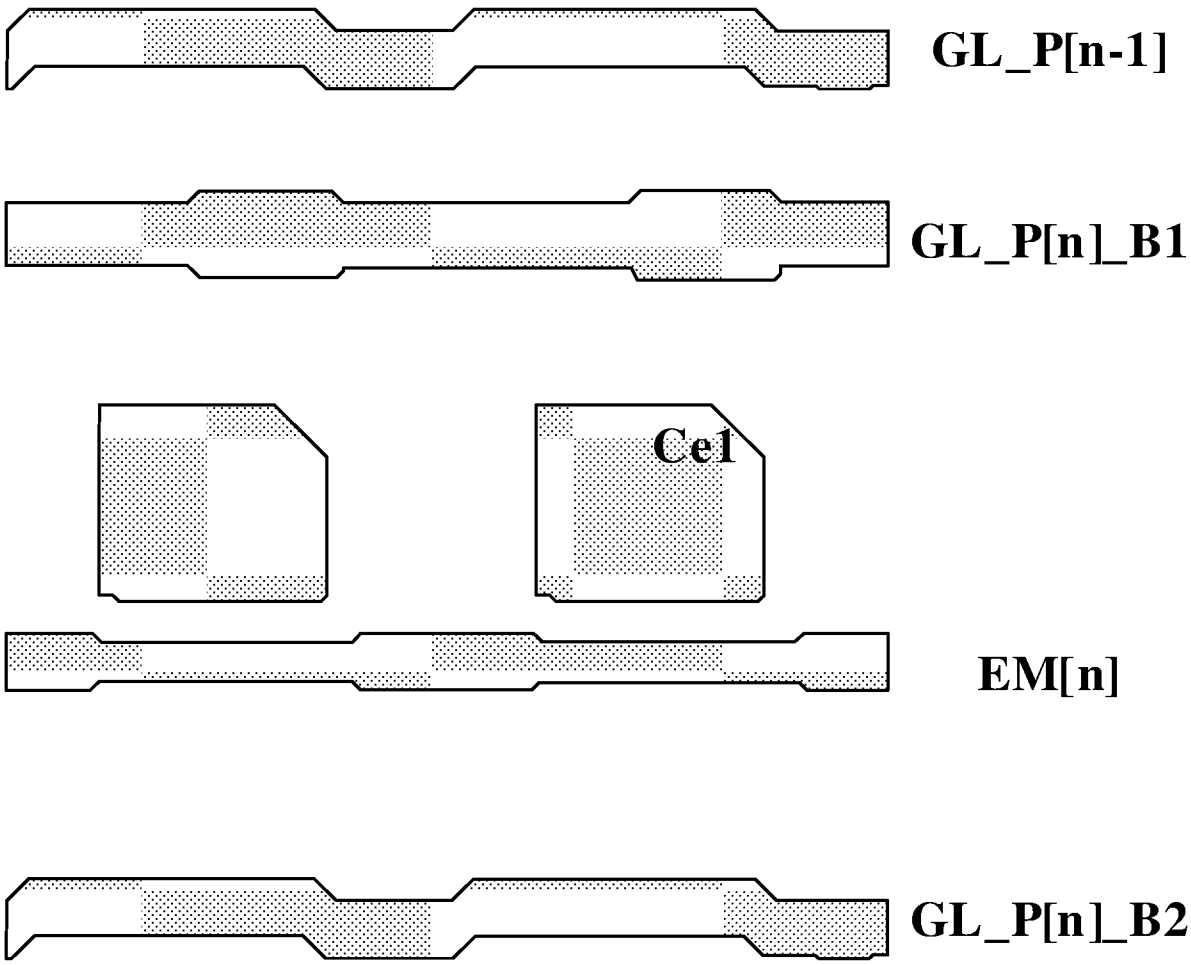

FIG. 5C

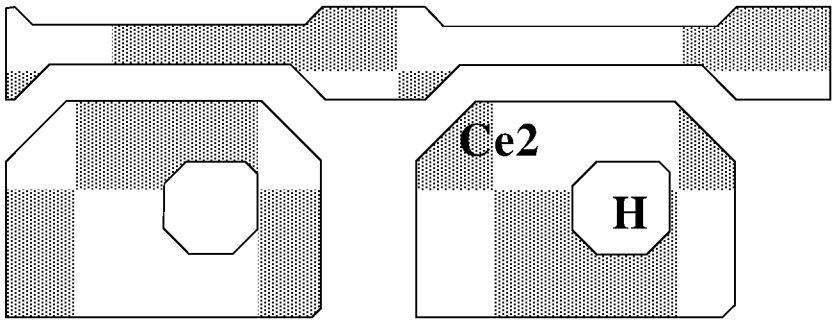

FIG. 5D

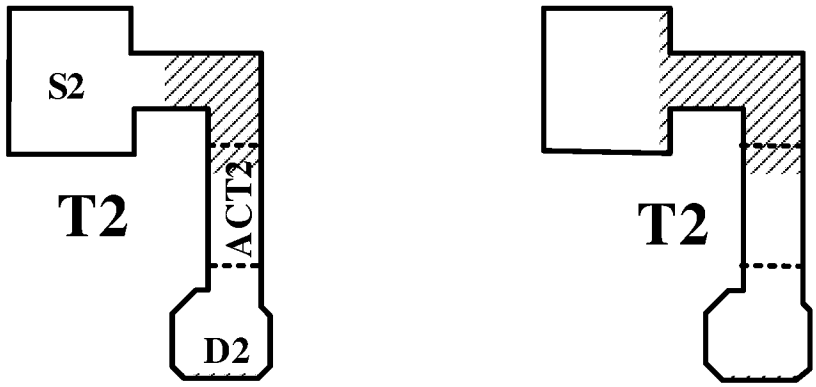

FIG. 5E

FIG. 5F

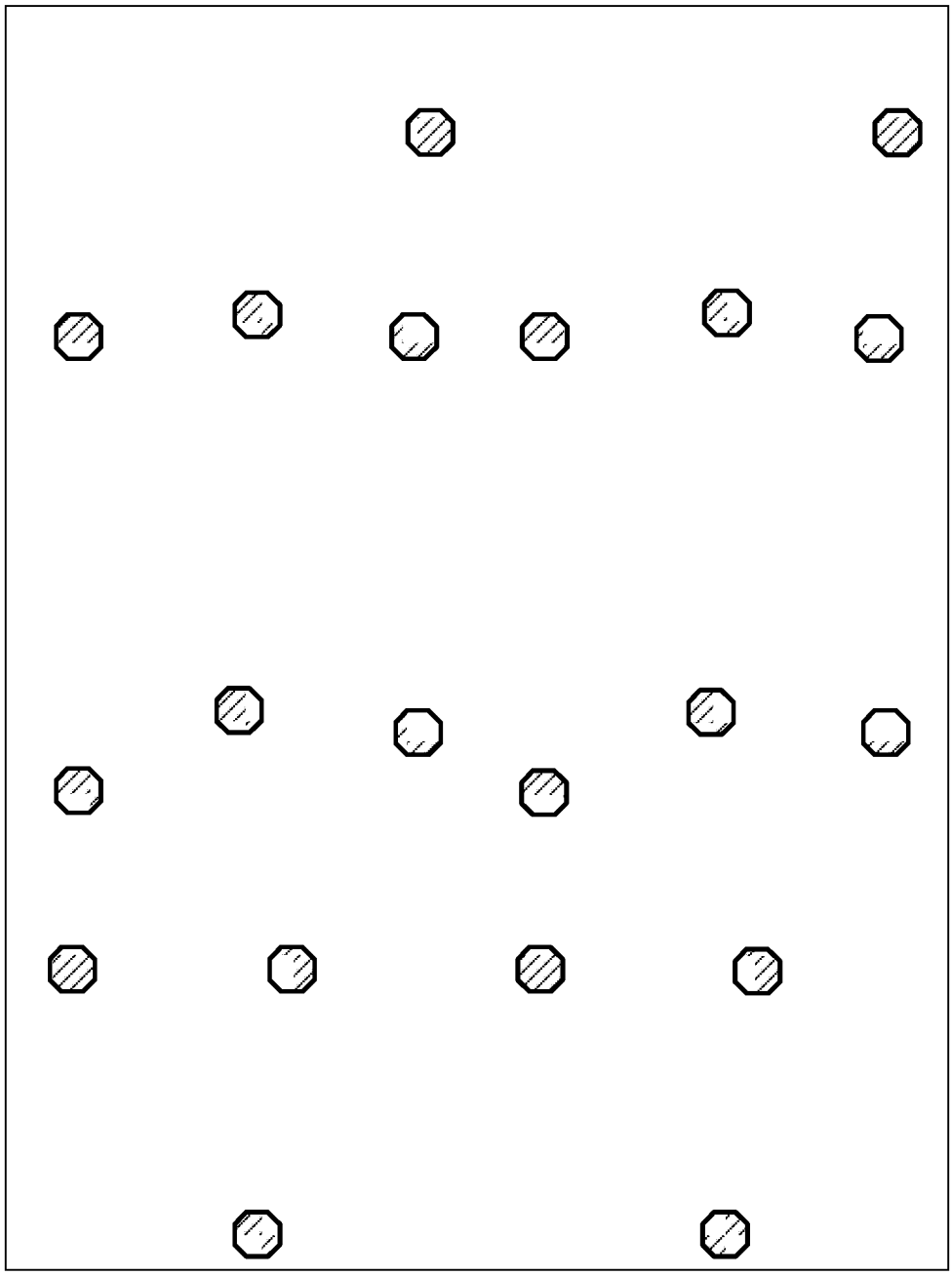

FIG. 5G

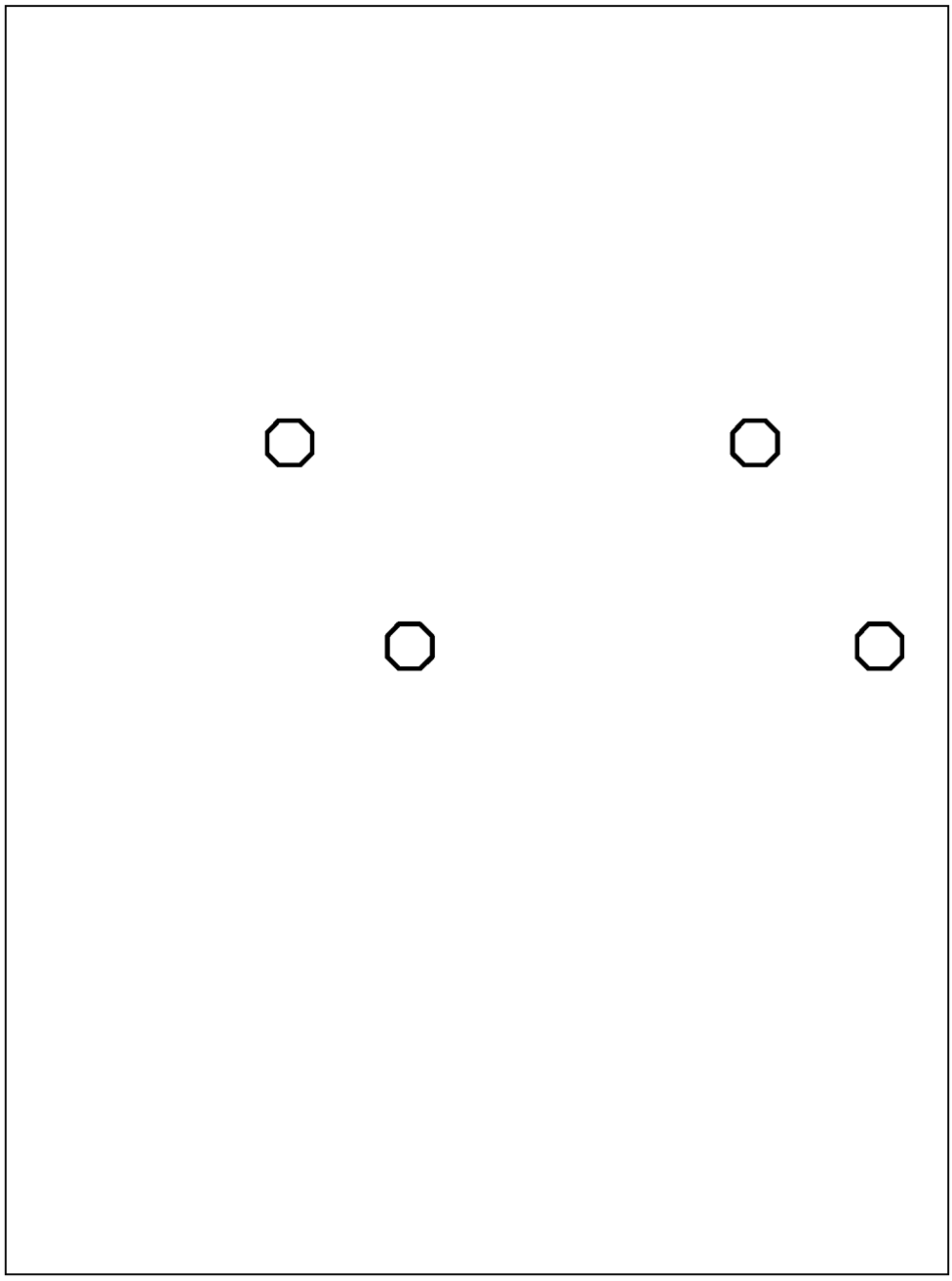

FIG. 5H

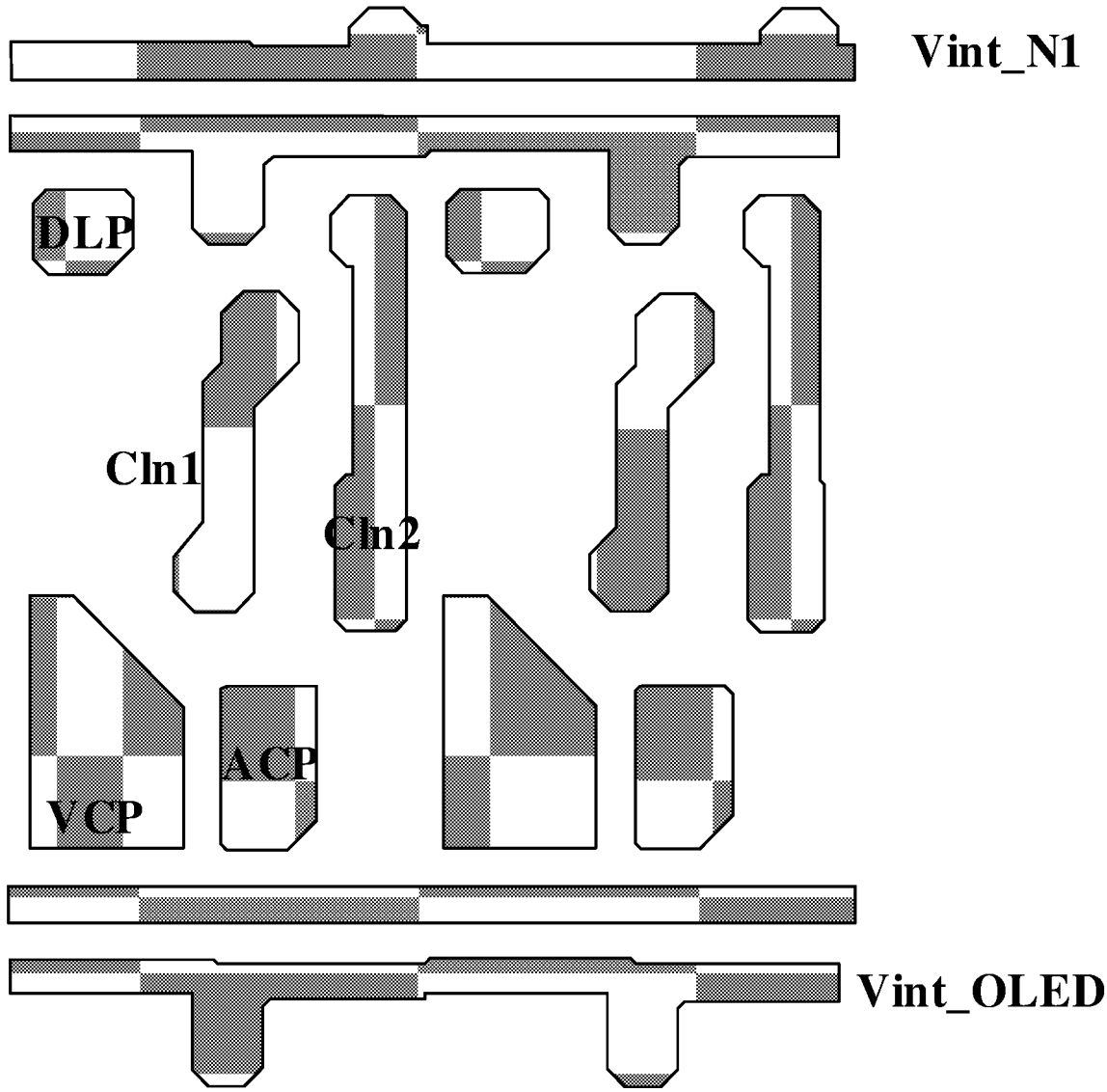

FIG. 5I

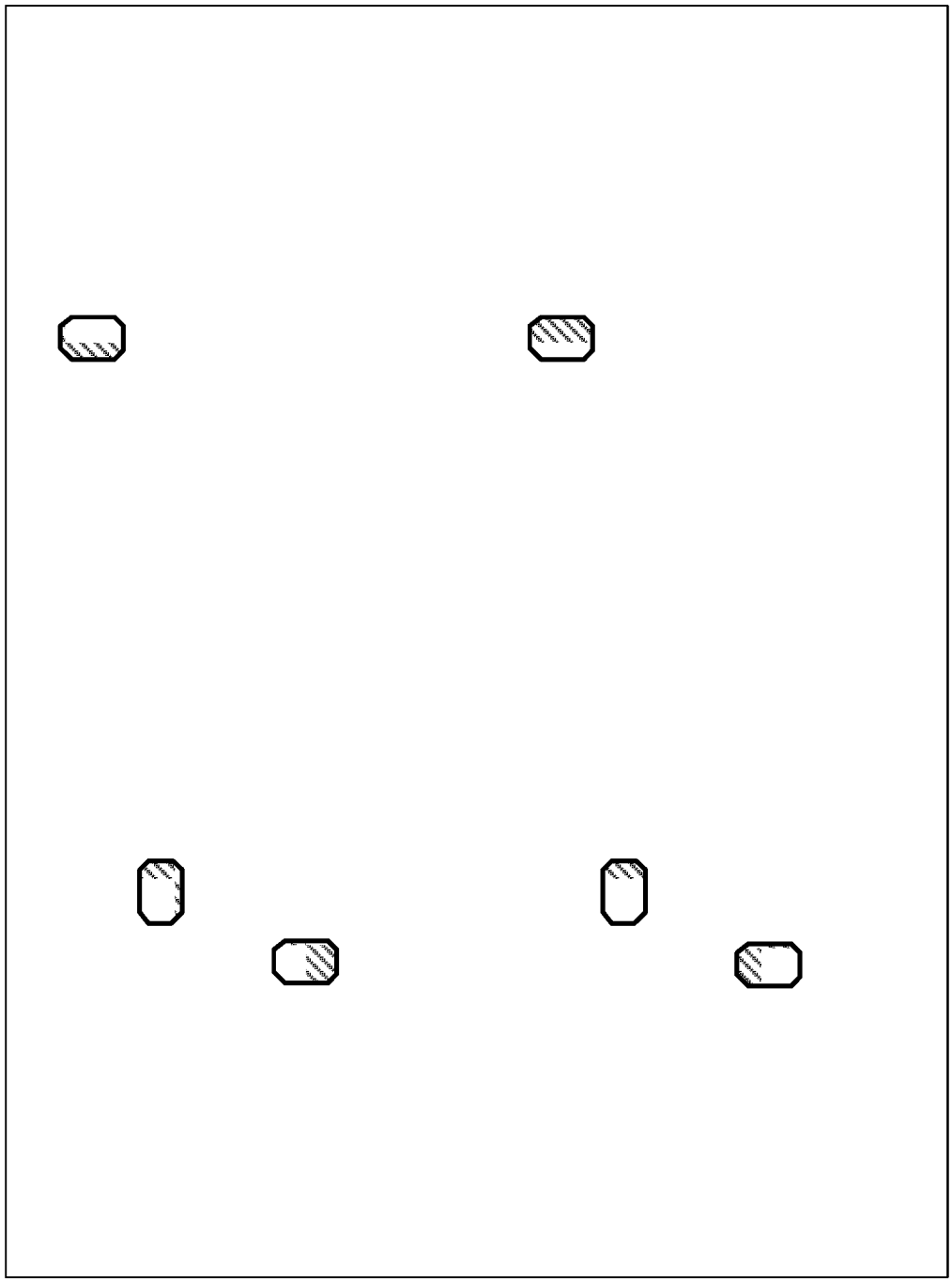

FIG. 5J

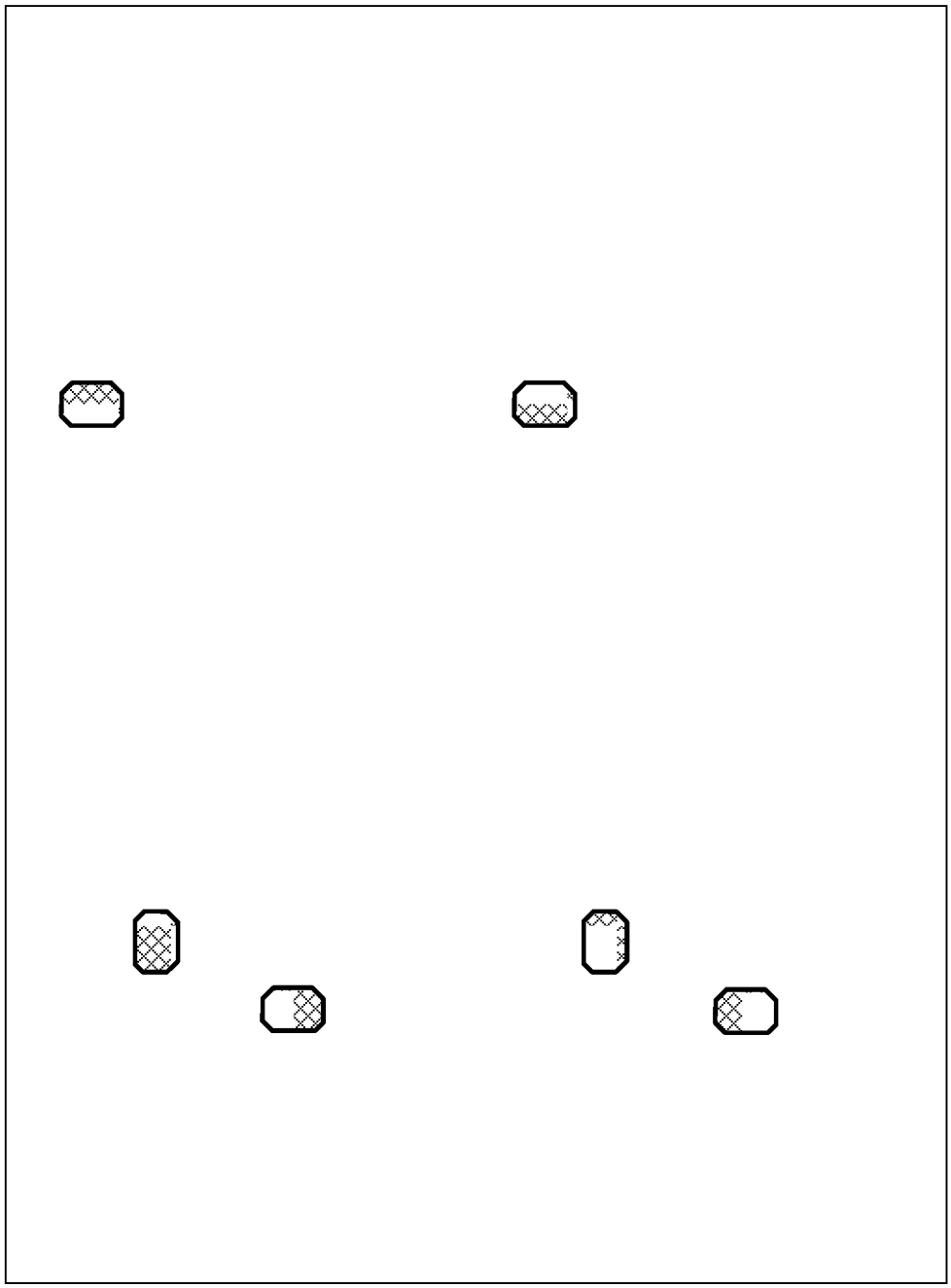

FIG. 5K

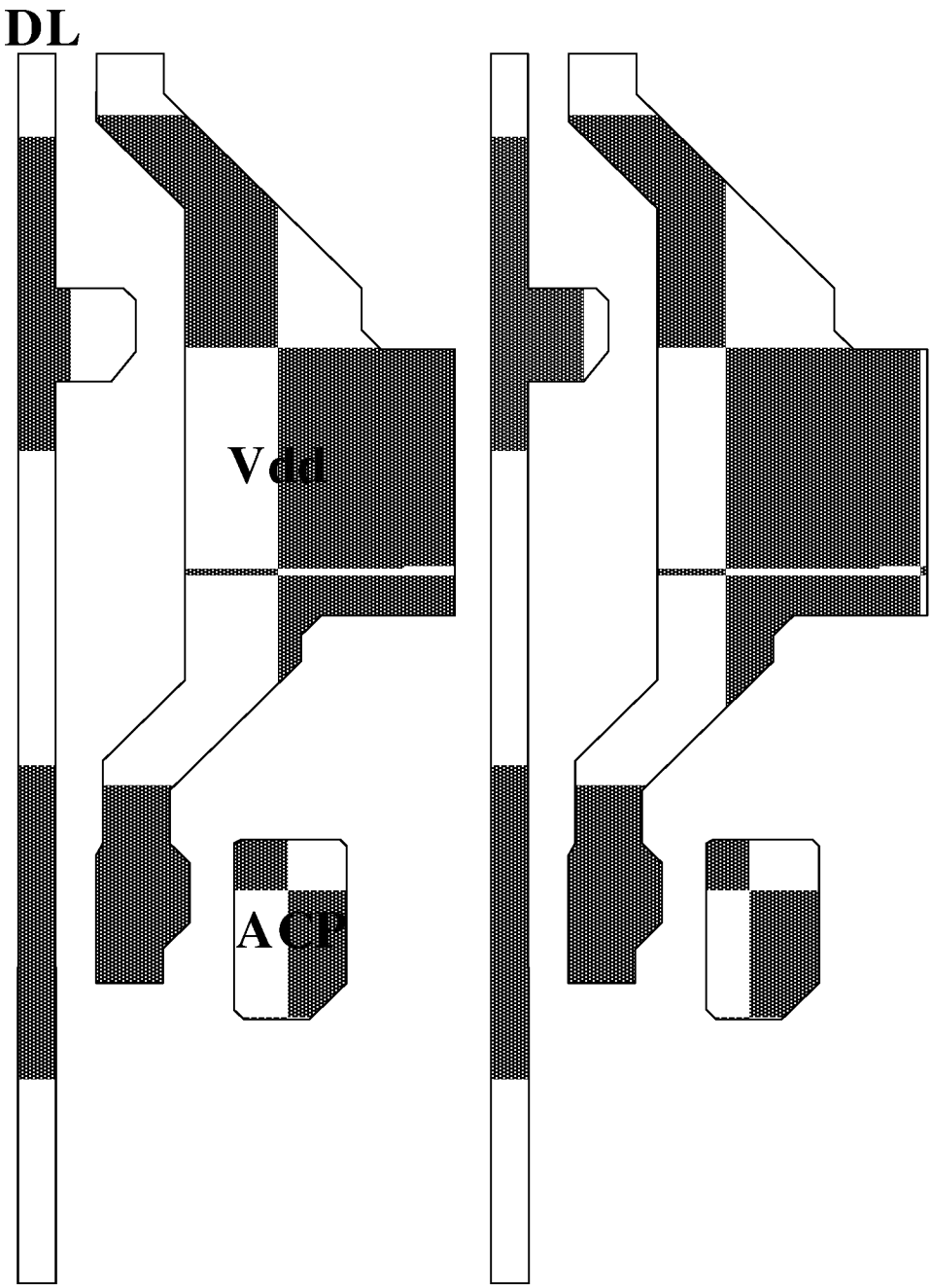

FIG. 5L

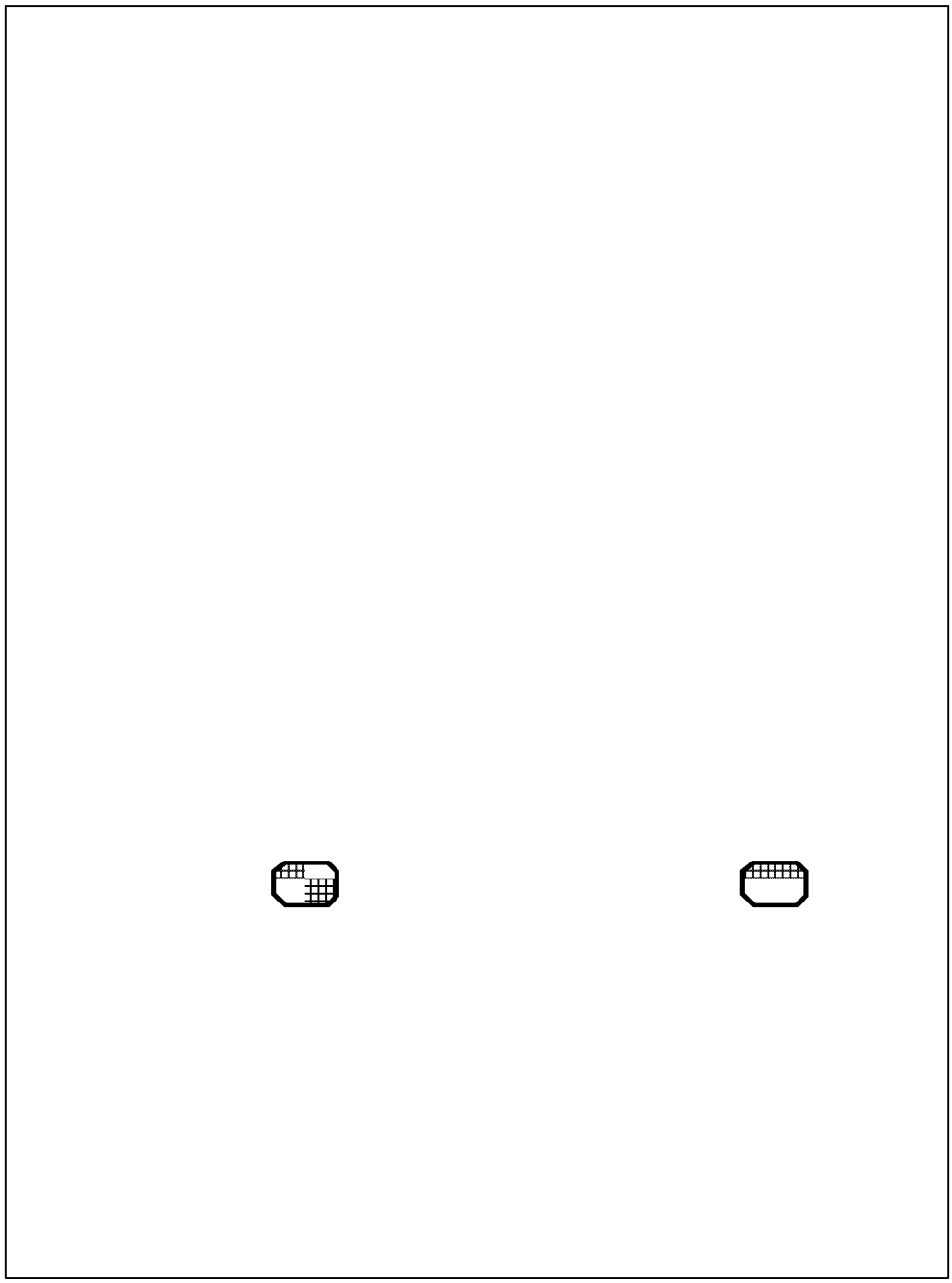

FIG. 5M

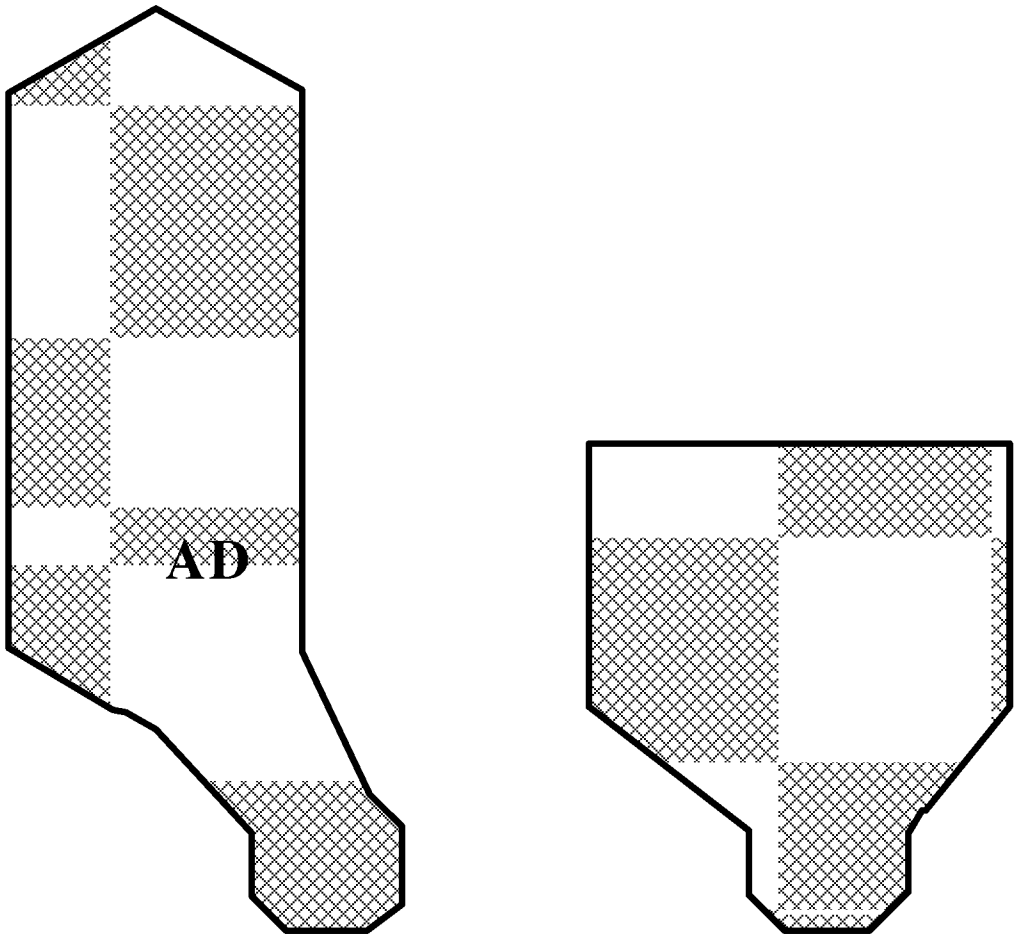

FIG. 5N

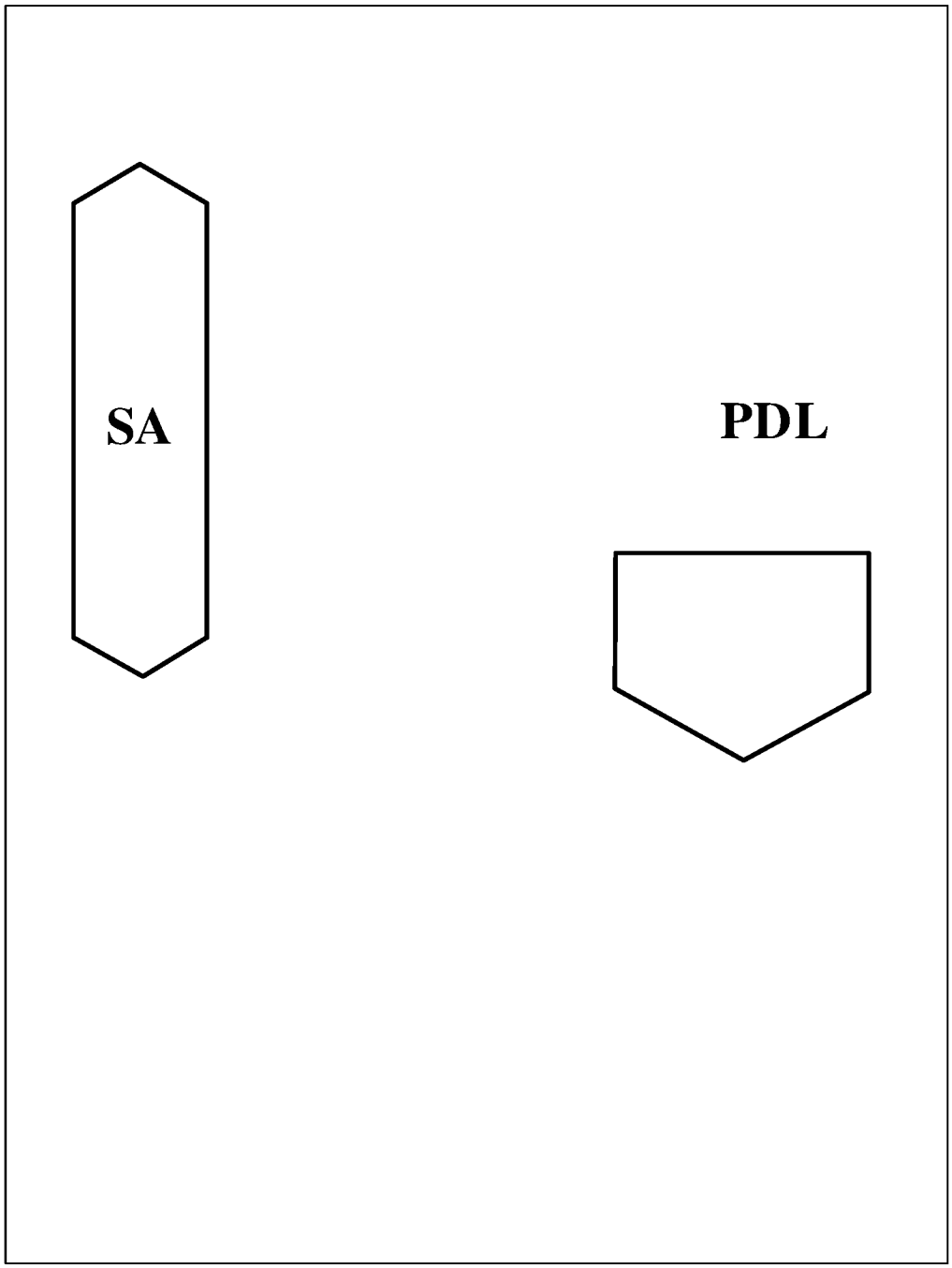

FIG. 5O

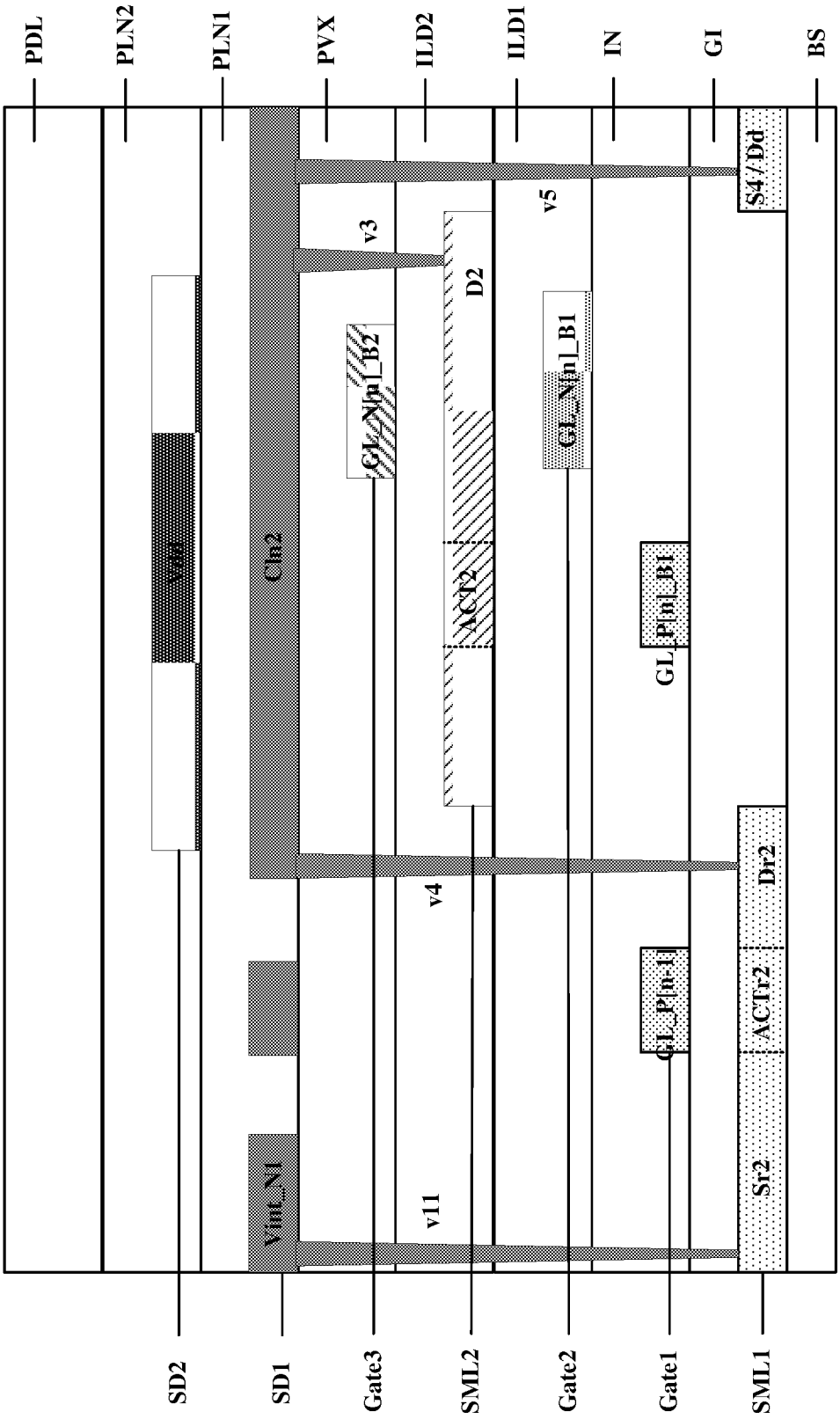
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
SD2
SD1
Gate3
SML2
Gate2
Gate1
SML1
Vdd
Chr2
Vmt_N1
v3
v4
v11
v5
D2
ACCr2
GL_Nn1_B2
GL_Nn1_B1
GL_Pin1_B1
GL_Pin-1
S4 / Dd
Dr2
ACTr2
Sr2

FIG. 6A

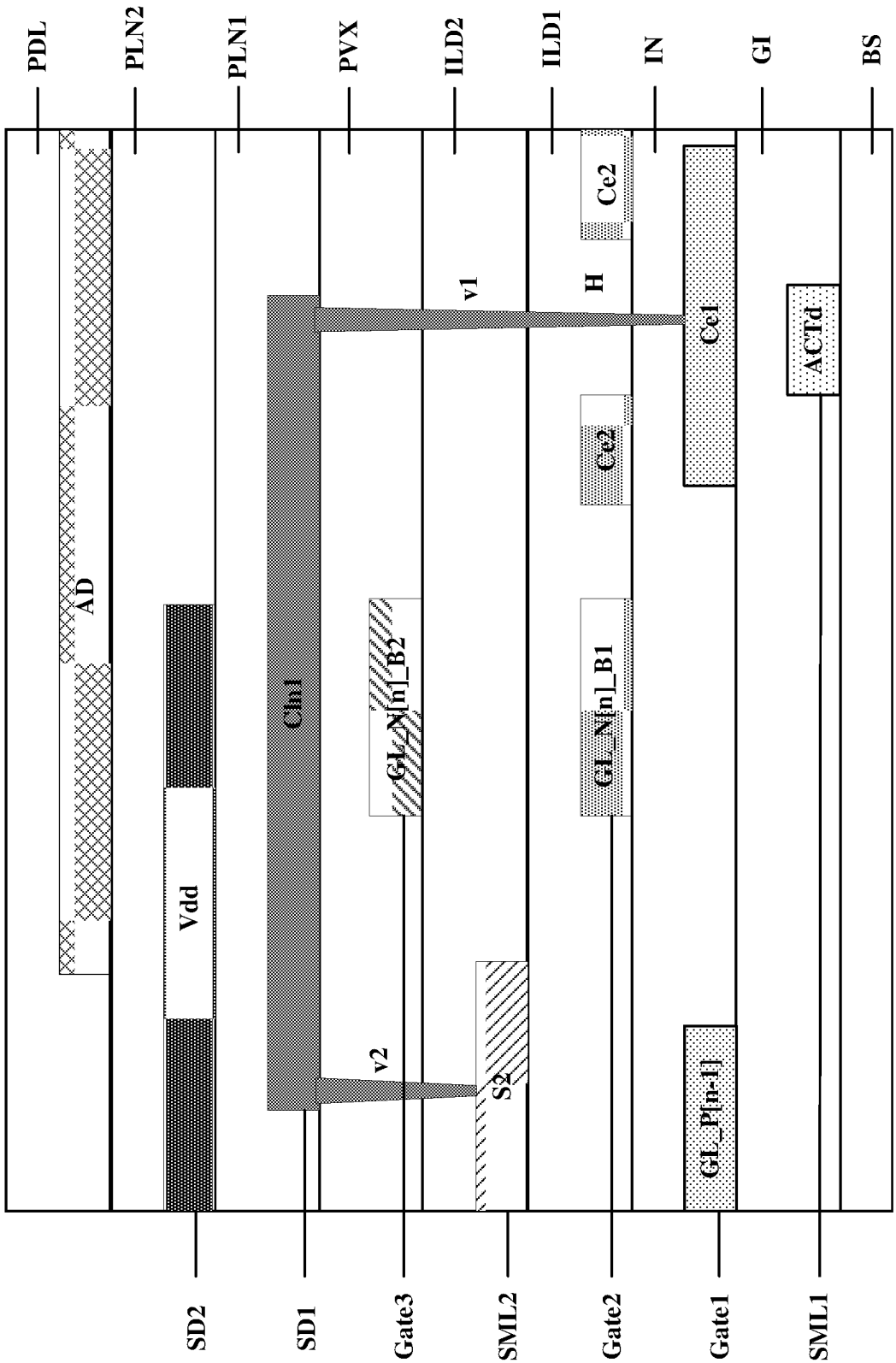
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
AD
Vdd
Cln1
GL_N[n]_B2
v1
v2
S2
H
Ce2
Ce2
GL_N[n]_B1
Ce1
ACTd
GL_P[n-1]
SD2
SD1
Gate3
SML2
Gate2
Gate1
SML1

FIG. 6B

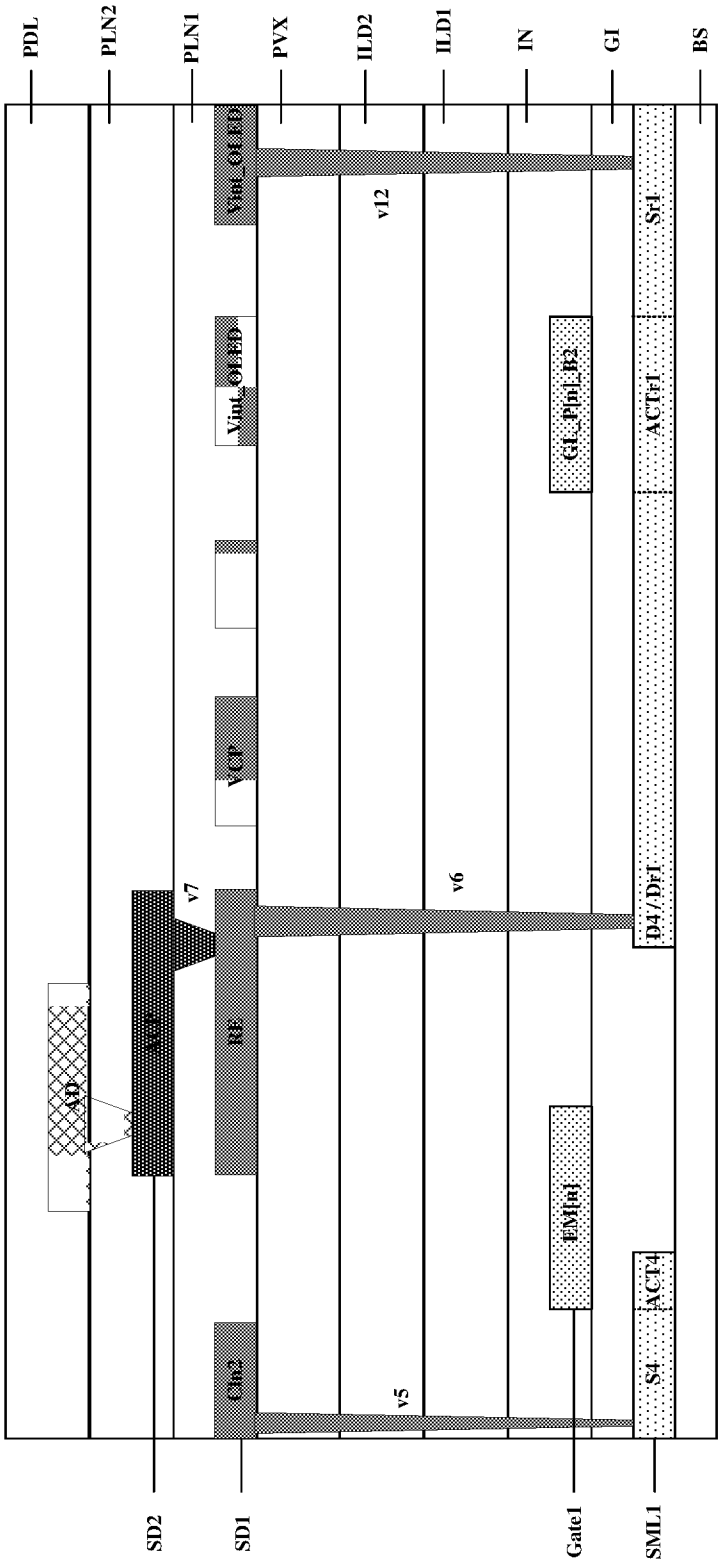
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
Vint_OLED
Vint_OLED
VCP
RE
AD
v7
v12
v6
v5
G1_Pint_B2
ACTrT
Sr1
D4/DrT
EMint1
Cin2
S4
ACT4
SD2
SD1
Gate1
SML1

FIG. 6C

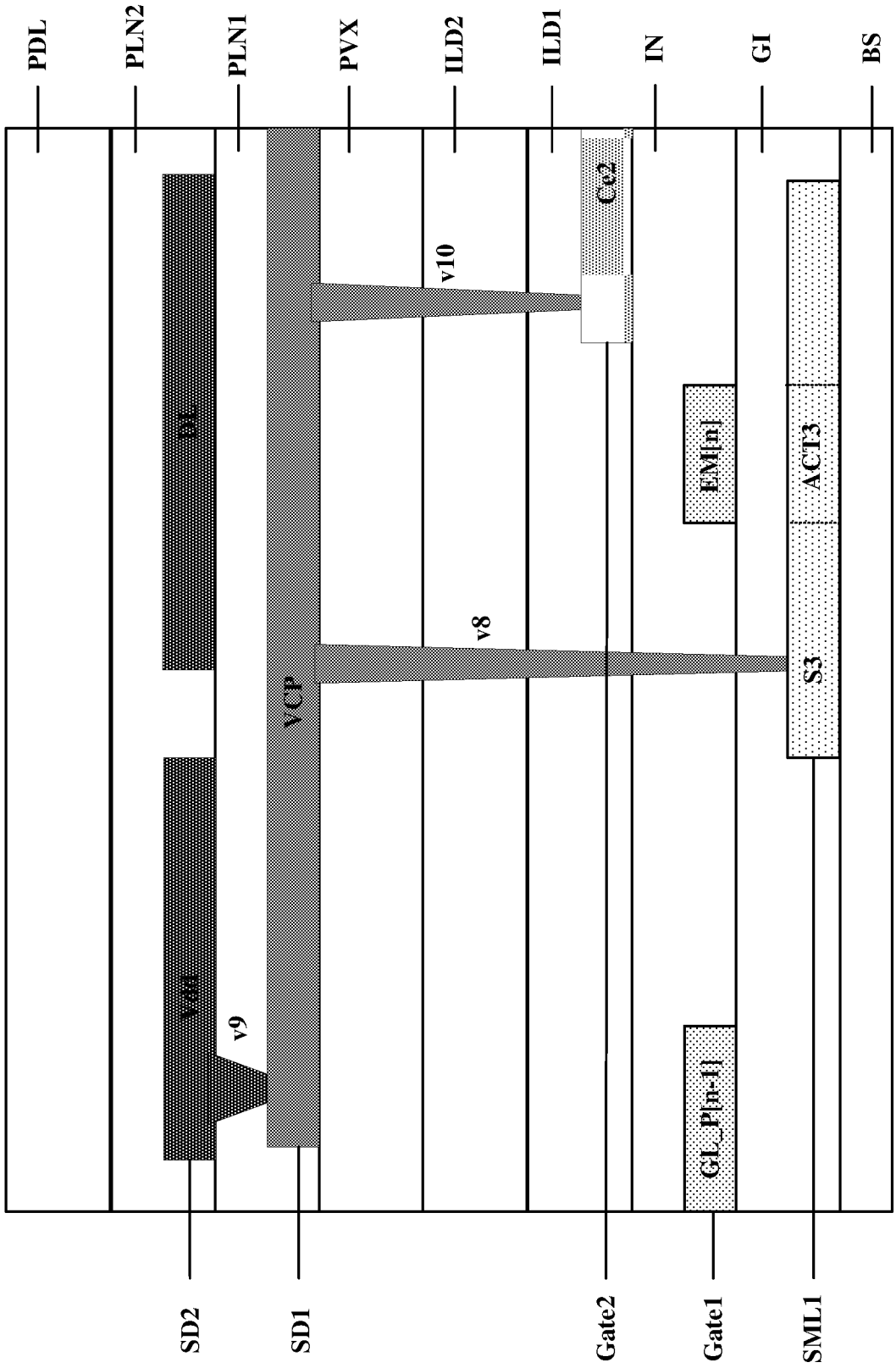
PDL
PLN2
PLN1
PVX
ILD2
ILD1
IN
GI
BS
DL
VCP
Ve1
v9
v10
v8
Ce2
EMn1
ACT3
S3
GL_Pln-11
SD2
SD1
Gate2
Gate1
SML1

FIG. 6D

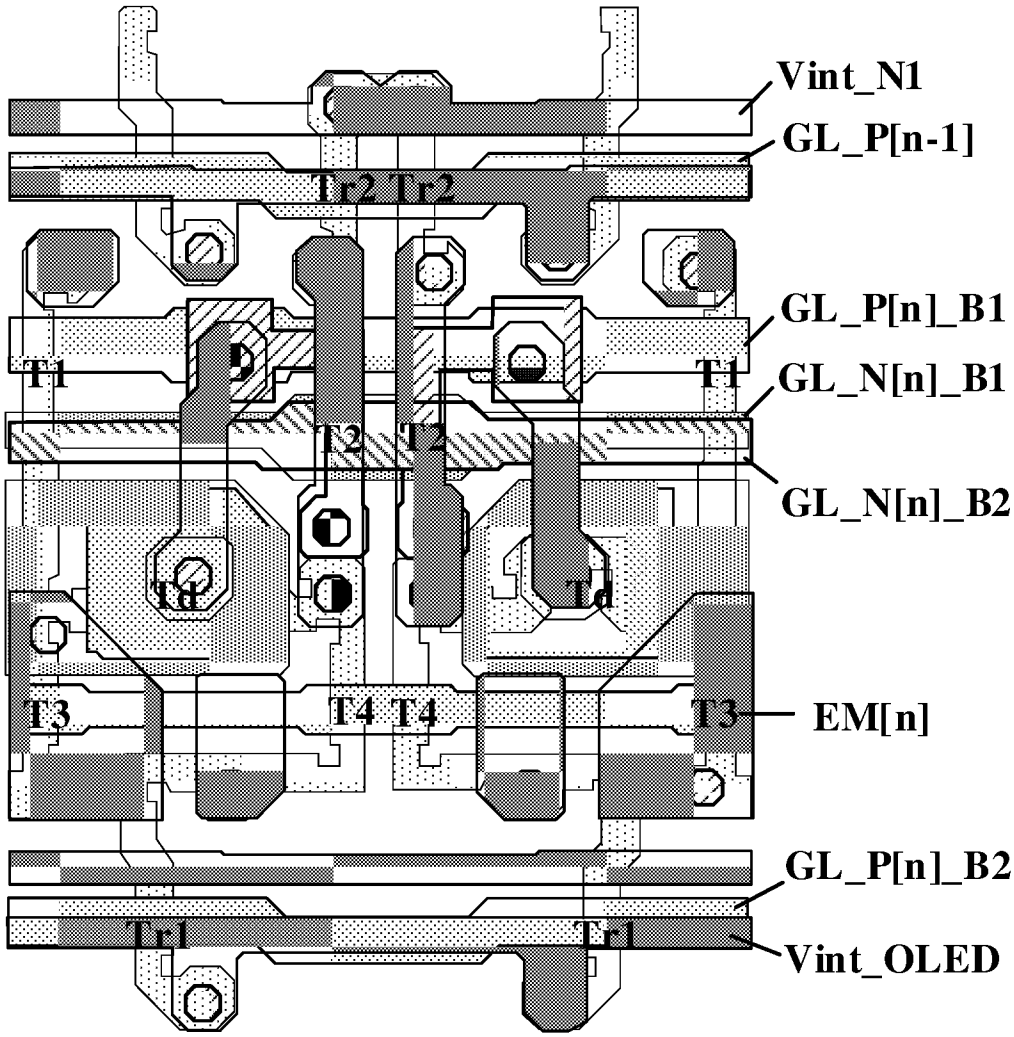
Vint_N1
GL_P[n-1]
Tr2 Tr2
GL_P[n]_B1
T1
T1
GL_N[n]_B1
T2 T2
GL_N[n]_B2
Td
Td
T3
T4 T4
T3
EM[n]
GL_P[n]_B2
Tr1
Tr1
Vint_OLED

FIG. 7A

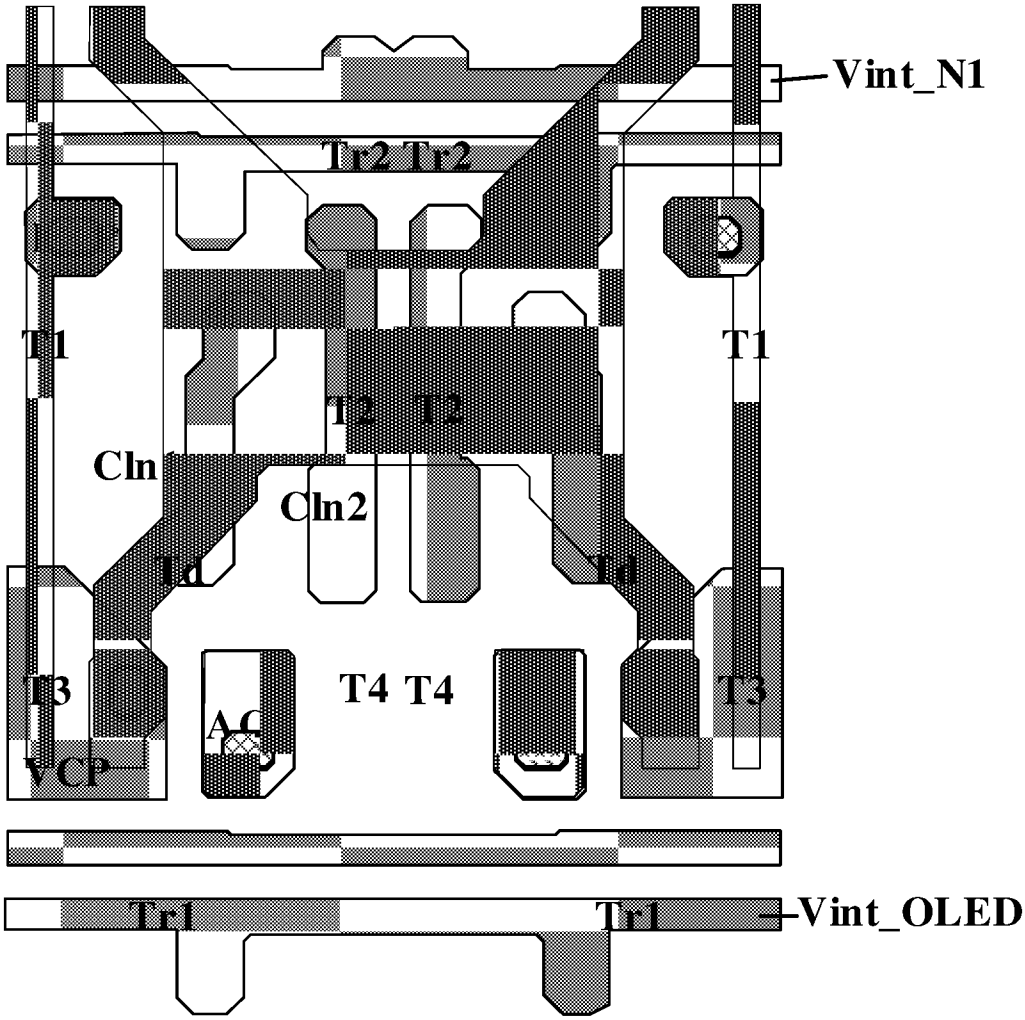
Vint_N1
Tr2 Tr2
T1
T1
T2 T2
Cln
Cln2
Td
Td
T3
T4 T4
T3
AG
VCP
Tr1
Tr1
Vint_OLED

FIG. 7B

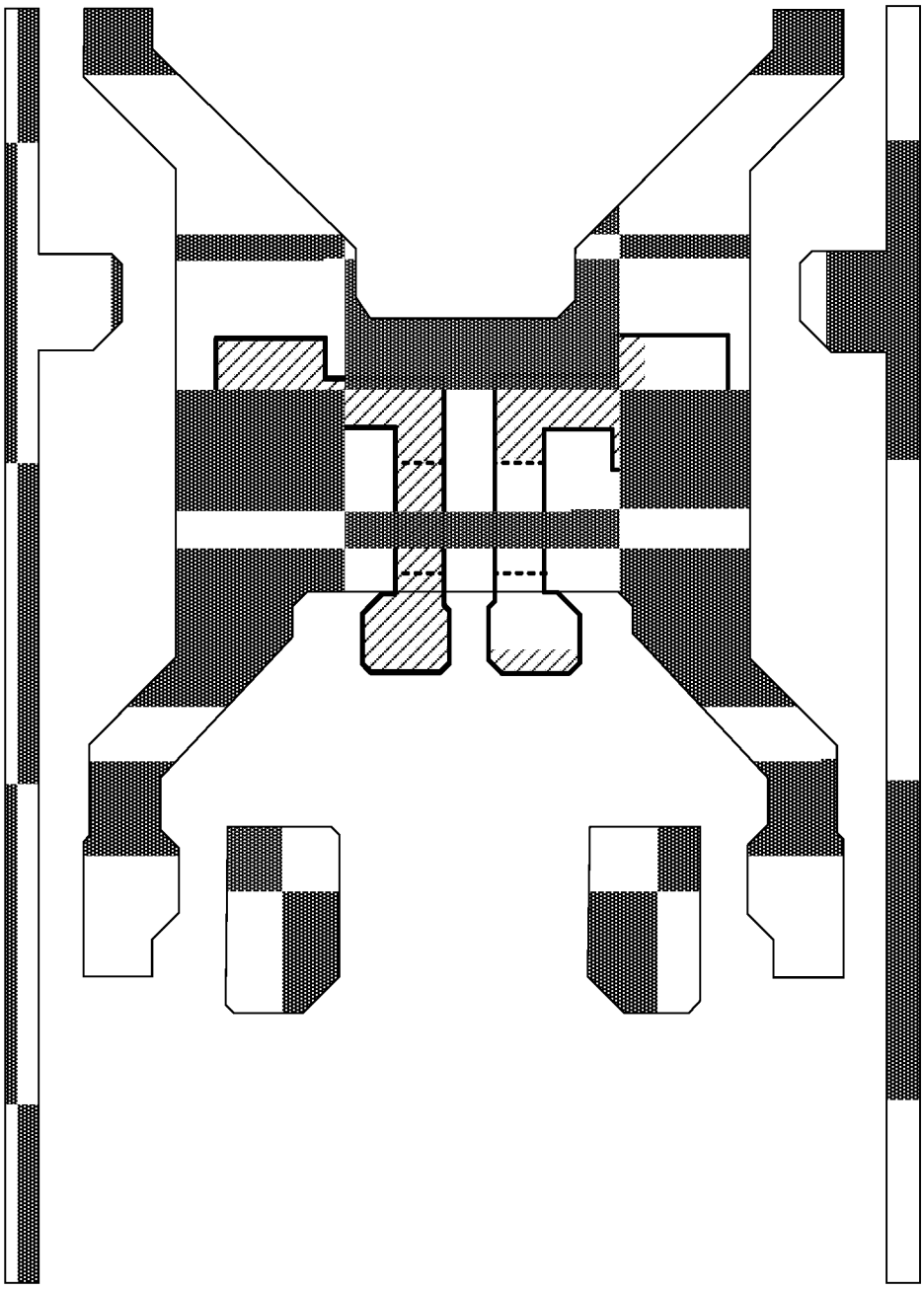

FIG. 7C

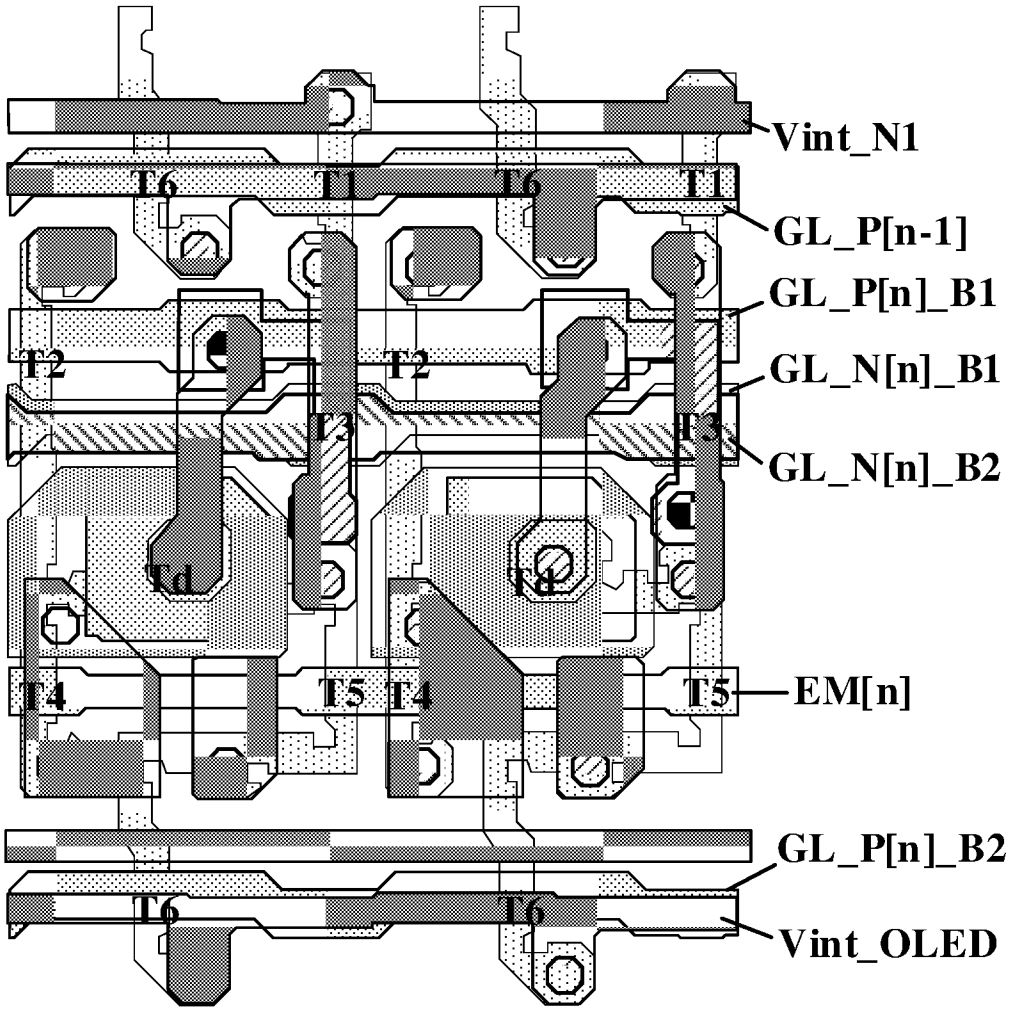
Vint_N1
T6
T1
T6
T1
GL_P[n-1]
GL_P[n]_B1
T2
T2
GL_N[n]_B1
T3
T3
GL_N[n]_B2
Td
Td
T4
T5
T4
T5
EM[n]
GL_P[n]_B2
T6
T6
Vint_OLED

FIG. 8A

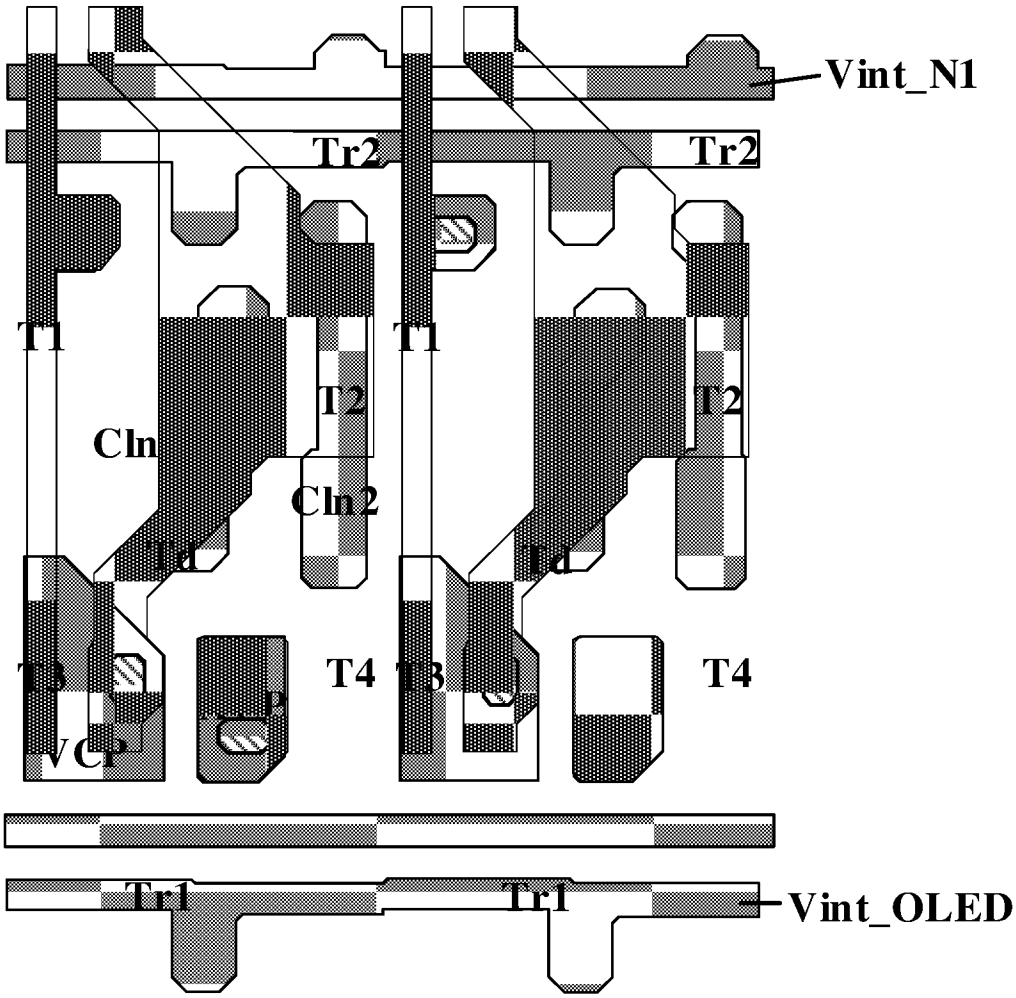
Vint_N1
Tr2
Tr2
T1
T1
T2
T2
Cln
Cln2
Td
Td
T3
T4
T3
T4
VCP
Tr1
Tr1
Vint_OLED

FIG. 8B

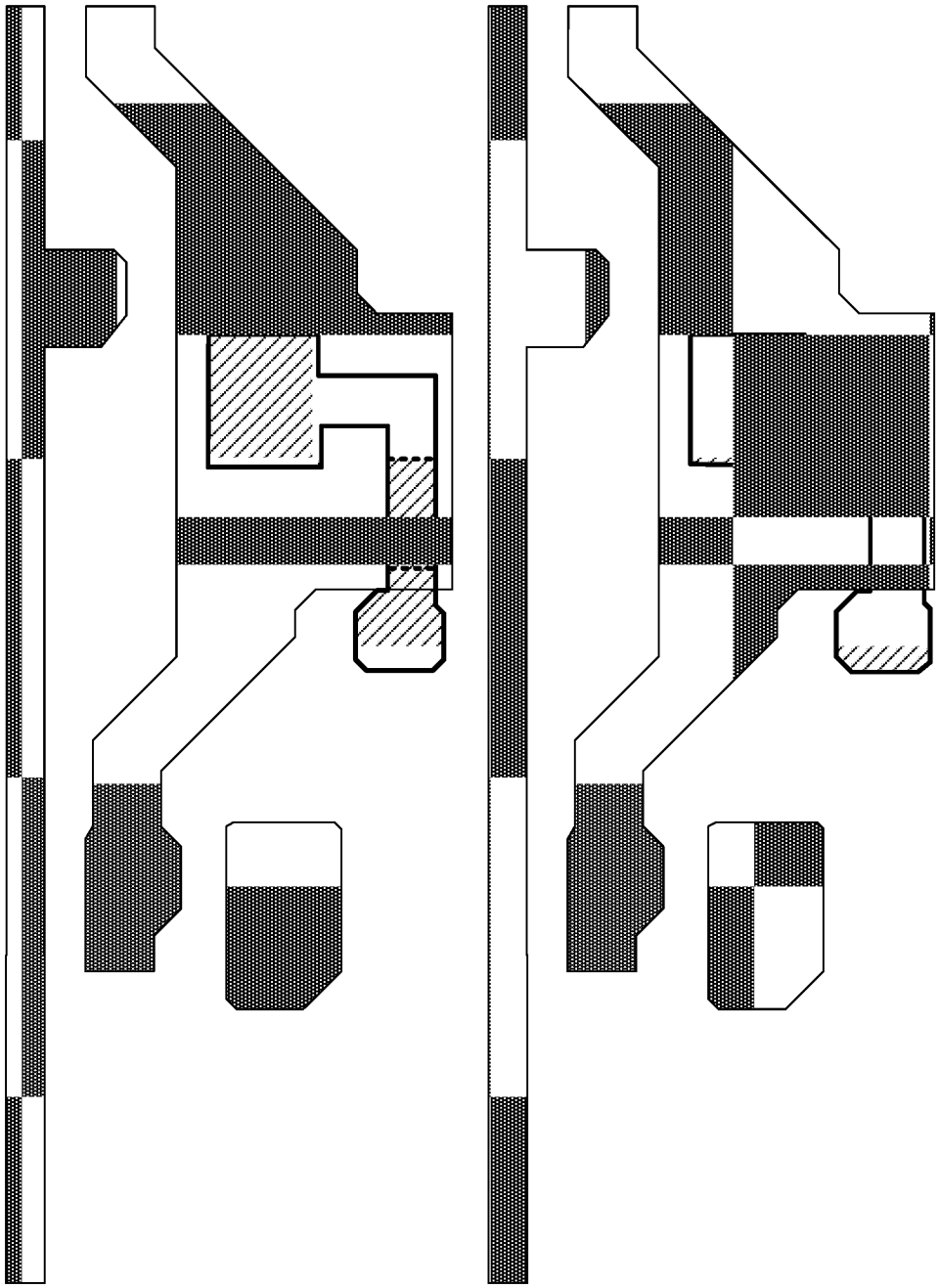

FIG. 8C

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2021/119060

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2016.01)i; H01L 27/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G3; H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS,CNTXT,ENTXTC,VEN:pixel?,driv+,?led,el,light+,diode,7t1c,seven+,six+,eight+,transistor?,switch+,+tft,+fet,mos+, capacit+,reset,initial+,anode,drain,previous,present,gate,scan+,line

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 109087610 A (WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD) 25 December 2018 (2018-12-25) description, page1, page 4 to page 7 and figures 2-6	1-33
X	CN 113257192 A (KUNSHAN GOVISIONOX OPTOELECTRONICS CO., LTD.) 13 August 2021 (2021-08-13) description, page 3 to page 9 and figures 2-13	1-33
X	CN 112785956 A (SAMSUNG DISPLAY CO., LTD.) 11 May 2021 (2021-05-11) description, page 4 to page 16 and figures 1-12	1-33
X	CN 112289269 A (HEFEI VISIONOX TECHNOLOGY CO., LTD.) 29 January 2021 (2021-01-29) description, page 3 to page 8 and figures 1-6	1-33
A	CN 112133253 A (GUANGDONG OPPO MOBILE TELECOMMUNICATIONS CORP. LTD.) 25 December 2020 (2020-12-25) the whole document	1-33
A	US 2017294503 A1 (SAMSUNG DISPLAY CO LTD) 12 October 2017 (2017-10-12) the whole document	1-33

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 June 2022	**21 June 2022**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China** Facsimile No. **(86-10)62019451**	Authorized officer **WANG,Chao** Telephone No. **(86-10)62085834**

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017062538 A1 (SAMSUNG DISPLAY CO LTD) 02 March 2017 (2017-03-02) the whole document	1-33
A	CN 112585761 A (BOE TECHNOLOGY GROUP CO., LTD. et al.) 30 March 2021 (2021-03-30) the whole document	1-33
A	CN 109473063 A (WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD.) 15 March 2019 (2019-03-15) the whole document	1-33

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2021/119060

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	109087610	A	25 December 2018	US	2021118361	A1	22 April 2021
				WO	2020037767	A1	27 February 2020
CN	113257192	A	13 August 2021		None		
CN	112785956	A	11 May 2021	US	2021134210	A1	06 May 2021
				KR	20210054114	A	13 May 2021
CN	112289269	A	29 January 2021		None		
CN	112133253	A	25 December 2020		None		
US	2017294503	A1	12 October 2017	US	2021242302	A1	05 August 2021
				US	2019027552	A1	24 January 2019
				US	2020185487	A1	11 June 2020
				KR	20160058330	A	25 May 2016
				US	2016141350	A1	19 May 2016
US	2017062538	A1	02 March 2017	KR	20170024203	A	07 March 2017
CN	112585761	A	30 March 2021	US	2021320156	A1	14 October 2021
				US	2022123089	A1	21 April 2022
				WO	2021018301	A1	04 February 2021
				WO	2021018304	A1	04 February 2021
				CN	113056828	A	29 June 2021
				WO	2021018303	A2	04 February 2021
				US	2021319754	A1	14 October 2021
CN	109473063	A	15 March 2019	US	2020327853	A1	15 October 2020
				WO	2020113790	A1	11 June 2020